PMC-Sierra

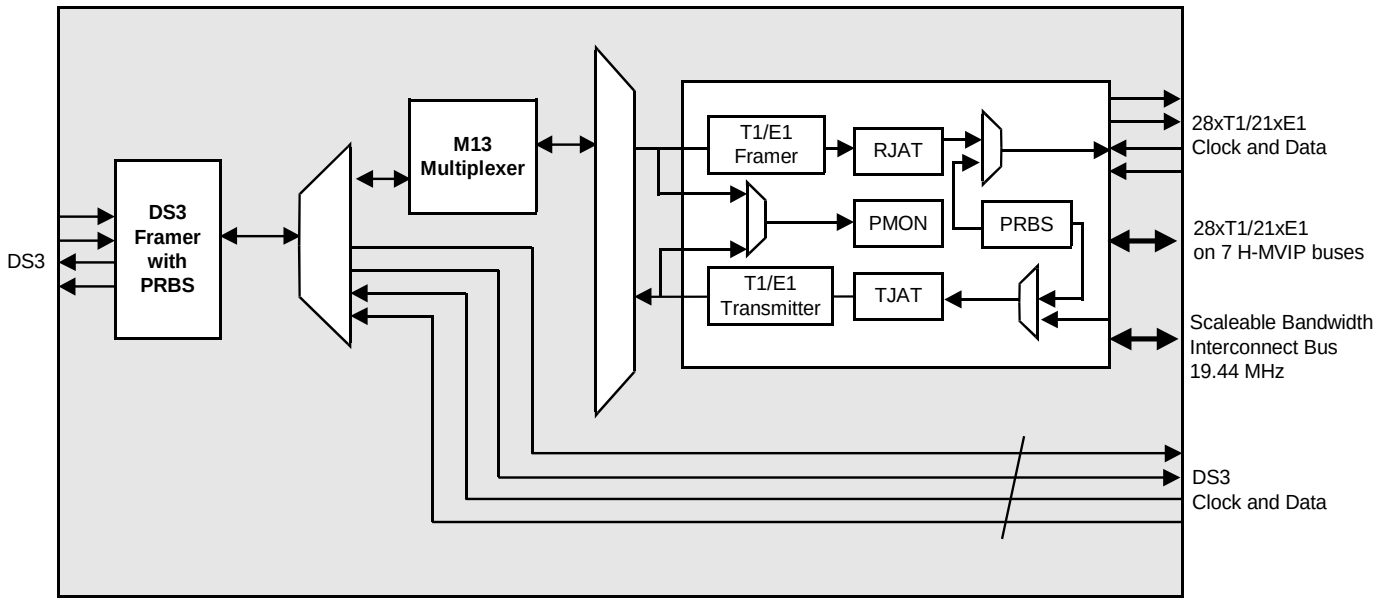
PM4328
TECT3

High Density T1/E1 Framer with Integrated M13 Multiplexer

FEATURES

- Integrates 28 T1 framers, 21 E1 framers and a full featured M13 multiplexer with DS3 framer in a single monolithic device for terminating DS3 multiplexed T1 or E1 streams.
- Four fundamental modes of operation:
  - Up to 28 T1 streams M13 multiplexed into a serial DS3.
  - Up to 21 E1 streams multiplexed into a DS3 following the ITU-T G.747 recommendation (using the serial clock and data or H-MVIP system interfaces).
  - DS3 M13 Multiplexer with ingress or egress per link monitoring.
  - Unchannelized DS3 framer mode for access to the entire DS3 payload.
- Supports transfer of PCM data to/from 1.544 MHz and 2.048 MHz serial interface system-side devices. Also supports a fractional T1 or E1 system interface with independent ingress/ egress Nx64 Kbps rates. Supports a 2.048 MHz system-side interface for T1 mode without external clock gapping.
- Supports 8 Mbps H-MVIP on the system interface for all T1 or E1 links, a separate 8 Mbps H-MVIP system interface for all T1 or E1 CAS channels and a separate 8 Mbps H-MVIP system interface for all T1 or E1 CCS and V5.1/V5.2 channels.
- Supports a byte serial Scaleable Bandwidth Interconnect (SBI) bus interface for high density system side device interconnection of up to 84 T1 streams or 3 DS3 streams.
- Provides jitter attenuation in the T1 or E1 receive and transmit directions.
- Provides two independent de-jittered T1 or E1 recovered clocks for system timing and redundancy.
- Provides per-DS0 line loopback and per link diagnostic and line loopbacks.
- Provides an on-board programmable binary sequence generator and detector for error testing at DS3 rates. Includes support for patterns recommended in ITU-T O.151.
- Also provides PRBS generators and detectors on each tributary for error testing at DS1, E1 and NxDS0 rates as recommended in ITU-T O.151 and O.152.
- Provides robbed bit signaling extraction and insertion on a per-DS0 basis.
- Provides programmable idle code substitution, data and sign inversion, and digital milliwatt code insertion on a per-DS0 basis.
- Supports the M23 and C-bit parity DS3 formats.
- Standalone unchannelized DS3 framer mode for access to the entire DS3 payload.
- When configured to operate as a DS3 Framer, gapped transmit and receive clocks can be optionally generated for interface to link layer devices which only need access to payload data bits.
- DS3 Transmit clock source can be selected from either an external oscillator or from the receive side clock (loop-timed).
- Register level compatibility with the PM4388 TOCTL Octal T1 Framer, the PM6388 EOCTL Octal E1 Framer, the PM4351 COMET E1/T1 transceiver and the PM8313 D3MX M13 Multiplexer/Demultiplexer.

BLOCK DIAGRAM



High Density T1/E1 Framer with Integrated M13 Multiplexer

- Provides a generic 8-bit microprocessor bus interface for configuration, control and status monitoring.
- Provides a standard 5 signal P1149.1 JTAG test port for boundary scan board test purposes.

VOLTAGE

- Low power 2.5 V/3.3 V CMOS technology. All pins are 5 V tolerant.

PACKAGE

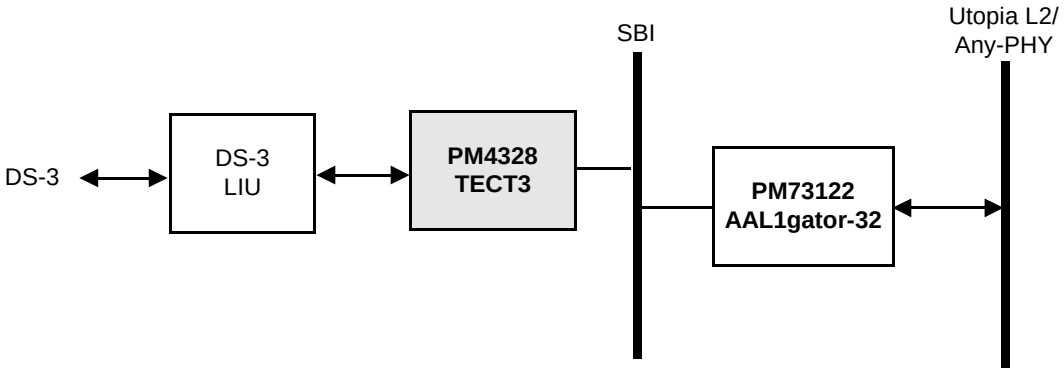
- 324-pin fine pitch PBGA package (23 mm x 23 mm).
- Supports industrial temperature range (-40 ^{o}C to 85 ^{o}C) operation.

APPLICATIONS

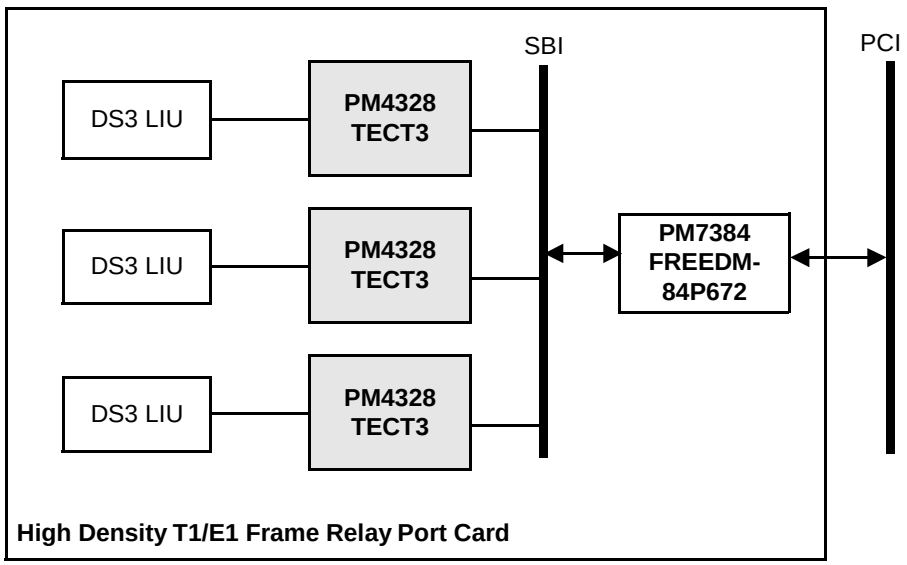
- High density T1 interfaces for multiplexers, multi-service switches, routers and digital modems.
- High density E1 interfaces for multiplexers, multi-service switches, routers and digital modems.
- Frame Relay switches and access devices (FRADS).
- M23 Based M13 Multiplexer.
- C-Bit Parity Based M13 Multiplexer.
- Channelized and Unchannelized DS3 Frame Relay Interfaces.

TYPICAL APPLICATIONS

CHANNELIZED DS3 CIRCUIT EMULATION APPLICATION



HIGH DENSITY FRAME RELAY APPLICATION



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