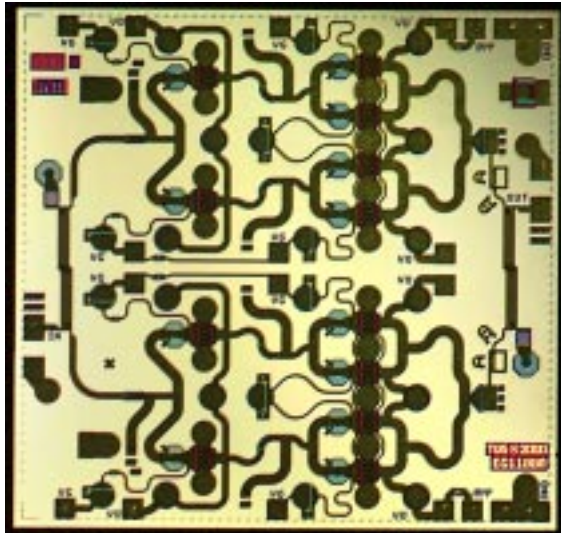


**36 to 40 GHz 1W Power Amplifier**

**TGA1171-SCC**



**Key Features and Performance**

- 0.25  $\mu\text{m}$  pHEMT Technology
- 36-40 GHz Frequency Range
- 29 dBm Nominal Pout @ P1dB, 38 GHz
- 14 dB Nominal Gain
- OTOI 36 dBm at 40 GHz typical
- Bias 6-7 V @ 500 mA
- Chip Dimensions: 2.863 mm x 2.740 mm x 0.1016 mm

**Primary Applications**

- Point-to-Point Radio
- Point-to-Multipoint Radio

**Product Description**

The TriQuint TGA1171-SCC is a two-stage PA MMIC design using TriQuint's proven 0.25  $\mu\text{m}$  Power pHEMT process to support a variety of millimeter wave applications including point-to-point digital radio and point-to-multipoint systems.

The balanced design consists of four 400  $\mu\text{m}$  input devices driving eight 400  $\mu\text{m}$  output devices.

The TGA1171 provides 29 dBm of output power at 1 dB gain compression and >30 dBm saturated output power across 36-40 GHz with a typical small signal gain of 14 dB. Typical Input/Output RL is typically greater than 12-15 dB across the band.

The TGA1171 requires minimal off-chip components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form.

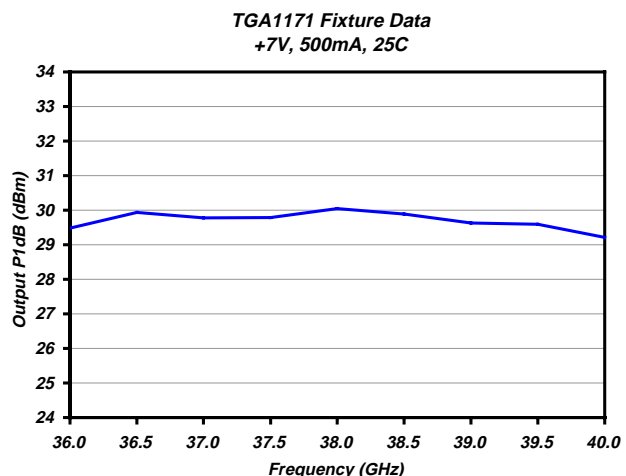
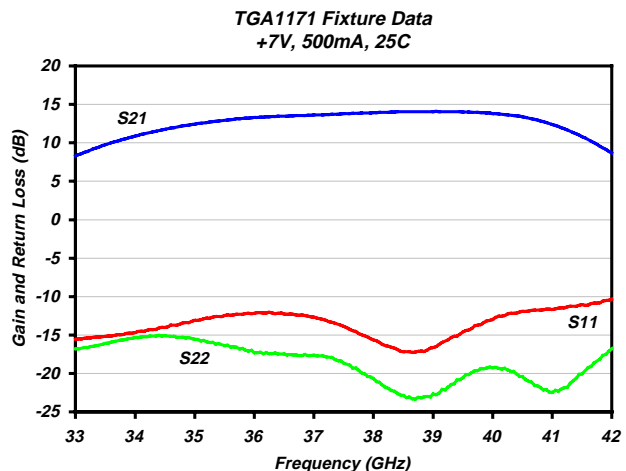


TABLE I  
MAXIMUM RATINGS

Symbol	Parameter <u>5/</u>	Value	Notes
V <sup>+</sup>	Positive Supply Voltage	8 V	<u>4/</u>
V <sup>-</sup>	Negative Supply Voltage Range	-5V TO 0V	
I <sup>+</sup>	Positive Supply Current (Quiescent)	960 mA	<u>4/</u>
I <sub>G</sub>	Gate Supply Current	56.32 mA	
P <sub>IN</sub>	Input Continuous Wave Power	27 dBm	<u>4/</u>
P <sub>D</sub>	Power Dissipation	5.25 W	<u>3/ 4/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>1/ 2/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T<sub>M</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 9.5 E+6 to 6.1 E+5 hours.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 5/ These ratings represent the maximum operable values for this device.

TABLE II  
 DC PROBE TEST  
 (TA = 25 °C ± 5 °C)

Symbol	Parameter	Minimum	Maximum	Unit
$I_{DSS(Q3-6)}$	Saturated Drain Current	160	752	mA
$G_{m(Q3-6)}$	Transconductance	352	848	mS
$V_P$	Pinch-off Voltage	-1.5	-0.5	V
$BVGS_{(Q3-6)}$	Breakdown Voltage Gate-Source	-30	-11	V
$BVGD_{(Q3-6)}$	Breakdown Voltage Gate-Drain	-30	-11	V

TABLE III  
 AUTOPROBE FET PARAMETER MEASUREMENT CONDITIONS

FET Parameters	Test Conditions
$I_{DSS}$ : Maximum drain current ( $I_{DS}$ ) with gate voltage ( $V_{GS}$ ) at zero volts.	$V_{GS} = 0.0$ V, drain voltage ( $V_{DS}$ ) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of $I_{DS}$ ; voltage for $I_{DSS}$ is recorded as VDSP.
$G_m$ : Transconductance; $\frac{(I_{DSS} - IDS1)}{VG1}$	For all material types, $V_{DS}$ is swept between 0.5 V and VDSP in search of the maximum value of $I_{ds}$ . This maximum $I_{DS}$ is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at $V_{GS} = VG1 = -0.5$ V. For Low Noise, HFET and pHEMT material, $V_{GS} = VG1 = -0.25$ V. For LNBECOLC, use $V_{GS} = VG1 = -0.10$ V.
$V_P$ : Pinch-Off Voltage; $V_{GS}$ for $I_{DS} = 0.5$ mA/mm of gate width.	$V_{DS}$ fixed at 2.0 V, $V_{GS}$ is swept to bring $I_{DS}$ to 0.5 mA/mm.
$V_{BVDG}$ : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current ( $I_{BD}$ ) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage ( $V_{GD}$ ) measured is $V_{BVDG}$ and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
$V_{BVGS}$ : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current ( $I_{BS}$ ) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage ( $V_{GS}$ ) measured is $V_{BVGS}$ and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

TABLE IV  
RF WAFER CHARACTERIZATION TEST

( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )  
( $V_d = 7\text{V}$ ,  $I_d = 500\text{ mA} \pm 5\%$ )

Parameter	Unit	Min	Typical	Max
Frequency	GHz	36		40
Output P1dB	dBm	26	29	
Small Signal Gain	dB	12	14	
Input Return Loss	dB		-15	
Output Return Loss	dB		-15	
Output TOI	dBm		36	

TABLE V  
THERMAL INFORMATION\*

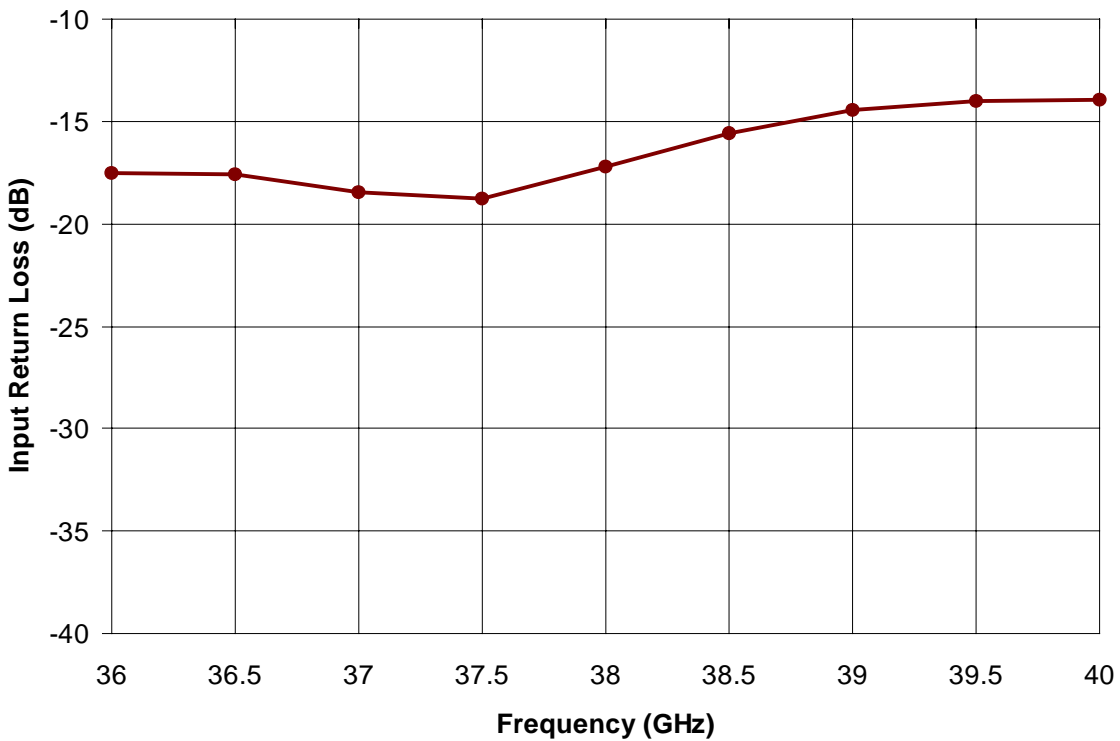
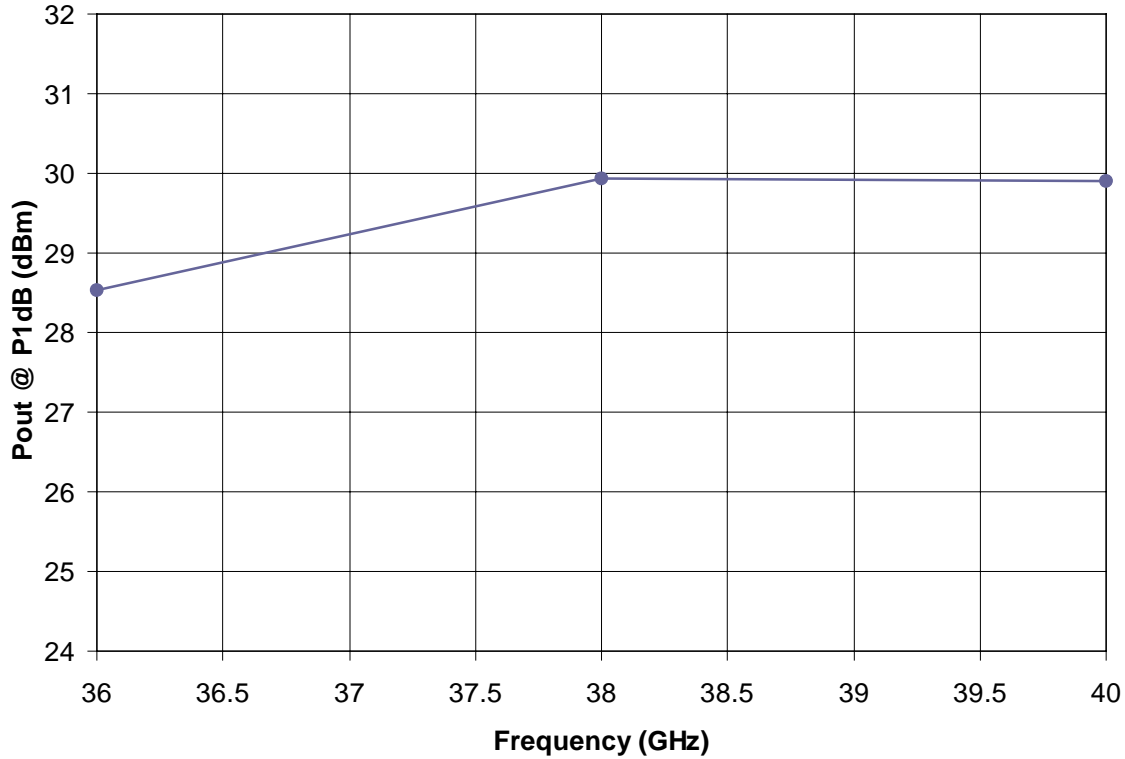
Parameter	Test Conditions	$T_{CH}$ ( $^\circ\text{C}$ )	$R_{\theta JC}$ ( $^\circ\text{C/W}$ )	$T_M$ (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	$V_d = 7\text{V}$ $I_D = 500\text{ mA}$ $P_{diss} = 3.5\text{ W}$	125.03	15.79	9.5 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

\* This information is a result of a thermal model analysis.

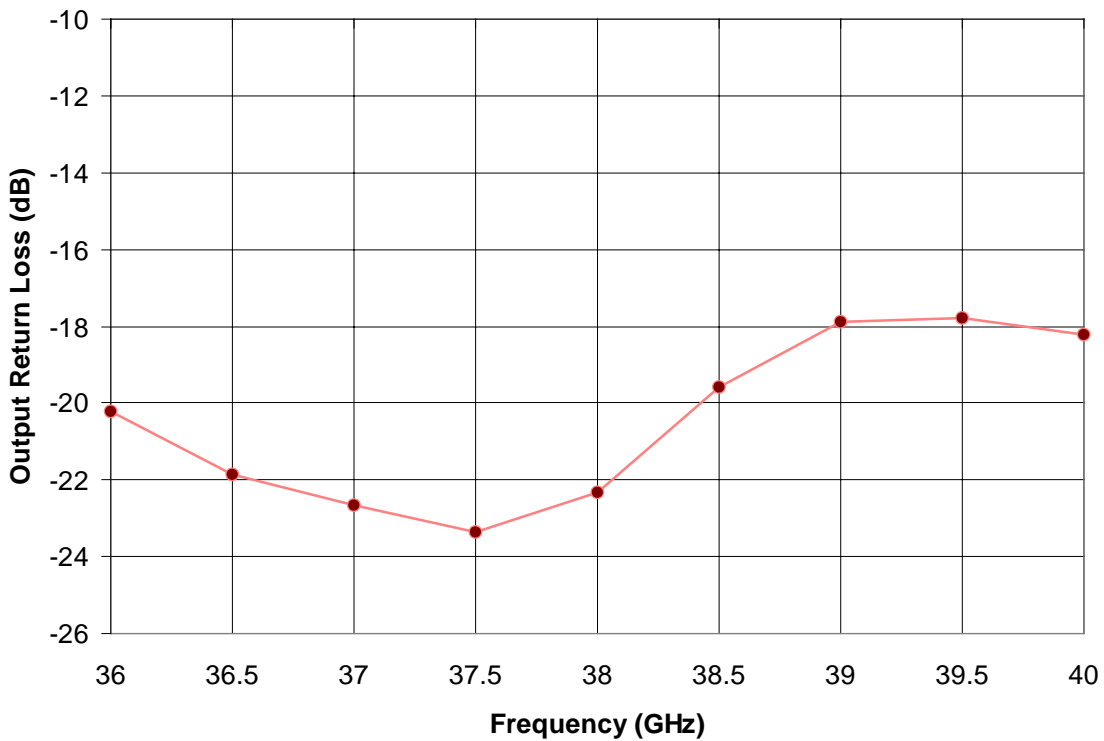
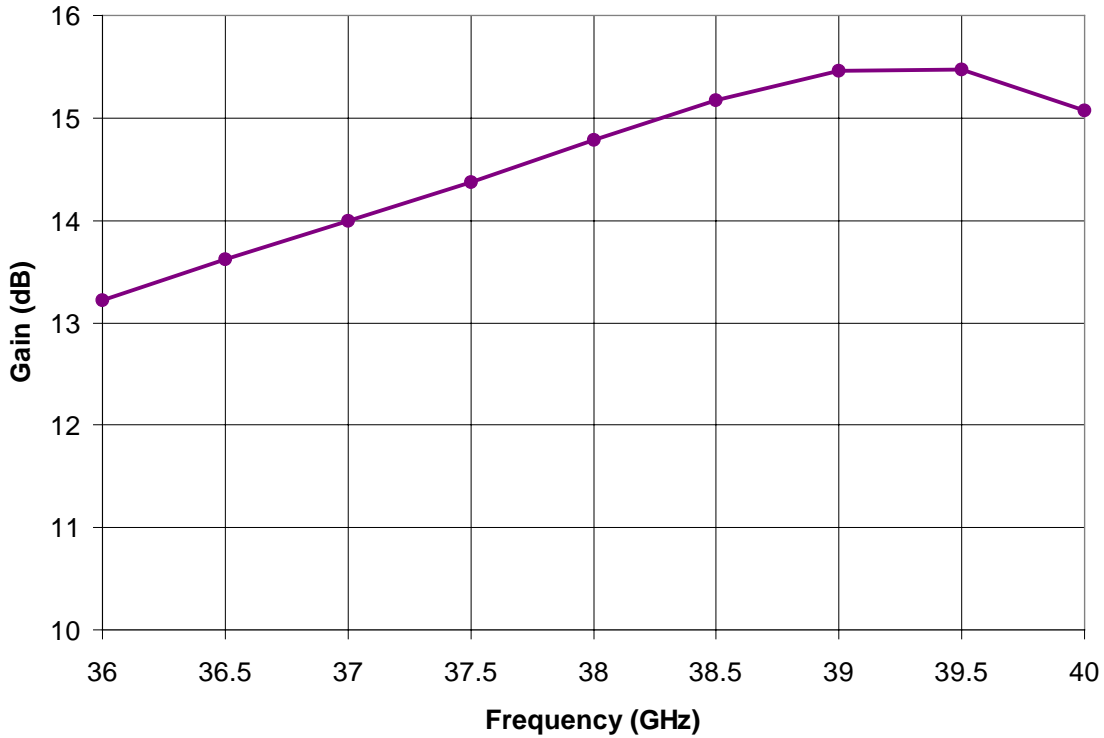
**Data Based on the 50th percentile On-Wafer RF Probe Test Results, Sample Size = 13971 Devices**

**Bias Conditions:  $V_d = 7\text{ V}$ ,  $I_d = 500\text{ mA}$**

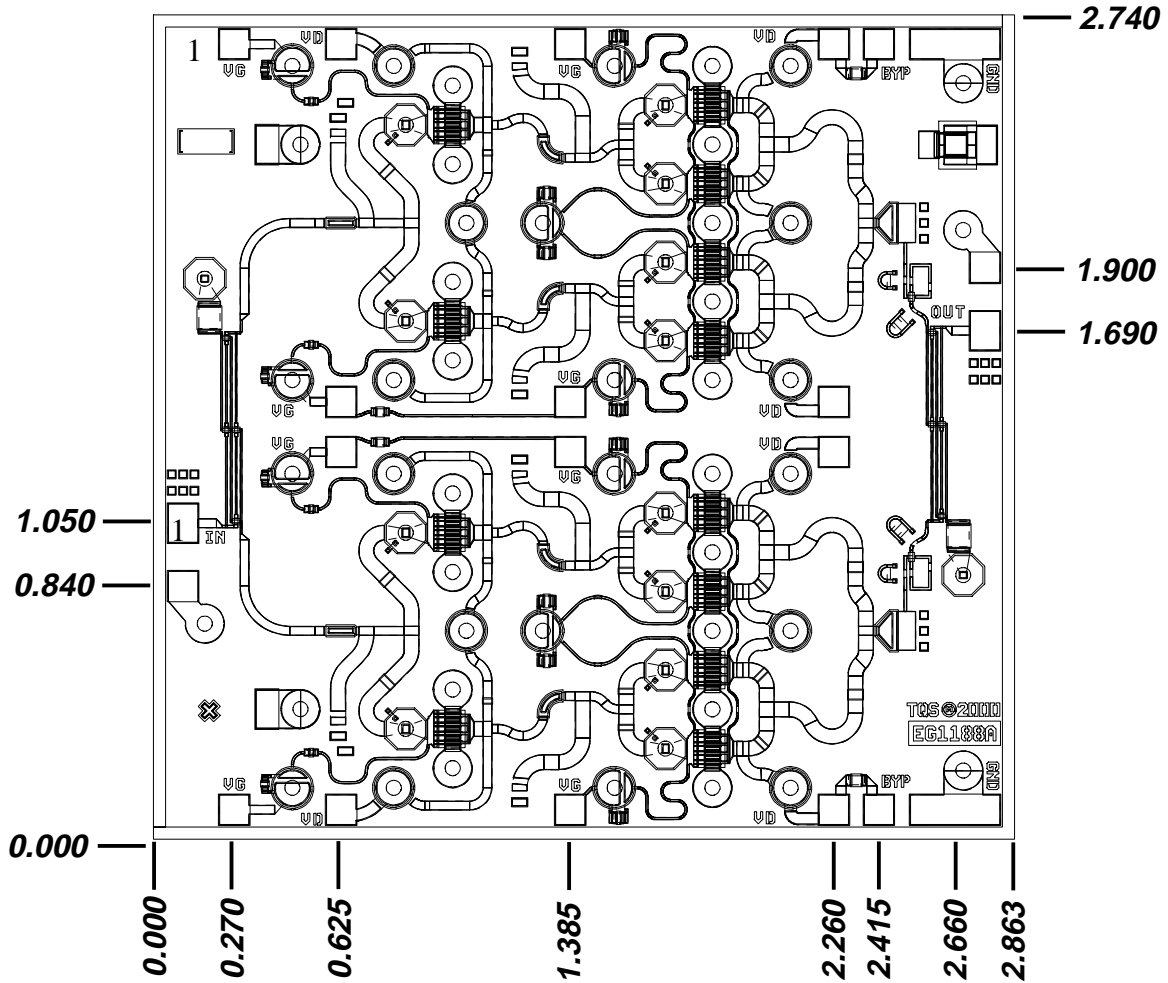


**Data Based on the 50th percentile On-Wafer RF  
Probe Test Results, Sample Size = 13971 Devices**

**Bias Conditions:  $V_d = 7\text{ V}$ ,  $I_d = 500\text{ mA}$**



**Mechanical Characteristics**

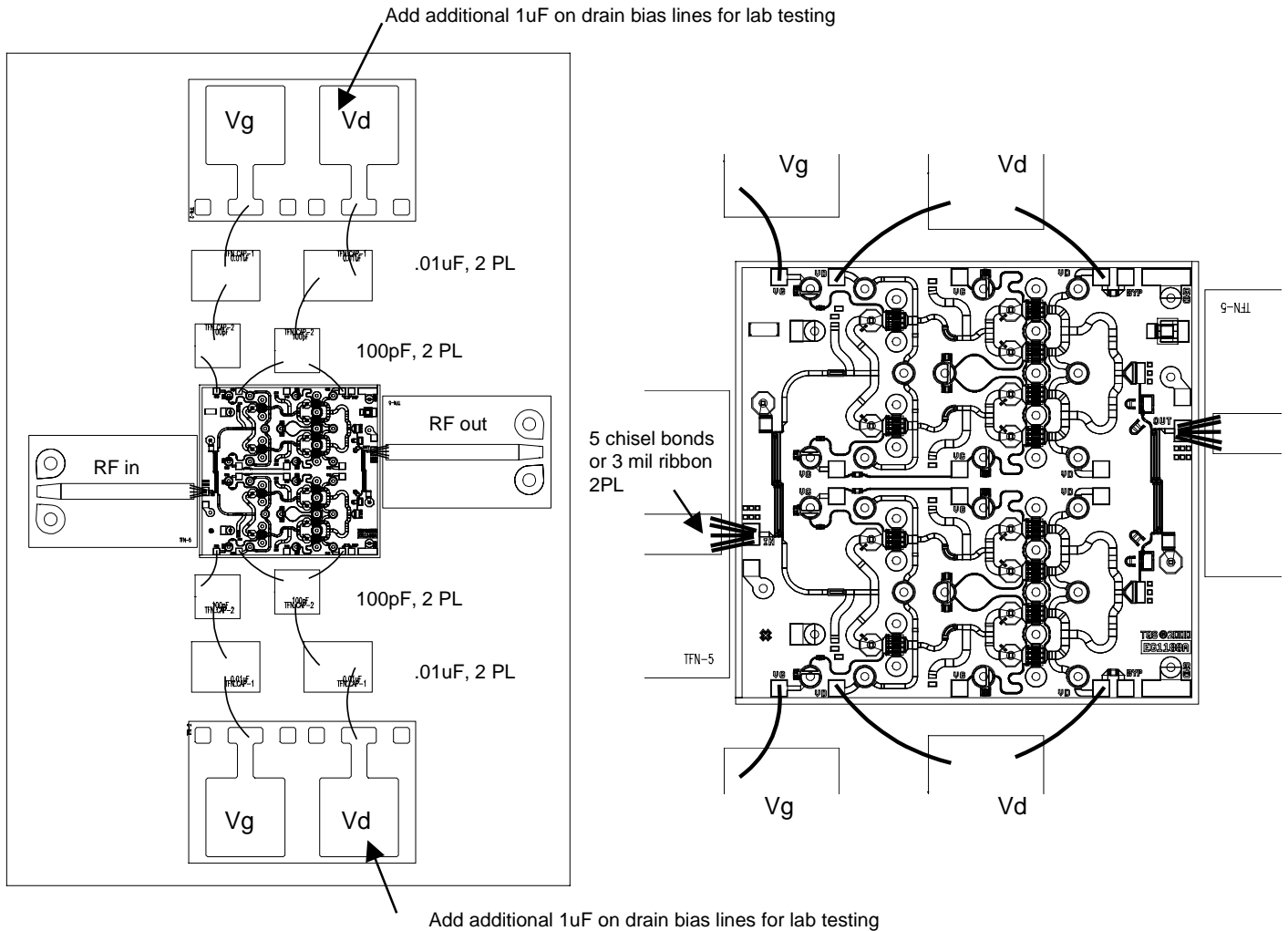


**Dimensions in mm**

**RF Pads: 130x100  $\mu\text{m}$**

**DC Pads: 100x100  $\mu\text{m}$**

**Die Area: 7.845  $\text{mm}^2$**



## Chip Assembly and Bonding Diagram

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**



## Assembly Process Notes

### Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

### Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

### Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***