



## GENERAL DESCRIPTION



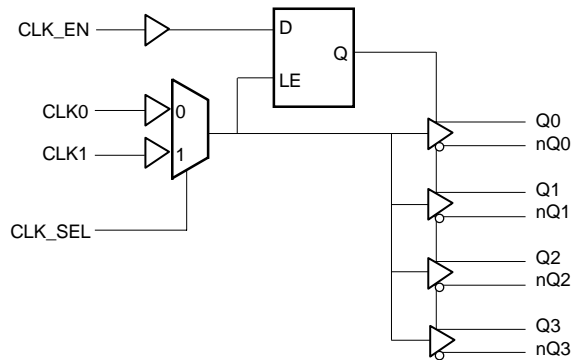
The ICS8525 is a low skew, high performance 1-to-4 LVCMOS-to-LVHSTL fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8525 has two selectable clock inputs that accept LVCMOS or LVTTTL input levels and translate them to LVHSTL levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8525 ideal for those applications demanding well defined performance and repeatability.

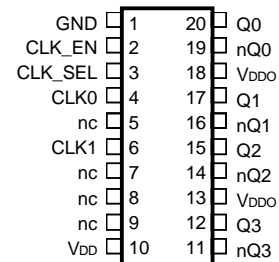
## FEATURES

- 4 differential LVHSTL compatible outputs
- Selectable LVCMOS / LVTTTL clock inputs for redundant and multiple frequency fanout applications
- Maximum output frequency: 266MHz
- Translates LVCMOS and LVTTTL levels to LVHSTL levels
- Output skew: 35ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.9ns (maximum)
- 3.3V core, 1.8V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS8525**  
**20-Lead TSSOP**  
6.5mm x 4.4mm x 0.92mm Package Body  
**G Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS / LVTTTL interface levels.
4	CLK0	Input	Pulldown	LVCMOS / LVTTTL clock input.
6	CLK1	Input	Pulldown	LVCMOS / LVTTTL clock input.
5, 7, 8, 9	nc	Unused		No connect.
10	V <sub>DD</sub>	Power		Positive supply pin.
13, 18	V <sub>DDO</sub>	Power		Output supply pins.
11, 12	nQ3, Q3	Output		Differential output pair. LVHSTL interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVHSTL interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVHSTL interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVHSTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance				4	pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ

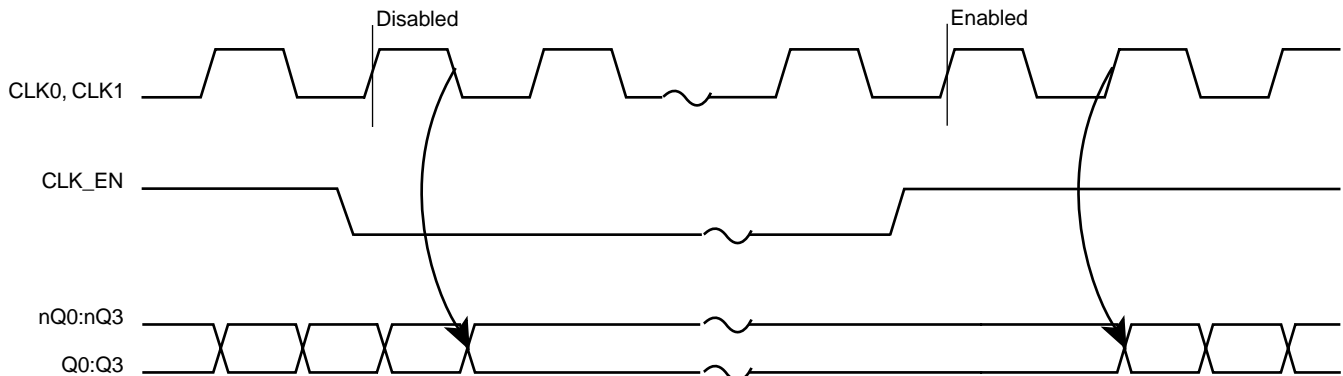


**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1.

In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3B.



**FIGURE 1 - CLK\_EN TIMING DIAGRAM**

**TABLE 3B. CLOCK INPUT FUNCTION TABLE**

Inputs	Outputs	
CLK0 or CLK1	Q0:Q3	nQ0:nQ3
0	LOW	HIGH
1	HIGH	LOW



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DDx}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current				50	mA

**TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	CLK0, CLK1		2	3.765	V
		CLK_EN, CLK_SEL		2	3.765	V
$V_{IL}$	Input Low Voltage	CLK0, CLK1		-0.3	1.3	V
		CLK_EN, CLK_SEL		-0.3	0.8	V
$I_{IH}$	Input High Current	CLK0, CLK1, CLK_SEL	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		CLK_EN	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1, CLK_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		CLK_EN	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**TABLE 4C. LVHSTL DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1		1.2	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.4	V
$V_{OX}$	Output Crossover Voltage		$40\% \times (V_{OH} - V_{OL}) + V_{OL}$		$60\% \times (V_{OH} - V_{OL}) + V_{OL}$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.75		1.25	V

NOTE 1: Outputs terminated with 50Ω to GND.



**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Maximum Output Frequency				266	MHz
$t_{PD}$	Propagation Delay; NOTE 1	$f \leq 266MHz$	1.0		1.9	ns
$tsk(o)$	Output Skew; NOTE 2, 4				35	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 4				150	ps
$t_R$	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
$t_F$	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		45	50	55	%

All parameters measured at 266MHz unless noted otherwise.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1: Measured from the  $V_{DD}/2$  of the input to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

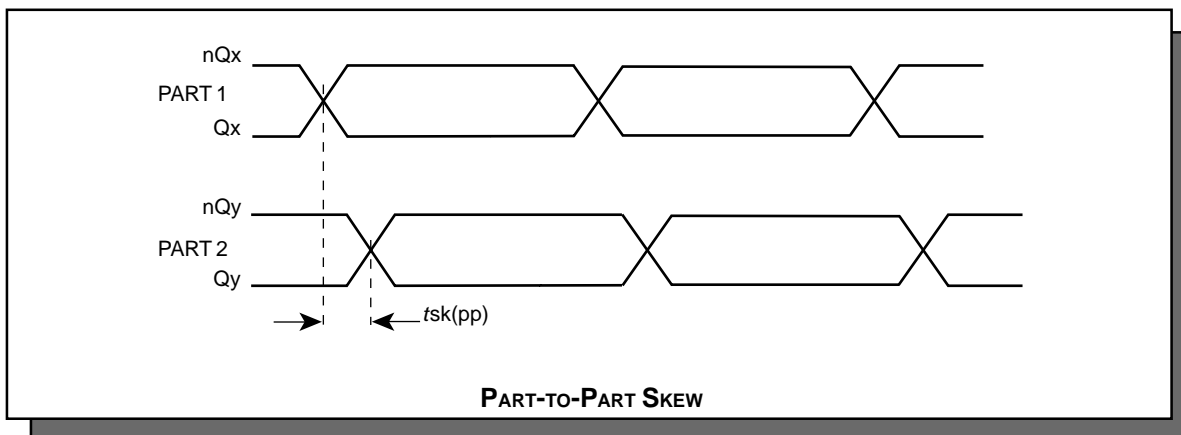
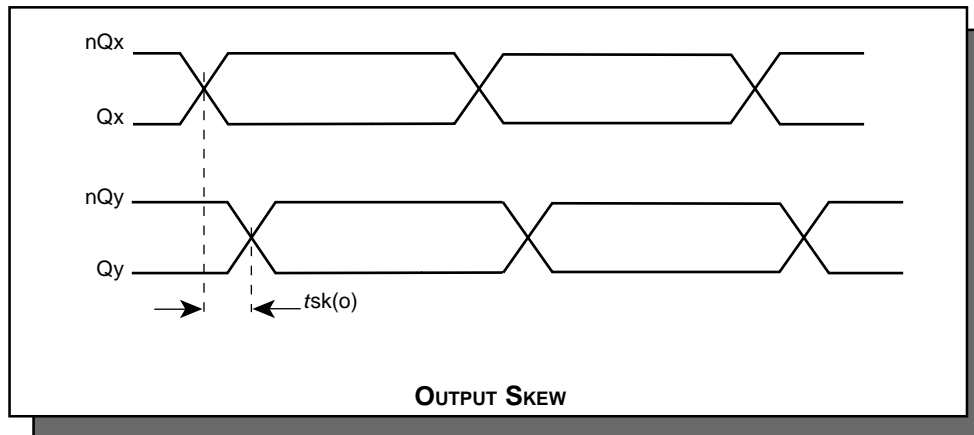
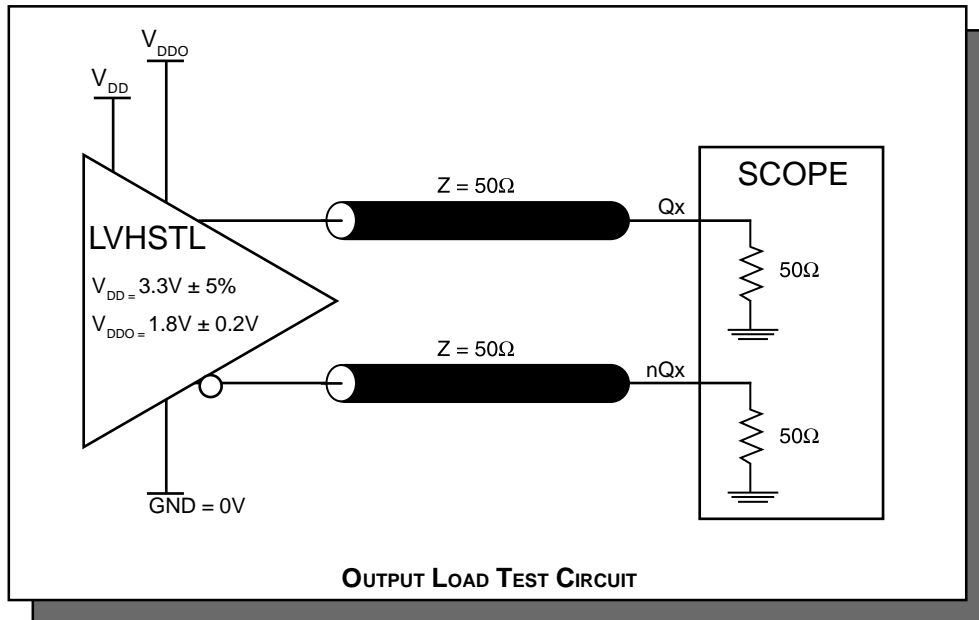
Measured at the output differential cross points.

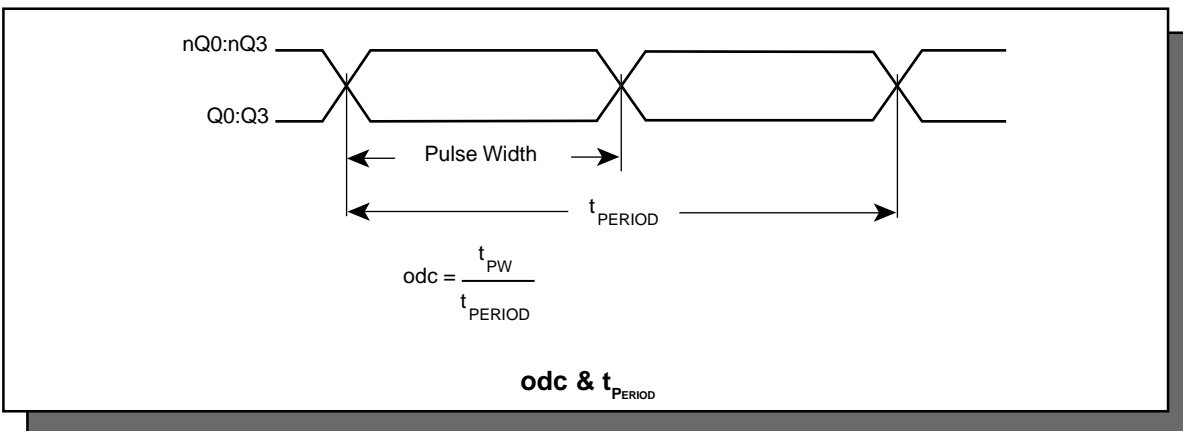
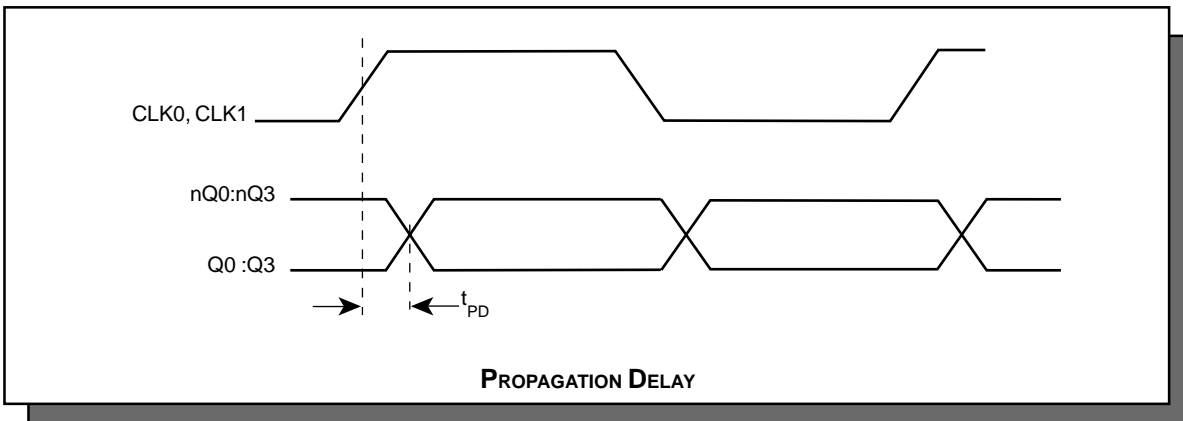
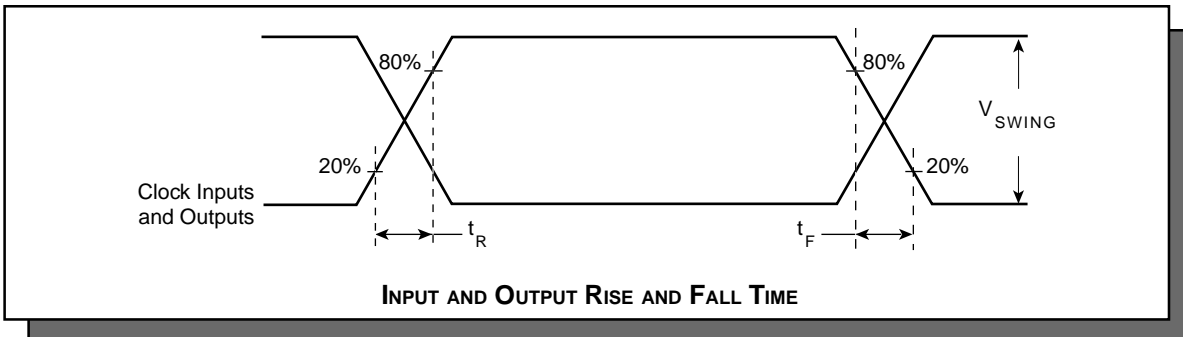
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.



## PARAMETER MEASUREMENT INFORMATION







## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8525. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8525 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 50mA = 173.25mW$
- Power (outputs)<sub>MAX</sub> = **32mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $4 * 32mW = 128mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 173.25mW + 128mW = 301.25mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-ambient thermal resistance

$Pd\_total$  = Total device power dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below. Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.301W * 66.6^\circ C/W = 90.05^\circ C. \text{ This is well below the limit of } 125^\circ C$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

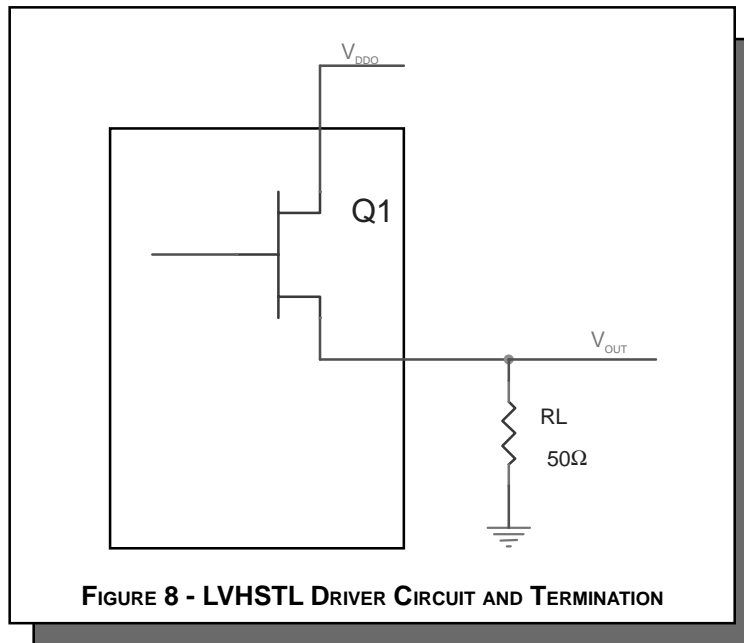




3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVHSTL output driver circuit and termination are shown in *Figure 8*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.  
Pd\_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd\_H = (1.2V/50\Omega) * (2V - 1.2V) = \mathbf{19.2mW}$$

$$Pd\_L = (0.4V/50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{32mW}$$



## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8525 is: 484



PACKAGE OUTLINE - G SUFFIX

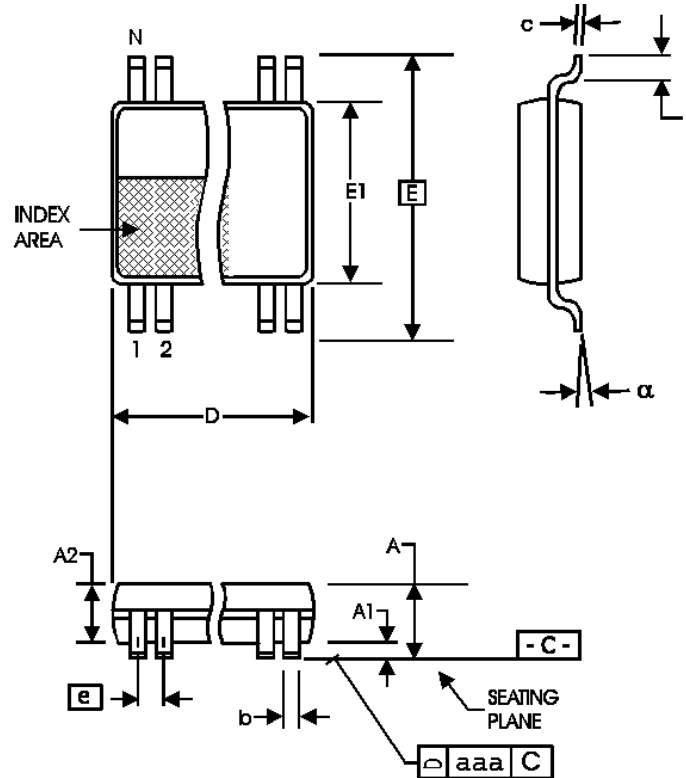


TABLE 8. PACKAGE DIMENSIONS

Symbol	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

REFERENCE DOCUMENT: JEDEC PUBLICATION 95, MO-153



Integrated  
Circuit  
Systems, Inc.

**ICS8525**  
LOW SKEW, 1-TO-4  
LVCMOS-TO-LVHSTL FANOUT BUFFER

**TABLE 9. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS8525BG	ICS8525BG	20 lead TSSOP	72 per tube	0°C to 70°C
ICS8525BG-T	ICS8525BG	20 lead TSSOP on Tape and Reel	2500	0°C to 70°C

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**ICS8525**  
LOW SKEW, 1-TO-4  
LVCMOS-TO-LVHSTL FANOUT BUFFER

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
B		3	Updated Figure 1, CLK_EN Timing Diagram.	10/17/01
B		3	Updated Figure 1, CLK_EN Timing Diagram.	11/2/01
B		1	Features section, deleted 1.8V in Bullet 1 and 4.	5/6/02