

September 1998

Features

- 1A, 80V and 100V
- $r_{DS(ON)} = 1.200\Omega$

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1N08	TO-205AF	RFL1N08
RFL1N10	TO-205AF	RFL1N10

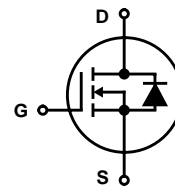
NOTE: When ordering, use the entire part number.

Description

These are N-channel enhancement mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

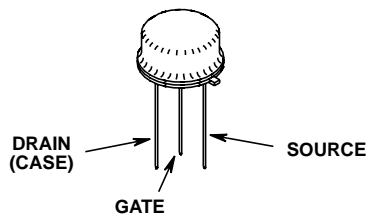
Formerly developmental type TA09282.

Symbol



Packaging

JEDEC TO-204AA



RFL1N08, RFL1N10

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFL1N08	RFL1N10	UNITS
Drain to Source Voltage (Note 1)	80	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	80	100	V
Continuous Drain Current	1	1	A
Pulsed Drain Current (Note 3)	5	5	A
Gate to Source Voltage	± 20	± 20	V
Maximum Power Dissipation	8.33	8.33	W
Linear Derating Factor	0.0667	0.0667	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 150	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	260	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage RFL1N08 RFL1N10	BV _{DSS}	I _D = 250 μ A, V _{GS} = 0V	80	-	-	V
			100	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250 μ A, (Figure 8)	2	-	4	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = Rated BV _{DSS} , V _{GS} = 0V	-	-	1	μ A
		V _{DS} = 0.8 x Rated BV _{DSS} , V _{GS} = 0V, T _J = 125 $^\circ\text{C}$	-	-	25	μ A
On-State Drain Current (Note 2)	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)MAX} , V _{GS} = 10V	1	-	-	A
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ± 20 V	-	-	± 100	nA
Drain to Source On Resistance	r _{DS(ON)}	I _D = 5.6A, V _{GS} = 10V, (Figures 6, 7)			1.200	Ω
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 50V, V _{GS} = 10V, I _D \approx 1A, R _G = 50 Ω , R _L = 50 Ω (Figures 10, 11, 12) MOSFET Switching Times are Essentially Inde- pendent of Operating Temperature	-	17	25	ns
Rise Time	t _r		-	30	45	ns
Turn-Off Delay Time	t _{d(OFF)}		-	30	45	ns
Fall Time	t _f		-	30	50	ns
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 9)	-	-	200	pF
Output Capacitance	C _{OSS}		-	-	80	pF
Reverse Transfer Capacitance	C _{RSS}		-	-	25	pF
Thermal Resistance Junction to Case	R _{θJC}		-	-		$^\circ\text{C}/\text{W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V _{SD}	T _J = 25 $^\circ\text{C}$, I _{SD} = 1A, V _{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t _{rr}	T _J = 25 $^\circ\text{C}$, I _{SD} = 1A, dI _{SD} /dt = 100A/ μ s	-	100	-	ns

NOTES:

2. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

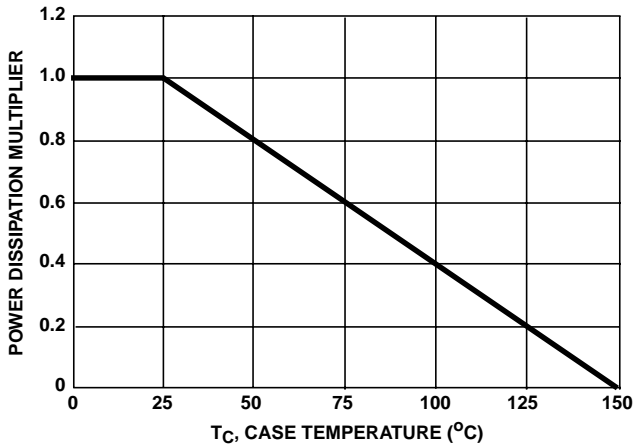


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

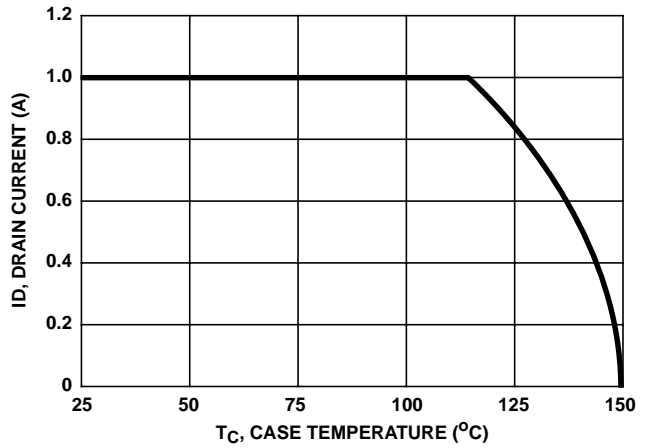


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

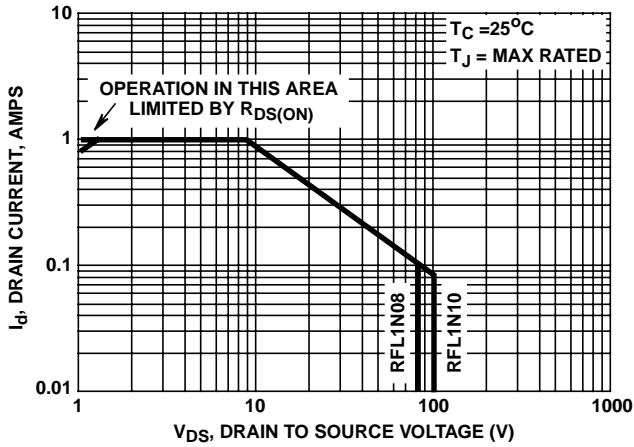


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

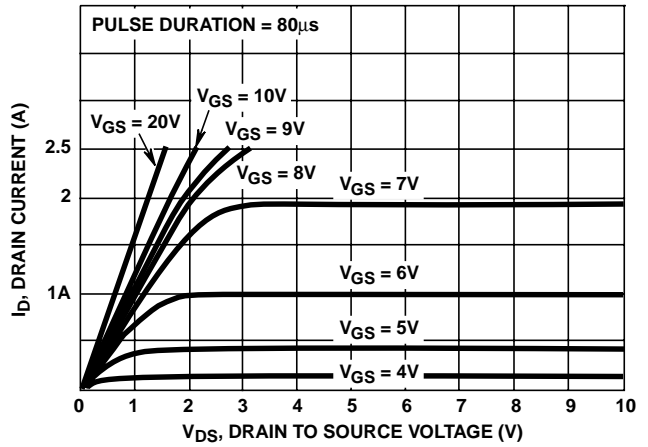


FIGURE 4. SATURATION CHARACTERISTICS

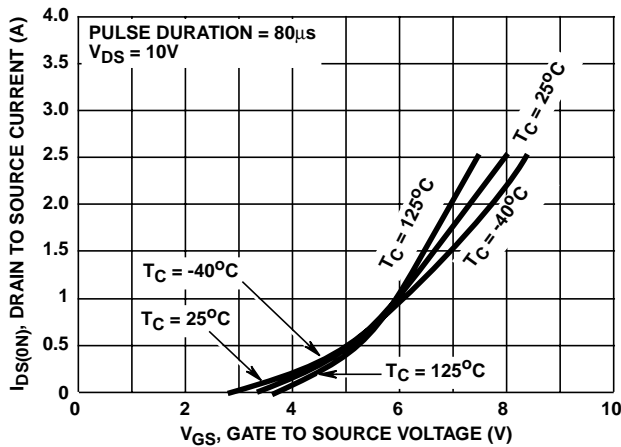


FIGURE 5. TRANSFER CHARACTERISTICS

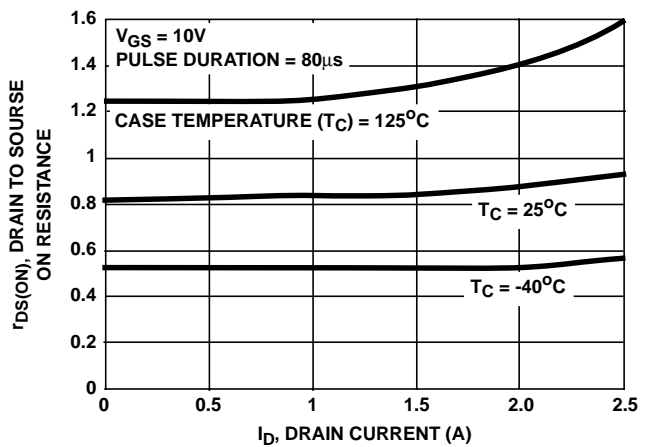


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

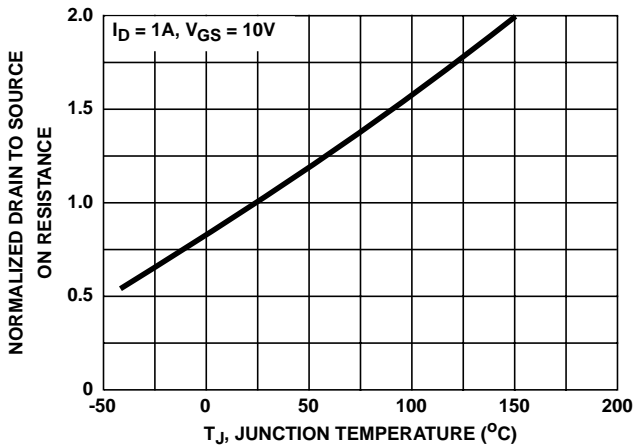


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

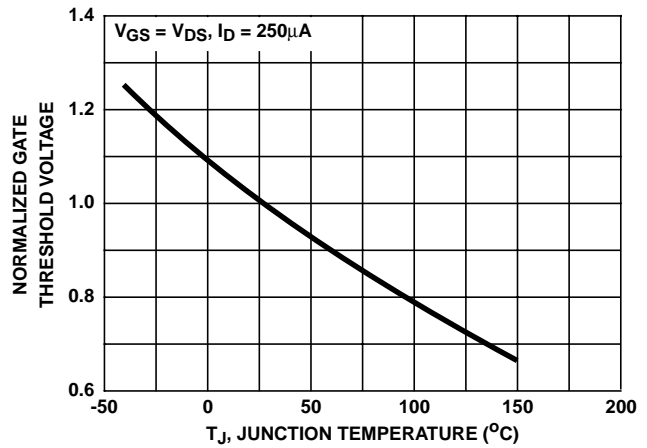


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

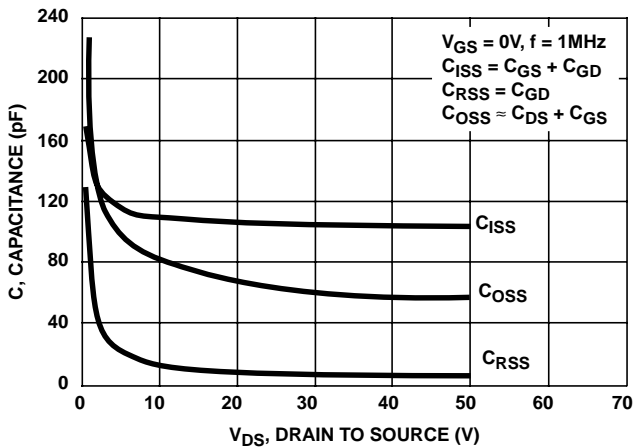
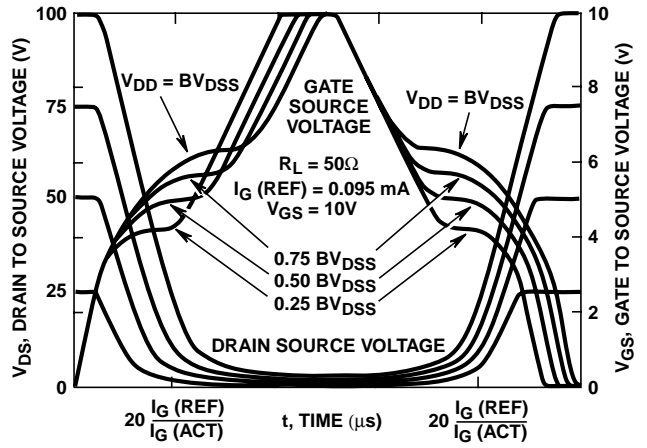


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Harris Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

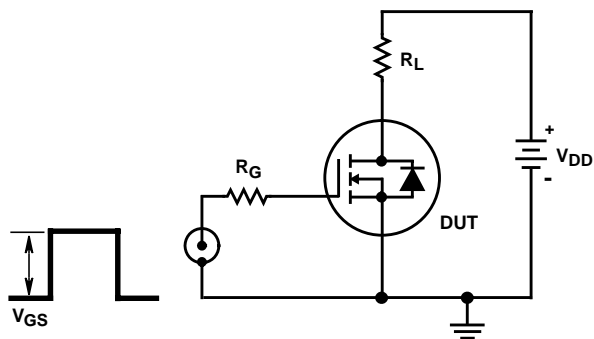


FIGURE 11. SWITCHING TIME TEST CIRCUIT

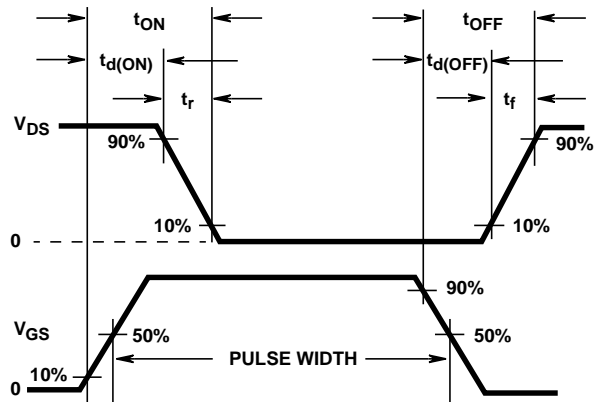


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS