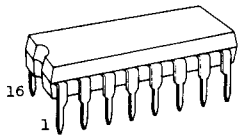
TC5050P

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5050P DUAL 50/64 STAGE STATIC SHIFT REGISTER

TC5050P is static shift register consisting of D type flip-flops, and can be used as either 50 bit shift register or 64 bit shift register depending on OUTPUT MODE input.
Since one of two input data can be selected by INPUT MODE input, the applications for scratch pad memories, etc. can be realized by connecting one of data inputs to the output. And if two circuits are connected in series, this can be expanded to 100 bit, 114 bit or 128 bit shift register.
When used with 5 volts power supply, one of TTL or DTL can be directly driven.

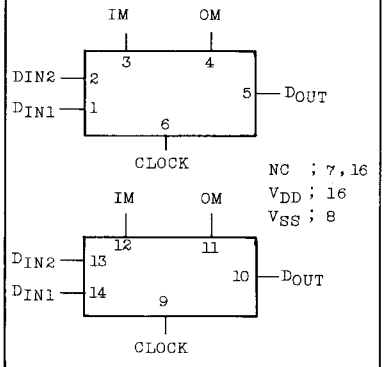


DIP 16 (3D16A-P)

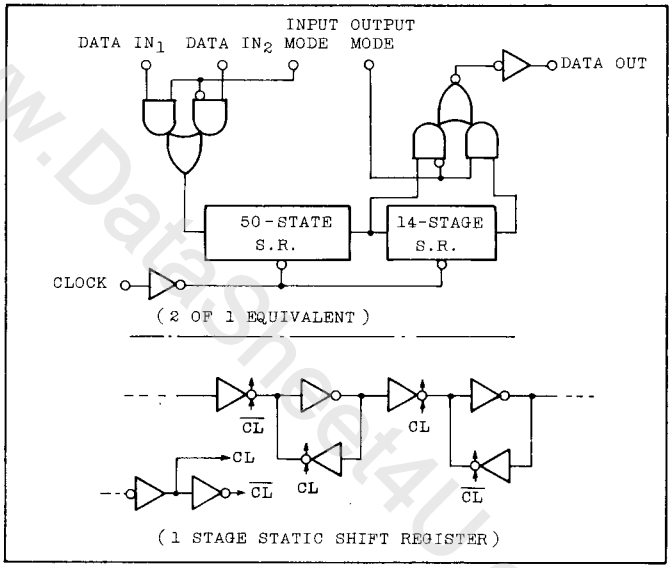
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Storage Temperature Range	T_{stg}	-55 ~ 125	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



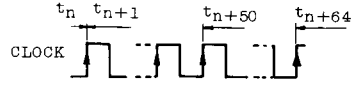
LOGIC DIAGRAM



TRUTH TABLE

t_n, t_{n+1}			t_{n+50}		t_{n+64}	
D_{IN1}	D_{IN2}	IM	OM	D_{OUT}	OM	D_{OUT}
H	*	H	L	H	H	H
L	*	H	L	L	H	L
*	H	L	L	H	H	H
*	L	L	L	L	H	L

* Don't Care



RECOMMENDED OPERATING CONDITIONS (V_{SS}=OV)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3	-	8	V
Input Voltage	V_{IN}		0	-	V_{DD}	V
Operating Temperature	Topr		-30	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=OV)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-30°C MIN.	-30°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	4.95	-	4.95	5.00	-	4.95	-	V
Low Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{DD},V_{SS}$	5	-	0.05	-	0.00	0.05	-	0.05	
High Level Output Current	I_{OH}	V_{OH}=2.5V $V_{IN}=V_{DD},V_{SS}$	5	-1.25	-	-1.25	-5.0	-	-1.0	-	mA
Low Level Output Current	I_{OL}	V_{OL}=0.4V $V_{IN}=V_{DD},V_{SS}$	5	3.2	-	3.2	7.0	-	2.4	-	
High Level Input Voltage	V_{IH}	V_{OUT}=0.5V,4.5V $\|I_{OUT}\|<1\mu A$	5	3.5	-	3.5	2.75	-	3.5	-	V
Low Level Input Voltage	V_{IL}	V_{OUT}=0.5V,4.5V $\|I_{OUT}\|<1\mu A$	5	-	1.5	-	2.25	1.5	-	1.5	
H.Level Input Current	I_{IH}	V_{IH}=8V	8	-	0.2	-	10^{-5}	0.2	-	1.0	μA
L.Level Input Current	I_{IL}	V_{IL}=0V	8	-	-0.2	-	-10^{-5}	-0.2	-	-1.0	μA
Quiescent Current C.	I_{DD}	*V_{IN}=VSS,V_{DD}	5	-	50	-		50	-	375	μA

* All valid input combination

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=OV, C_L=50pF)

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{TLH}		5	-	135	400	ns
Output Fall Time		t_{THL}		5	-	100	200	ns
(Low-High)P.Delay Time		t_{pLH}		5	-	500	1000	ns
(High-Low)P.Delay Time		t_{pHL}		5	-	400	1000	
Max.Clock Rise Time		t_{rCL}		5	20	-	-	μs
Max.Clock Fall Time		t_{fCL}						
Max. Clock Frequency		f_{CL}		5	1.0	2.5	-	MHz
Data Set Up Time		t_{SU}		5	-	100	250	ns
Data Hold Time		t_H		5	-	-100	50	ns
InputCapacitance	CLOCK INPUT	C_{IN}			-	10	15	pF
	OTHER INPUT				-	5	7.5	

SWITCHING TIME TEST WAVEFORM