

FEATURES

- 21.3 dB Gain
- Very Low Distortion
- Excellent 75 Ω Input and Output Match
- Stable with High VSWR Load Conditions
- Monolithic Design for Consistent Performance Part-to-Part
- Low DC Power Consumption
- Surface Mount Package Compatible with Automatic Assembly
- Low Cost Alternative to Hybrids
- Meets Cenelec Standards

APPLICATIONS

- CATV Line Amplifiers, System Amplifiers, Distribution Nodes



PRODUCT DESCRIPTION

The ACA2407E is a highly linear, monolithic GaAs RF amplifier that has been developed to replace, in new designs, standard CATV hybrid amplifiers. Offered in a convenient surface mount package, the MMIC consists of two pairs of parallel amplifiers that are optimized for exceptionally low distortion and

noise figure. A hybrid equivalent that provides flat gain response and excellent input and output return loss over the 40 to 870 MHz CATV downstream band is formed when one ACA2407E is cascaded between two appropriate transmission line baluns.

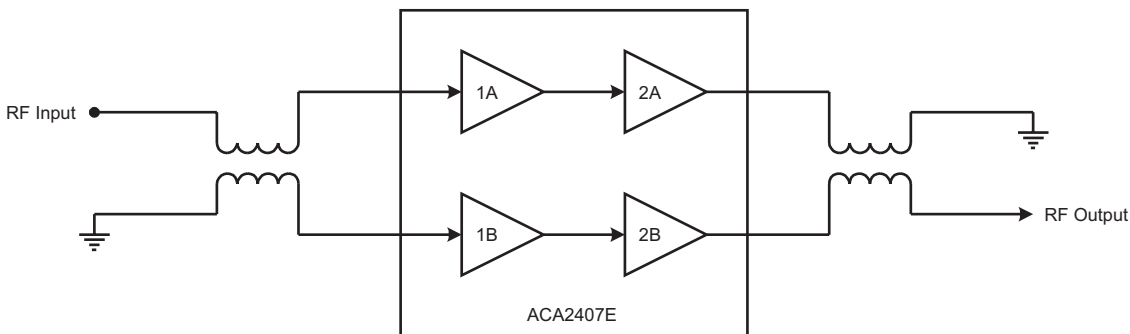


Figure 1: Hybrid Application Diagram

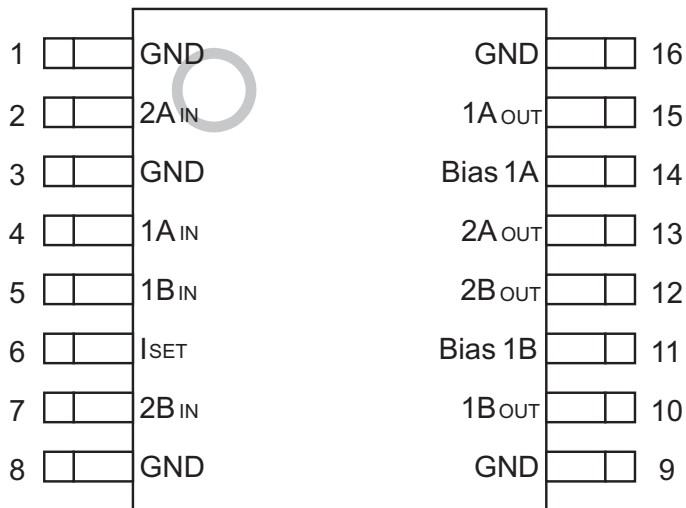


Figure 2: Pin Out

Table 1: Pin Description

| PIN | NAME | DESCRIPTION | PIN | NAME | DESCRIPTION |
|-----|------------------|--------------------|-----|-------------------|--------------------------------|
| 1 | GND | Ground | 9 | GND | Ground |
| 2 | 2A _{IN} | Amplifier 2A Input | 10 | 1B _{OUT} | Amplifier 1B Output |
| 3 | GND | Ground | 11 | Bias 1B | Bias for 1B Amplifier |
| 4 | 1A _{IN} | Amplifier 1A Input | 12 | 2B _{OUT} | Amplifier 2B Output and Supply |
| 5 | 1B _{IN} | Amplifier 1B Input | 13 | 2A _{OUT} | Amplifier 2A Output and Supply |
| 6 | I _{SET} | Current Adjust | 14 | Bias 1A | Bias for 1A Amplifier |
| 7 | 2B _{IN} | Amplifier 2B Input | 15 | 1A _{OUT} | Amplifier 1A Output |
| 8 | GND | Ground | 16 | GND | Ground |

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Mimimum and Maximum Ratings

| PARAMETER | MIN | MAX | UNIT |
|--------------------------------|-----|------|------|
| Supply (pins 12, 13) | 0 | +28 | VDC |
| RF Power at Inputs (pins 4, 5) | - | +75 | dBmV |
| Storage Temperature | -65 | +150 | °C |
| Soldering Temperature | - | +260 | °C |
| Soldering Time | - | 5.0 | Sec |

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Notes:

1. Pins 2, 4, 5 and 7 should be AC-coupled. No external DC bias should be applied.
2. Pin 6 should be AC-grounded and/or pulled to ground through a resistor for current control.
3. Pins 11 and 14 are bias feeds for input amplifiers 1A and 1B. No external DC bias should be applied.
4. Pins 10 and 15 receive DC bias directly from pins 11 and 14.

Table 3: Operating Ranges

| PARAMETER | MIN | TYP | MAX | UNIT |
|---------------------------------------|-----|-----|------|------|
| Supply: V _{DD} (pins 12, 13) | - | +24 | - | VDC |
| Voltage at I _{SET} (pin 6) | - | +3 | - | VDC |
| RF Frequency | 40 | - | 870 | MHz |
| Case Temperature | -40 | - | +110 | °C |

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

Table 4: Electrical Specifications
(T_A = +25 °C, V_{DD} = +24 VDC)

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|----------------------------------------------------------------------------------|-------------|------------|----------|------|------------------------------------------|
| Gain ⁽¹⁾ | 20.4 | 21.3 | 22.4 | dB | |
| Cable Equivalent Slope ⁽¹⁾ | - | 0 | - | dB | |
| Gain Flatness ⁽¹⁾ to 750 MHz | - | ± 0.2 | - | dB | |
| Noise Figure ⁽¹⁾ | - | 4.0 | 4.5 | dB | |
| CTB ⁽¹⁾ 77 Channels ⁽²⁾ 110 Channels ⁽³⁾ | - - - | -70 -65 | -66 - | dBc | |
| CSO ⁽¹⁾ 77 Channels ⁽²⁾ 110 Channels ⁽³⁾ | - - - | -66 -60 | -64 - | dBc | |
| XMOD ⁽¹⁾ 77 Channels ⁽²⁾ 110 Channels ⁽³⁾ | - - - | -62 -60 | -60 - | dBc | |
| Return Loss (Input/Output) ⁽¹⁾ | 18 | 22 | - | dB | 75 Ω system |
| Supply Current (I _{DD}) | 410 | 425 | 440 | mA | R1 = 75 kΩ, R3 open Refer to Figure 8 |
| Thermal Resistance | - | 3.1 | 3.8 | °C/W | |
| I _{DD} Adjust | - | <1 | - | mA | Refer to Figure 8 |

Notes:

(1) Measured with baluns on the input and output of the device.

(2) Parts measured with 77 channels, +56 dBm V power, 13.5 dB tilt at 870 MHz.

(3) Parts measured with 110 channels, +52 dBm V power, 13.5 dB tilt at 870 MHz.

4. All specifications as measured on Evaluation Board (see Figures 7 & 8).

Table 5: Electrical Specifications at Reduced I_{DD}
(T_A = +25 °C, V_{DD} = +24 VDC)

| PARAMETER | TYP | TYP | UNIT | COMMENTS |
|---------------------------------------------------|------|------|------|----------|
| Gain | 21.0 | 21.2 | dB | |
| CTB ⁽¹⁾ 77 Channels ⁽²⁾ | -58 | -64 | dBc | |
| CSO ⁽¹⁾ 77 Channels ⁽²⁾ | -60 | -62 | dBc | |
| XMOD ⁽¹⁾ 77 Channels ⁽²⁾ | -50 | -55 | dBc | |
| Supply Current (I _{DD}) | 360 | 390 | mA | |
| R1 (Figure 8) | Open | Open | Ω | |
| R3 (Figure 8) | 10 k | Open | Ω | |

Notes:

(1) Measured with baluns on the input and output of the device.

(2) Parts measured with 77 channels, +56 dBm V power, 13.5 dB tilt at 870 MHz.

PERFORMANCE DATA

Figure 3: Noise Figure vs. Frequency

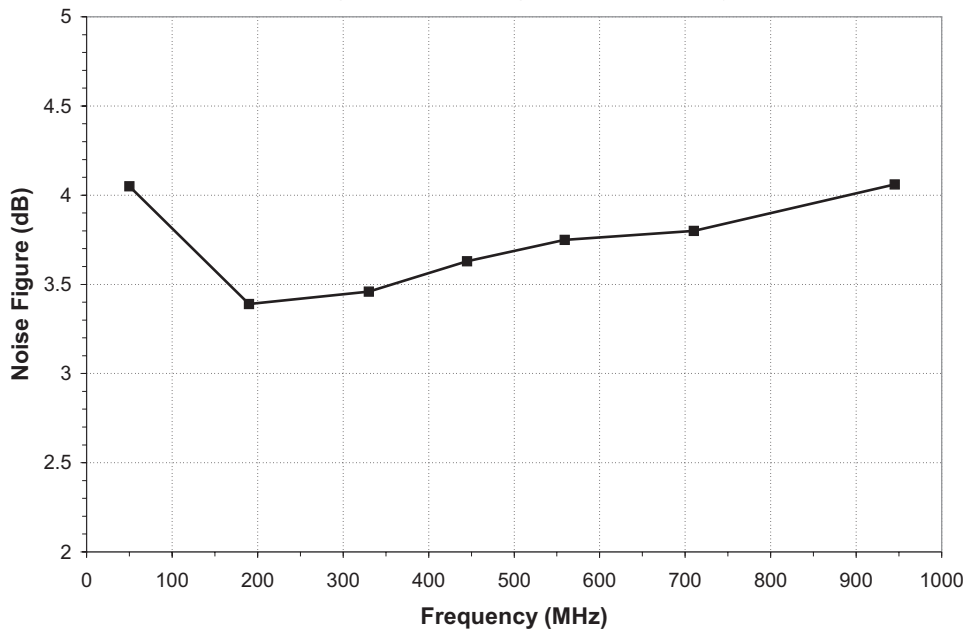


Figure 4: Gain (S21) vs. Frequency

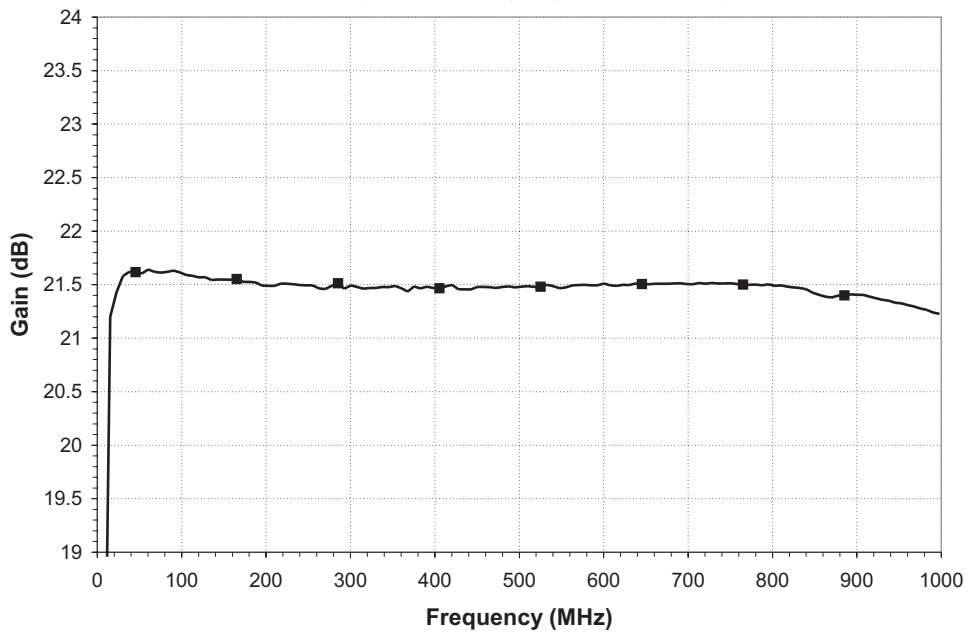


Figure 5: Input and Output Return Loss (S11 and S22) vs. Frequency

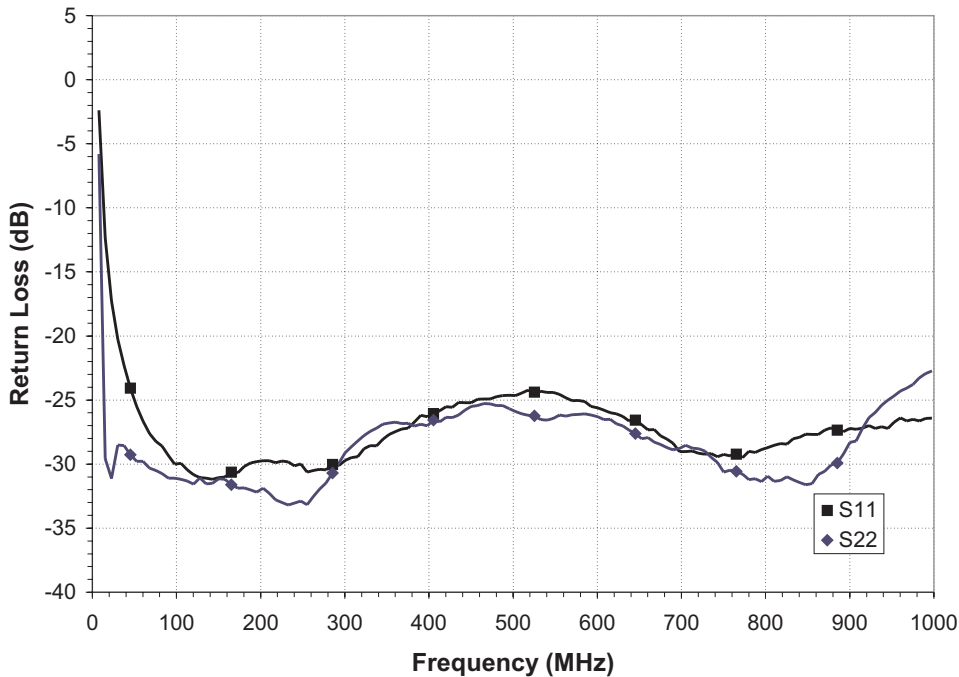
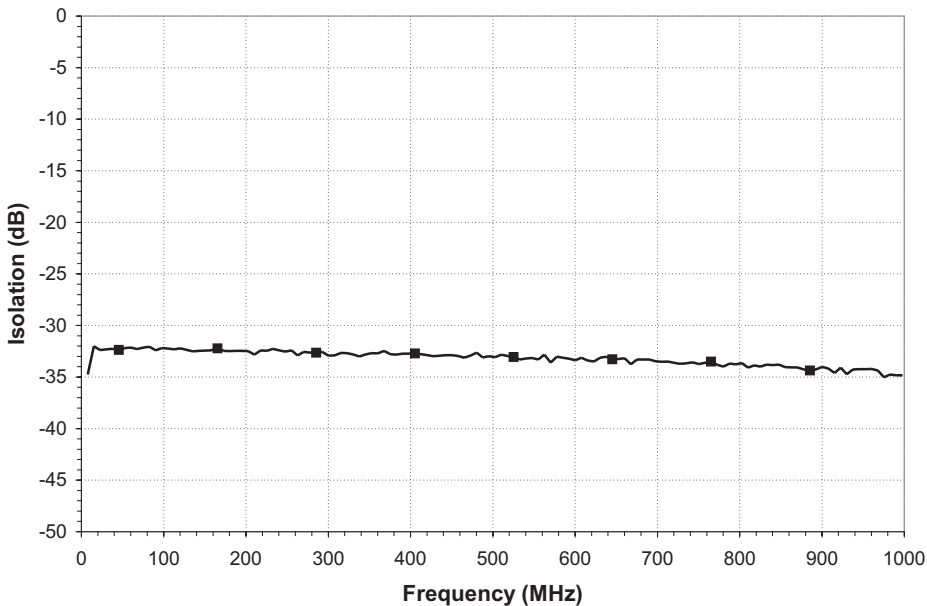


Figure 6: Isolation (S12) vs. Frequency



APPLICATION INFORMATION

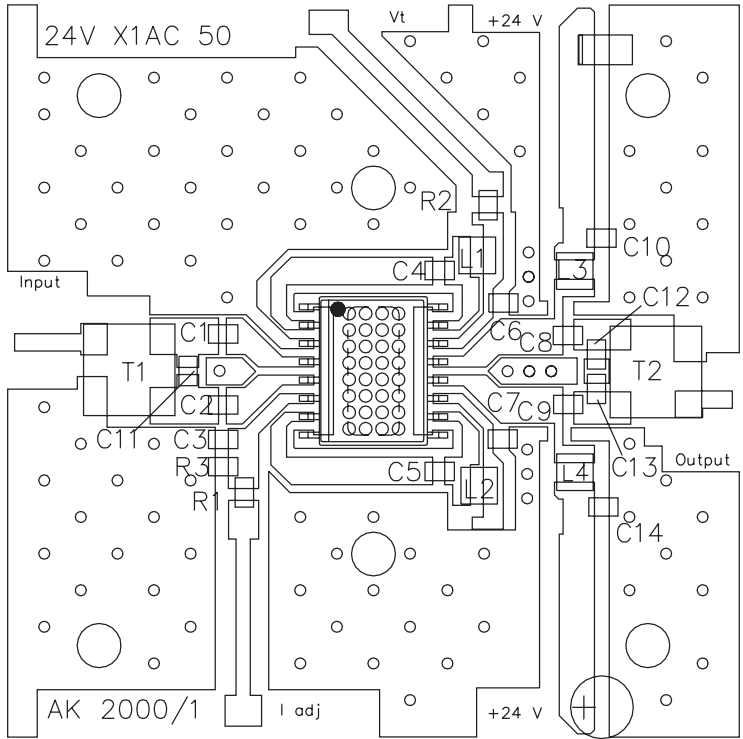


Figure 7: Evaluation Board Layout

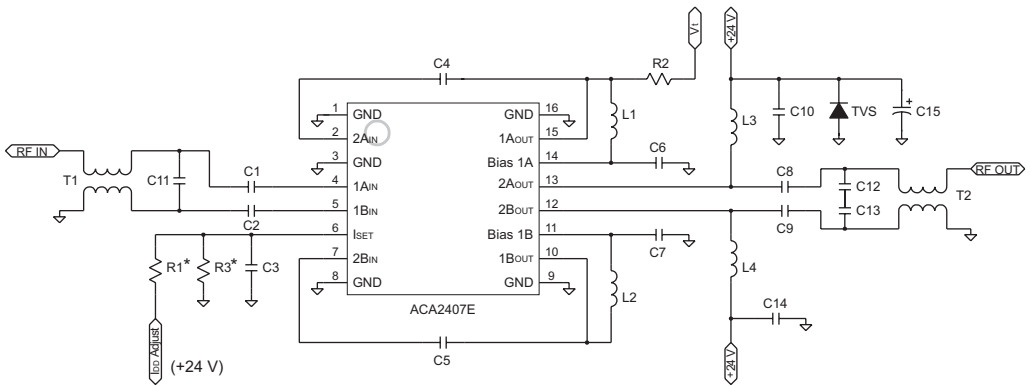


Figure 8: Evaluation Board Schematic

* Refer to Table 5 for R1, R3 use at lower I_{DD} operation.

Table 6: Evaluation Board Parts List

| REF | DESCRIPTION | QTY | VENDOR | VENDOR P/N |
|----------------------------------|--------------------------------------|-----|----------------------------|-----------------|
| C1, C2, C3, C6, C7, C10, C14 | 0.01 μ F Chip Cap | 7 | MURATA | GRM39X7R103K50V |
| C4, C5, C8, C9 | 470 pF Chip Cap | 4 | MURATA | GRM39X7R471K50V |
| C11 | 0.5 pF Chip Cap | 1 | MURATA | GRM36COG0R5C50 |
| C15 | 47 μ F Elect. Cap | 1 | DIG-KEY CORP | P5275-ND |
| C12, C13, R2 | Not Used | | | |
| TVS | TVS 24 Volt 600 Watt | 1 | DIG-KEY CORP | SMBJ24ACCCT-ND |
| L1, L2, L3, L4 ⁽⁴⁾ | 680 nH Inductor | 4 | COILCRAFT | 1008CS-681XKBC |
| R1 ⁽⁵⁾ | 75 k Ω Resistor | 1 | DIG-KEY CORP | P75KGCT-ND |
| R3 ⁽⁵⁾ | 10 k Ω Resistor | 1 | DIG-KEY CORP | P10KGCT-ND |
| CONNECTOR ⁽¹⁾ | 75 Ω N Male Panel Mount | 2 | PASTERNAK ENTERPRISES | PE4504 |
| T1, T2 ⁽²⁾ (BALUN) | Ferrite Core | 2 | FAIR-RITE | 2843002702 |
| | Wire | | MWS WIRE IND. | T-2361429-20 |
| | Printed Circuit Board ⁽³⁾ | 1 | STANDARD PRINTED CIRC. INC | 24VX1AC50 |
| INDIUM | 300 X 160 Mils | 1 | INDIUM CORP OF AMERICA | 14996Y |

Notes:

- (1) N connector center pin should be approximately 80 mils in length.
(2) T1, T2 balun: 6.5 turns thru, as shown in Figure 9.
(3) Due to the power dissipation of this device, the printed circuit board should be mounted / attached to a heat sink.
(4) 400 mA minimum current rating.
(5) Refer to Table 5 for R1, R3 use at lower I_{DD} operation.

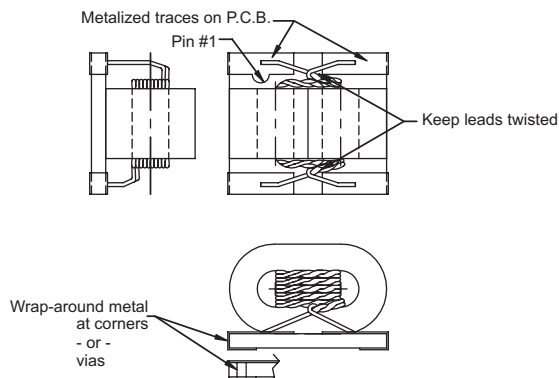
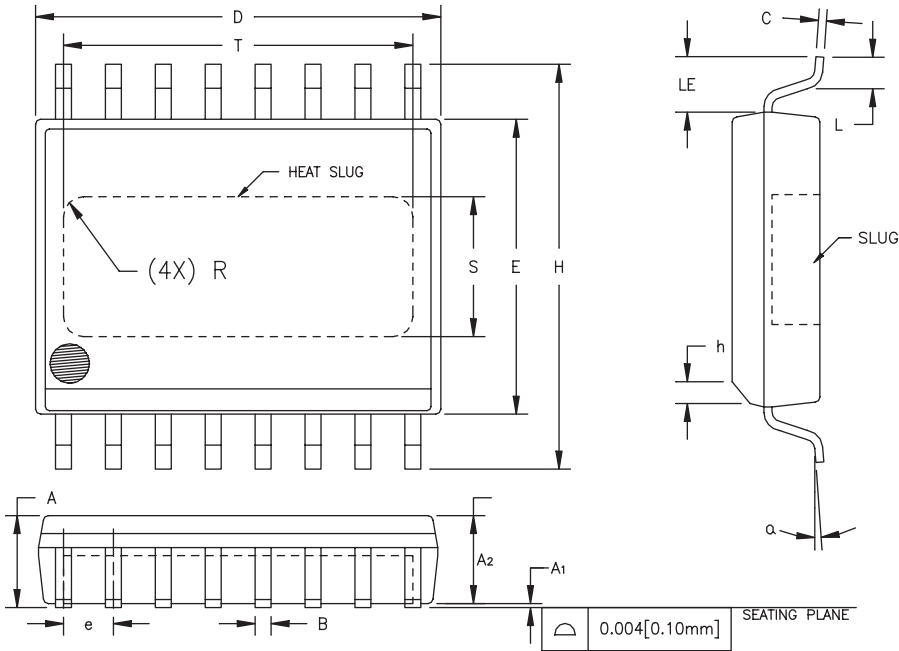


Figure 9: Balun Drawing

PACKAGE OUTLINE



| S _M , B _{OL} | INCHES | | MILLIMETERS | | NOTE |
|----------------------------------|------------|-------|-------------|-------|------|
| | MIN. | MAX. | MIN. | MAX. | |
| A | 0.087 | 0.098 | 2.21 | 2.49 | |
| A ₁ | 0.000 | 0.004 | 0.00 | 0.10 | 6 |
| A ₂ | 0.087 | 0.094 | 2.21 | 2.39 | |
| B | 0.013 | 0.019 | 0.33 | 0.48 | |
| C | 0.007 | 0.009 | 0.18 | 0.23 | |
| D | 0.398 | 0.412 | 10.11 | 10.46 | 2 |
| E | 0.290 | 0.300 | 7.37 | 7.62 | 3 |
| e | 0.050 BSC | | 1.27 BSC | | 4 |
| H | 0.394 | 0.418 | 10.01 | 10.62 | |
| h | 0.010 | 0.028 | 0.25 | 0.71 | |
| L | 0.024 | 0.040 | 0.61 | 1.02 | |
| LE | 0.052 | — | 1.32 | — | |
| α | 0° | 8° | 0° | 8° | |
| S | 0.120 | 0.140 | 3.05 | 3.56 | 5 |
| T | 0.330 | 0.350 | 8.38 | 8.89 | 5 |
| R | REF. 0.015 | | REF. 0.38 | | 5 |

NOTES:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE ±0.005 [0.13mm].
5. DIMENSIONS "S", "T" AND "R" INDICATE EXPOSED SLUG AREA.
6. STANDOFF HEIGHT (A₁) MEASURED FROM BOTTOM OF SLUG.

Figure 10: S7 Package Outline - 16 Pin Wide Body SOIC with Heat Slug

NOTES

ORDERING INFORMATION

| ORDER NUMBER | TEMPERATURE RANGE | PACKAGE DESCRIPTION | COMPONENT PACKAGING |
|--------------|-------------------|--------------------------------------|-------------------------------------|
| ACA2407ES7P2 | -40 °C to +110 °C | 16 Pin Wide Body SOIC with Heat Slug | Tape and Reel, 1500 pieces per Reel |
| ACA2407ES7P0 | -40 °C to +110 °C | 16 Pin Wide Body SOIC with Heat Slug | Plastic Tubes, 25 pieces per Tube |

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