Ultra-Low Voltage MiniGate™ Devices Solve 1.2 V Interface Problems

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APPLICATION NOTE

Many integrated circuits such as microprocessors and DSPs need to operate at very low voltage in order to conserve power and not over dissipate. Issues arise when the designer has a device, like a DSP, operating at 1.2 V and needs to interface with other semiconductors operating at 3.3 V or more.

When performing the interface between a 3.3 V (or any voltage between 1.2 V and 3.3 V) the one single answer that solves all problems, simply with a minimum of board space, is the NL17SVyyyXV5T2 family. With the six available devices, the signal can be applied to the input and brought to the DSP in the fastest possible time (minimum delay), while occupying minimum board space and consuming minimum power.

The designer might ask why not simply use resistors to perform voltage division? Resistors can certainly be used for some applications but they consume power and limit the operating frequency and create a delay (when the designer includes the C of the input device). Figure 1 illustrates the use of two resistors to limit the voltage on the DSP. For simplicity, this article will not take into account tolerance issues. That will be left to the reader if he chooses this approach. In all cases, we will use V_1 = 3.3 V, V_2 = 1.2 V, f = 35 MHz, and C_{IN} = 10 pf. If 640 Ω and 330 Ω resistors are used, the circuit will perform the required voltage division. The loading will be 330 Ω and draw 1.0 mA when the device is on. If it is assumed to be a 50% duty cycle, then the power consumption for the simple resistor divider will be 16 mW. This power consumption is so high that it would be ruled out immediately. If we would have used larger value resistors, the frequency response would be impaired and 35 MHz would be impossible. The delay time through this circuit will be about 15 to 20 ns.

A second possible scheme might be to use a transistor. If an NPN transistor were used, it would need a voltage division scheme similar to Figure 1 and the values would need to be the same in order to keep the frequency response to > 50 MHz f_{3dB}. Power dissipation would be actually higher than for the passive case because we would have a third resistor from 1.2 V to the collector (Figure 2). We would have another 5.0 mW of power dissipation due to the output resistor. This solution would consume > 20 mW of power and again is outrageously high in the power budget. In addition, the manufacturer would have to place three parts (three resistors and one transistor or one BRT plus one resistor). Delay time would be longer than the passive solution above, hence more costly and would present absolutely no advantage over the simple resistive divider.

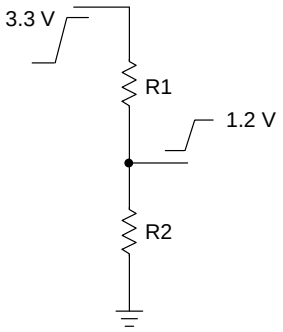


Figure 1.

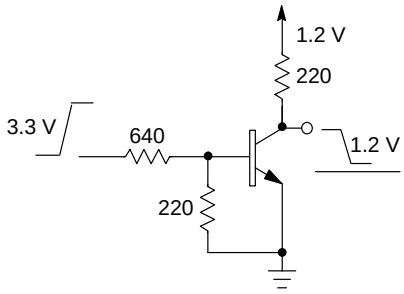
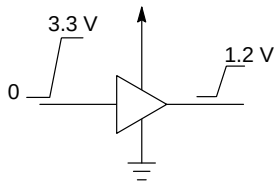


Figure 2.

It should be noticed that the signal is inverted for the case of the transistor. This may or may not be desirable. In fact, the phase inversion would be the only plausible reason to prefer the transistor case over the passive resistor divider. The last option that will be presented will be the ON Semiconductor sub−one volt family, NL17SVxx products. We have the choice of inverted or non−inverted output. Since the devices are Over−Voltage Tolerant (OVT) at their inputs, the designer may simply apply the 3.3 V signal to the input of the device. For this application, Figure 3 shows the supply voltage to the device will be 1.2 V. This assures that the output will be logic level compatible with the device that it is driving.



NL17SV16XV5T2

Figure 3.

Since the 3.3 V logic is only driving a capacitive input, there is very little power dissipation at the input. To calculate the total power consumed, we must use a different equation that depends on the Power Dissipation Capacitance (C_{PD}) as the main factor. To calculate the power loss in the gate, the following formula is used:

$$PD = (C_{PD} \cdot V_{CC}^2 \cdot f) + (I_{CC} \cdot V_{CC})$$

At 35 MHz and C_{PD} of 20 pf, the equation works out to ~ 2.0 mW total power, with about 50% of the power consumed in leakage current and 50% in the switching. The delay time is only 10 ns (worst case), at V_{CC} of 1.2 V.

Conclusion

The use of a single gate for logic level translation saves 90% of the power required for a passive solution and even more compared to a transistor solution. The manufacturer needs only to place one part versus two or more for any other approach. The time delay is much faster and less circuit dependent. Output may be either inverted or non−inverted (by selecting appropriate single gate device). The circuit will easily operate past 50 MHz, if needed at 1.2 V. It is clear that this is the only practical solution for logic level translation at low power.

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