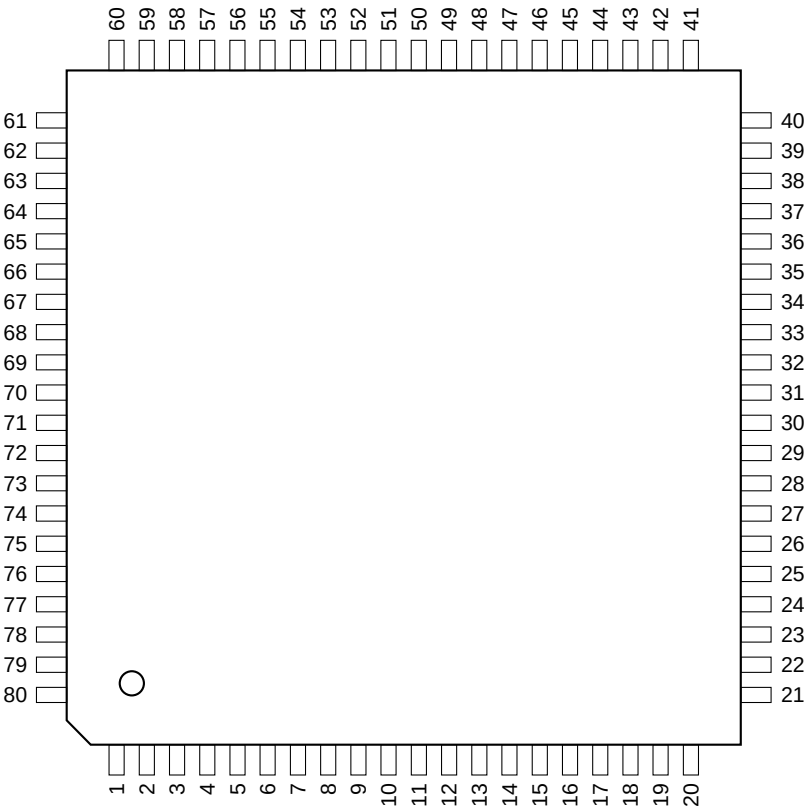
SIGNAL PROCESSOR FOR CCD COLOR CAMERAS

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	TEST18	21	—	GND	41	—	VCC	61	—	VCC
2	I	TEST19	22	O	DOC7	42	O	MCKO	62	I	MCKI32
3	I	TEST0	23	O	DOC6	43	O	MCKO14	63	O	FRO
4	I	INVI	24	O	DOC5	44	O	MFRO	64	O	HRO
5	O	INVO	25	O	DOC4	45	O	MHRO	65	O	$\overline{\text{CLPOB}}$
6	—	GND	26	O	DOC3	46	O	MWEO	66	I	WEI
7	I	TEST20	27	O	DOC2	47	O	MCKO32	67	I	MCKI
8	I	$\overline{\text{CLR}}$	28	O	DOC1	48	O	CDIS	68	I	DOCNT
9	I	$\overline{\text{CE}}$	29	O	DOC0	49	—	GND	69	—	GND
10	I	SCK	30	—	VCC	50	O	TEST7	70	I	AD9
11	I	SI	31	O	DOY7	51	O	TEST8	71	I	AD8
12	O	SO	32	O	DOY6	52	O	TEST9	72	I	AD7
13	O	TEST21	33	O	DOY5	53	I	TEST10	73	I	AD6
14	—	VCC	34	O	DOY4	54	I	TEST11	74	I	AD5
15	O	TEST1	35	O	DOY3	55	I	TEST12	75	I	AD4
16	O	TEST2	36	O	DOY2	56	I	TEST13	76	I	AD3
17	O	TEST3	37	O	DOY1	57	I	TEST14	77	I	AD2
18	I	TEST4	38	O	DOY0	58	I	TEST15	78	I	AD1
19	I	TEST5	39	—	GND	59	I	TEST16	79	I	AD0
20	—	TEST6	40	I	TSTON	60	I	TEST17	80	—	VCC

INPUTS

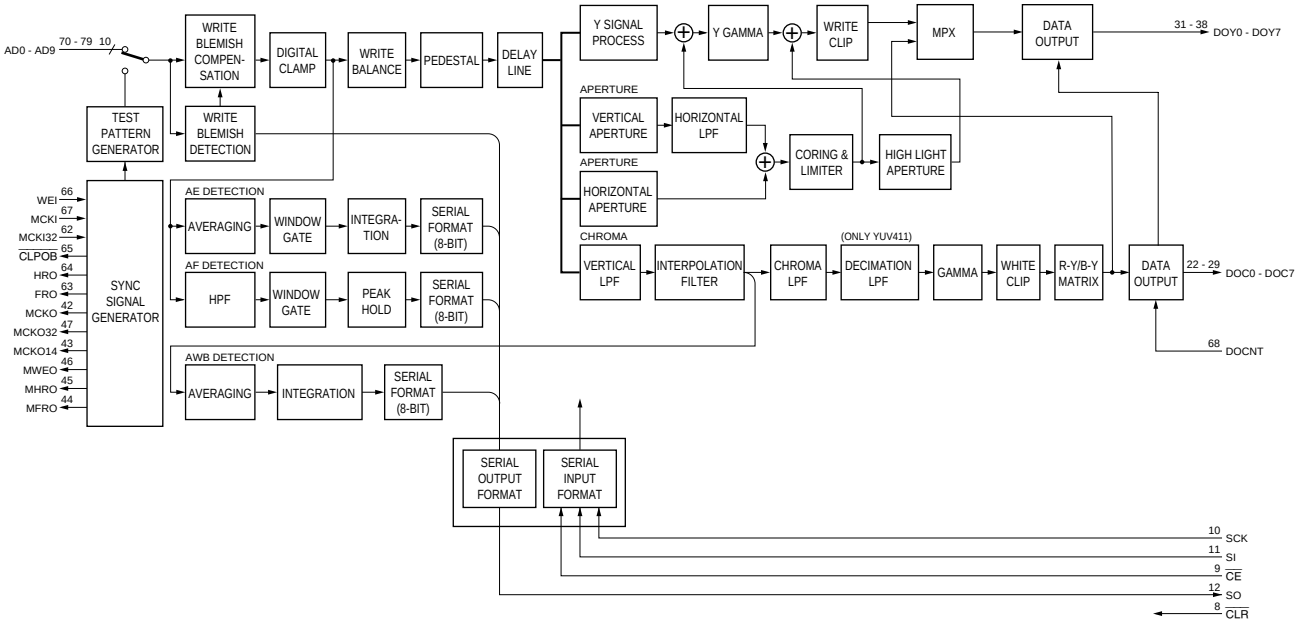
AD0 - AD9	:	DIGITAL SIGNAL DATA
$\overline{CE}$	:	CHIP SELECT
$\overline{CLR}$	:	INITIALIZE
DOCNT	:	TRI-STATE CONTROL
INVI	:	INVERTER
MCKI	:	SYSTEM MAIN CLOCK
MCKI32	:	3/2 MCKI
SCK	:	SERIAL CLOCK
SI	:	SERIAL DATA
WEI	:	WRITE ENABLE

OUTPUTS

$\overline{CDIS}$	:	Cr/Cb LINE IDENTIFICATION TIMING
$\overline{CLPOB}$	:	CLAMP PULSE
DOC0 - DOC7	:	DIGITAL CHROMA
DOY0 - DOY7	:	DIGITAL Y
FRO	:	V SYNC FOR CCD TIMING GENERATOR
HRO	:	H SYNC FOR CCD TIMING GENERATOR
INVO	:	INVERTER
MCKO	:	SYSTEM MAIN CLOCK
MCKO14	:	1/4 MCKO
MCKO32	:	3/2 MCKO
MFRO	:	V SYNC
MHRO	:	H SYNC
MWEO	:	WRITE ENABLE
SO	:	SERIAL DATA
TEST1 - TEST3, TEST21	:	(FOR TEST)
TEST7 - TEST9	:	OPEN

OTHERS

TEST0 - TEST21	:	(FOR TEST)
TSTON	:	(FOR TEST)


AD0 - AD9
70 - 79 10
WRITE BLEMISH COMPEN-SATION
DIGITAL CLAMP
WRITE BALANCE
PEDESTAL
DELAY LINE
Y SIGNAL PROCESS
Y GAMMA
WRITE CLIP
MPX
DATA OUTPUT
31 - 38
DOY0 - DOY7
TEST PATTERN GENERATOR
WRITE BLEMISH DETECTION
APERTURE
VERTICAL APERTURE
HORIZONTAL LPF
APERTURE
HORIZONTAL APERTURE
CORING & LIMITER
HIGH LIGHT APERTURE
WEI 66
MCKI 67
MCKI32 52
CLPOB 65
HRO 64
FRO 63
MCKO 42
MCKO32 47
MCKO14 43
MWEO 46
MHRO 45
MFRO 44
SYNC SIGNAL GENERATOR
AE DETECTION
AVERAGING
WINDOW GATE
INTEGRA-TION
SERIAL FORMAT (8-BIT)
AF DETECTION
HPF
WINDOW GATE
PEAK HOLD
SERIAL FORMAT (8-BIT)
AWB DETECTION
AVERAGING
INTEGRATION
SERIAL FORMAT (8-BIT)
CHROMA
VERTICAL LPF
INTERPOLATION FILTER
CHROMA LPF
(ONLY YUV411)
DECIMATION LPF
GAMMA
WHITE CLIP
R-Y/B-Y MATRIX
DATA OUTPUT
22 - 29
DOC0 - DOC7
68
DOCNT
SERIAL OUTPUT FORMAT
SERIAL INPUT FORMAT
10
SCK
11
SI
9
CE
12
SO
8
CLR