*Multi*GEN™ GF9105A
Component Digital Transcoder

DATA SHEET

FEATURES

- **drop in replacement for the GF9105 with lower power and increased functionality**
- **new mode for HVF output**
- **new mode for using low frequency clocks with non-multiplexed I/O data**
- **optimized HOST IF control signals for ensured shared bus compatibility**
- **multiple format conversions from one device**
  - **4:2:2:4 <-> 4:4:4:4**
  - **4:2:2:4 <-> R/G/B/KEY**
  - **4:2:2:4 <-> Y/U/V/KEY**
  - **Y/U/V/KEY <-> R/G/B/KEY**
  - **4:4:4:4 <-> R/G/B/KEY**
  - **4:4:4:4 <-> Y/U/V/KEY**
- **ITU-R-601 compliant interpolation/decimation filters**
- **supports both single link 4:4:4:4 (SMPTE RP174) and dual link 4:4:4:4 (SMPTE RP175) compliant I/O**
- **transparent conversions between Y/U/V and R/G/B color spaces.**
- **fully programmable 3X3 Color Space Converter (CSC)**
- **13 bit Color Space Converter coefficients**
- **13 bit KEY Channel scaling coefficient**
- **multiplexed and non-multiplexed I/O data**
- **bi-directional I/O data ports with tri-stating**
- **parallel HOST IF for reading and writing multiplier coefficients and device configuration words**
- **single +5V power supply.**

ORDERING INFORMATION

PART NUMBER	PACKAGE
GF9105ACQQ	160 Pin MQFP

DEVICE OVERVIEW

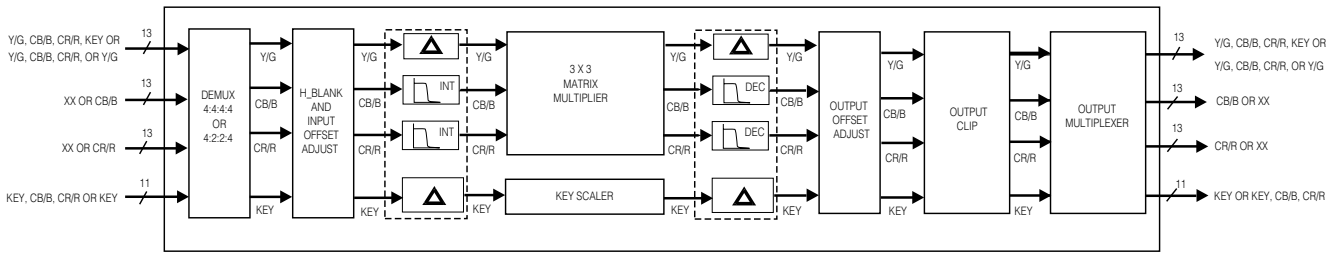
The GF9105A is a drop in replacement for the GF9105 with lower power and increased functionality. This increased functionality gives the user the option of having HVF output signals and the option of using a low frequency clock when operating with non-multiplexed input and output data. The GF9105A is a flexible VDSP engine capable of performing a variety of format conversions. The flexible architecture of the GF9105A also allows the user to perform a wide range of DSP functions that require a general 3X3 multiplier structure and/or high performance 1:2 interpolation and 2:1 decimation filters. Device configuration is selected by writing configuration words through an asynchronous parallel interface (HOST IF).

The GF9105A accepts either multiplexed or non-multiplexed input data and may produce either multiplexed or non-multiplexed output data. External H, V and F inputs allow for the insertion of TRS words into multiplexed output data streams.

All interpolation and decimation filtering required for ITU-R-601 compliant 4:2:2:4 <-> 4:4:4:4 sample rate conversions has been integrated into the GF9105A. In addition, all input and output offset adjustments required for transparent conversions between the Y/U/V and R/G/B color spaces have been included within the GF9105A.

The color space converter within the GF9105A has 13 bit multiplier coefficients, has 13 bit output resolution, maintains full precision throughout the 3X3 calculation and has a true unity gain by-pass mode. Sufficient resolution is maintained within the color space converter to ensure that truly transparent Y/U/V <-> R/G/B conversions may be achieved. A user programmable output clipper allows the GF9105A to output a variety of word lengths to meet specific system requirements.

The GF9105A is packaged in a 160 pin MQFP package, operates from a single +5V supply.



GENERAL FUNCTIONALITY OF GF9105A CORE

Revision Date: March 2000 Document No. 521 - 88 - 03

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PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
11, 20, 51, 60, 80, 101, 121, 141, 150	V_{DD}	+5 V ±5% power supply.
4, 7, 10, 14, 21, 43, 52, 61, 63, 72, 81, 88, 96, 100, 105, 113, 120, 129, 138, 140, 149, 158	GND	Ground.
147, 148, 151-157, 159, 160, 1, 2	$P1_{12..0}$	Data Port No. 1: Depending on device configuration, $P1_{12..0}$ may operate as an input data port or an output data port. Note: When HVF output is enabled H is always presented on $P1_{12}$ regardless of the state of INPUT/$\overline{\text{OUTPUT}}$.
131-137, 139, 142-146	$P2_{12..0}$	Data Port No. 2: Depending on device configuration, $P2_{12..0}$ may operate as an input data port or an output data port. Note: When HVF output is enabled V is always presented on $P2_{12}$ regardless of the state of INPUT/$\overline{\text{OUTPUT}}$.
115-119, 122-128, 130	$P3_{12..0}$	Data Port No. 3: Depending on device configuration, $P3_{12..0}$ may operate as an input data port or an output data port. Note: When HVF output is enabled F is always presented on $P3_{12}$ regardless of the state of INPUT/$\overline{\text{OUTPUT}}$.
102-104, 106-112, 114	$P4_{10..0}$	Data Port No. 4: Depending on device configuration, $P4_{10..0}$ may operate as an input data port or an output data port.
54, 53, 50-44, 42-39	$P5_{12..0}$	Data Port No. 5: Depending on device configuration, $P5_{12..0}$ may operate as an input data port or an output data port.
70-64, 62, 59-55	$P6_{12..0}$	Data Port No. 6: Depending on device configuration, $P6_{12..0}$ may operate as an input data port or an output data port.
86-82, 79-73, 71	$P7_{12..0}$	Data Port No. 7: Depending on device configuration, $P7_{12..0}$ may operate as an input data port or an output data port.
99-97, 95-89, 87	$P8_{10..0}$	Data Port No. 8: Depending on device configuration, $P8_{10..0}$ may operate as an input data port or an output data port.
22	SYNC_CB	Synchronization: Control signal input. SYNC_CB is used to synchronize the GF9105A to the incoming data stream.
24	H_BLANK	Horizontal Blanking: Control signal input. H_BLANK is used to replace portions of the input data with a user selectable set of blanking levels.
25	$\overline{\text{DP\_EN}}$	$\overline{\text{Data Port Enable}}$: Control signal input. $\overline{\text{DP\_EN}}$ is used to enable and disable data ports P1 - P8.
17	H	Horizontal: Control signal input. H identifies the horizontal blanking interval for the output multiplexer.
16	V	Vertical: Control signal input. V identifies the vertical blanking interval for the output multiplexer.
18	F	Field: Control signal input. F is used to identify field information for the output multiplexer.
26	$\overline{\text{CS}}$	$\overline{\text{Chip Select}}$: Host interface control signal input.
23	R/$\overline{\text{W}}$	Read/$\overline{\text{Write}}$: Host interface control signal input.
27-31	$ADDR_{4..0}$	Coefficient Address: Input port to identify which GF9105A device address shall be written to/read from.
3, 5, 6, 8, 9, 12, 13, 15	$COEFF\_PORT_{7..0}$	Coefficient Port: Host interface bi-directional data port for Color Space Converter coefficients, KEY scaler coefficient and device configuration words.
19	CLK	System Clock: All timing information is relative to the rising edge of CLK.
32	TCK	JTAG Test Clock Input: Independent clock signal for JTAG.

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
33	TDI	JTAG Test Data Input: Serial input for JTAG test data.
34	TMS	JTAG Test Mode Select: Serial input for selecting JTAG test mode.
35	$\overline{\text{TRST}}$	$\overline{\text{JTAG Test Reset}}$: Connect to GND for normal operation.
36	TDO	JTAG Test Data Output: Serial output for JTAG test data.
37	TN_IN	Connect to V_{DD}.
38	PTO	No Connect.

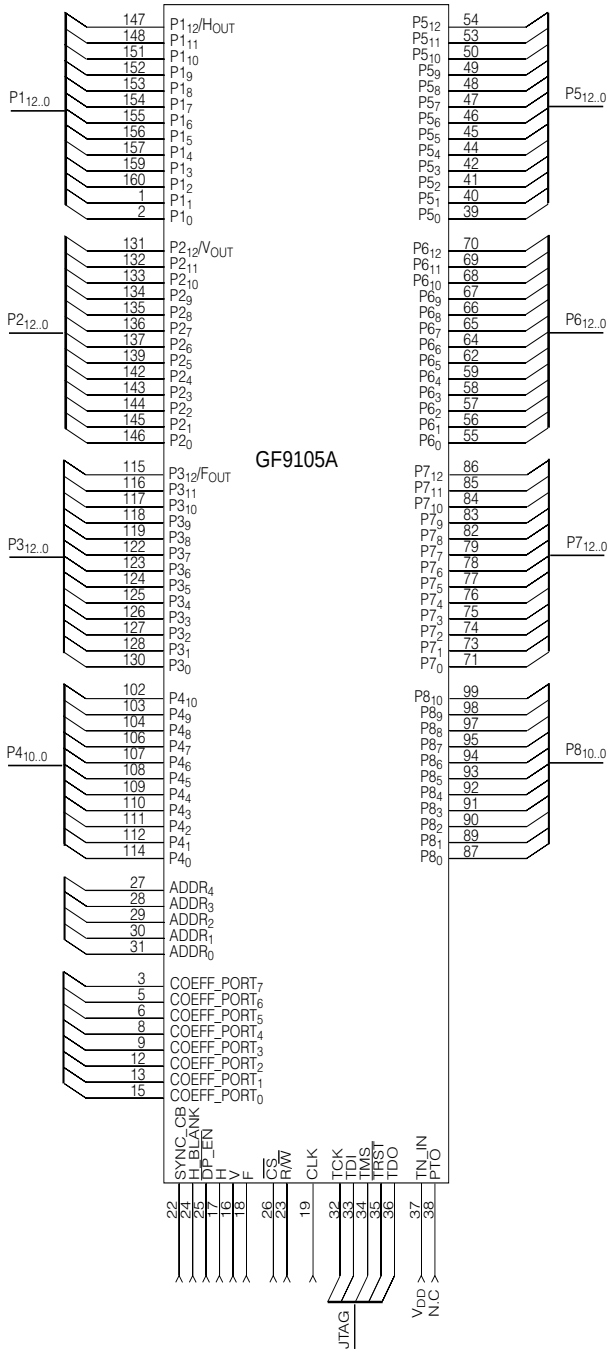


Fig. 1 GF9105A Data Pin Designations

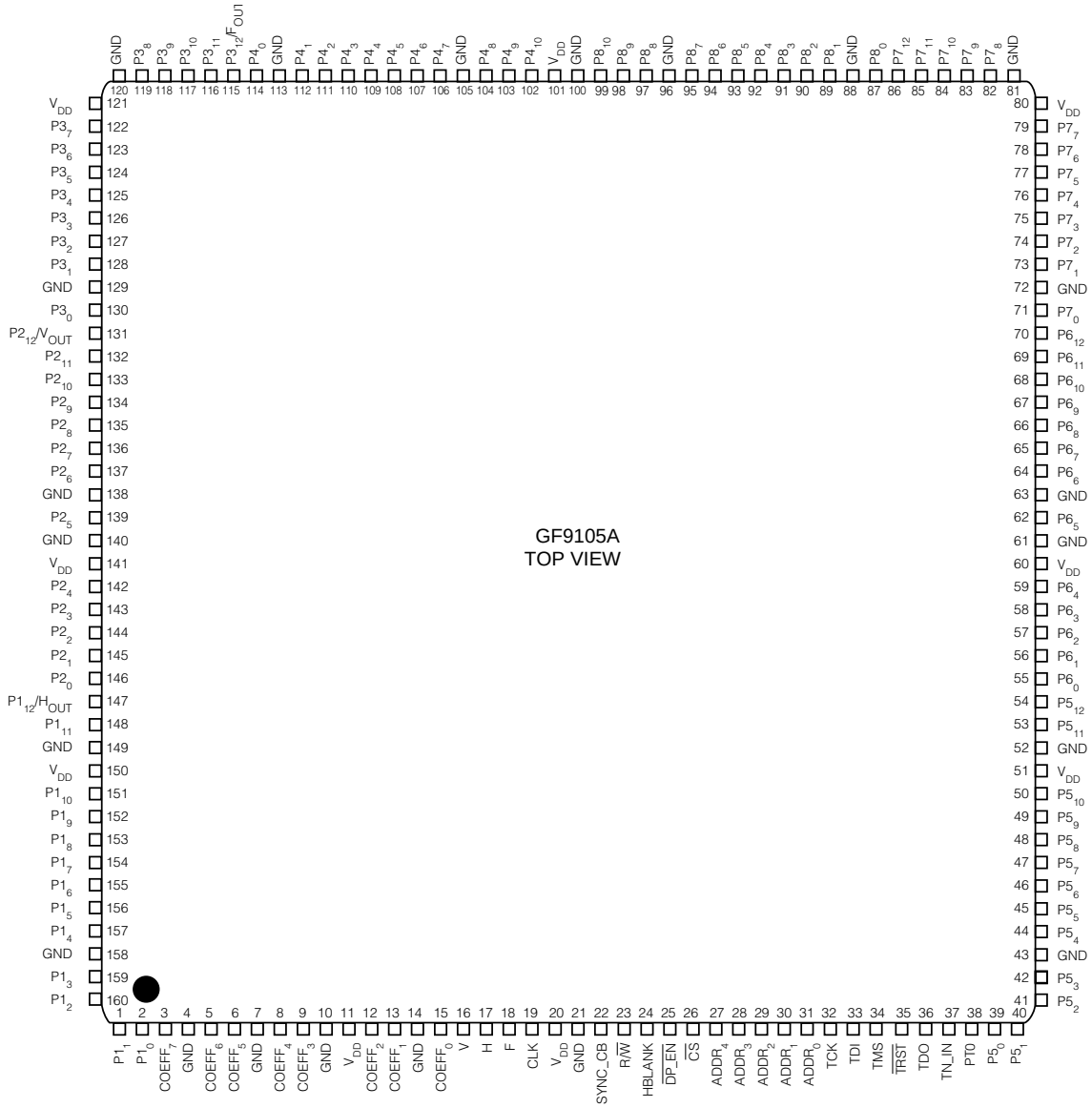


Fig. 2 GF9105A Pin Connections

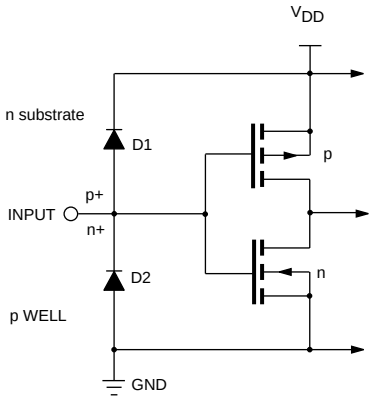


Fig. 3a GF9105A Equivalent Input Circuit

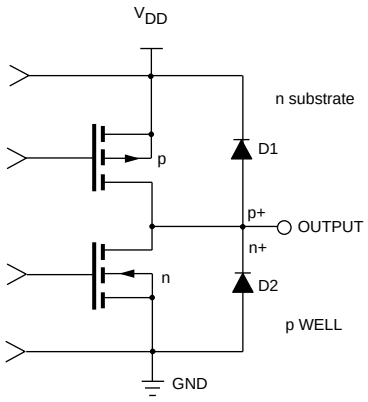


Fig. 3b GF9105A Equivalent Output Circuit

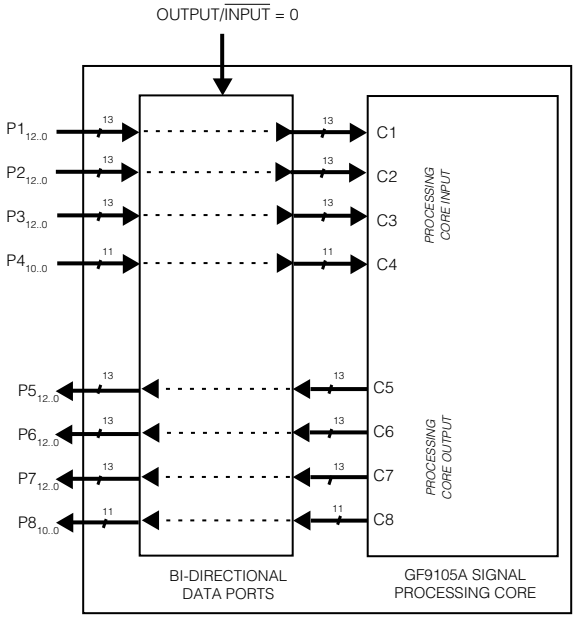


Fig. 4a Functional Block Diagram of GF9105A
(OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 0)

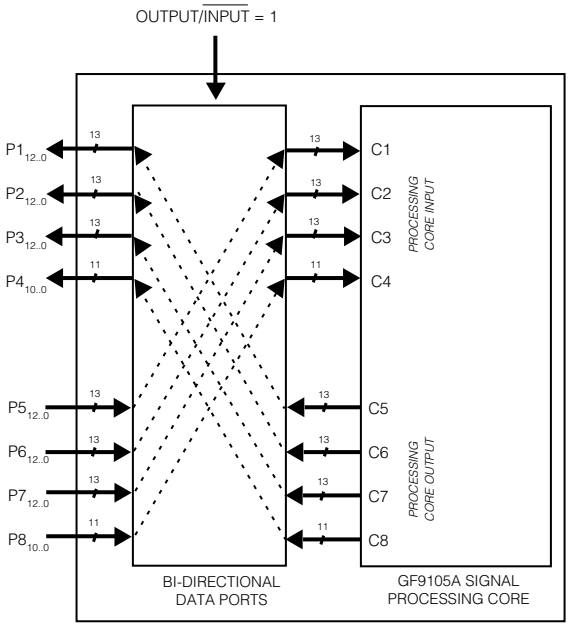


Fig. 4b Functional Block Diagram of GF9105A
(OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 0)

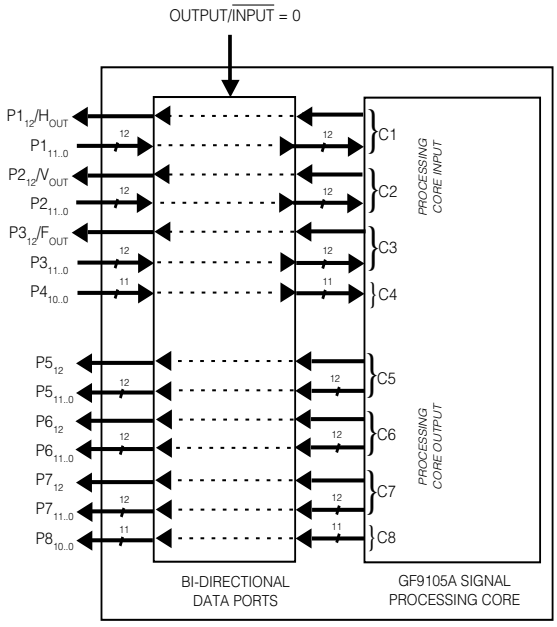


Fig. 4c Functional Block Diagram of GF9105A
(OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 1)

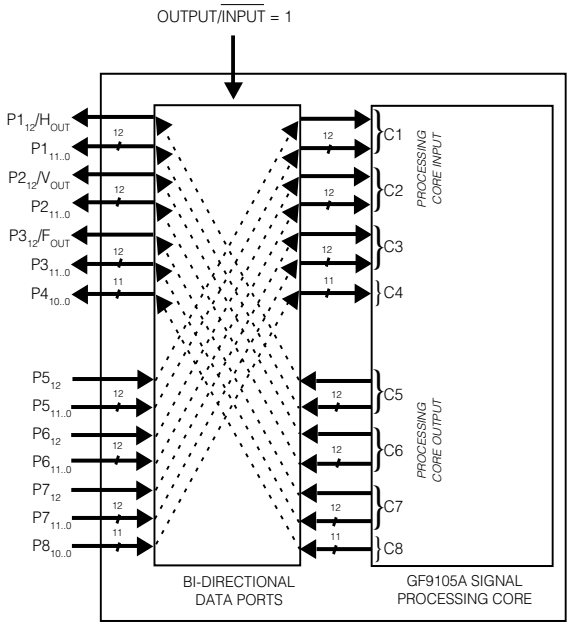


Fig. 4d Functional Block Diagram of GF9105A
(OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 1)

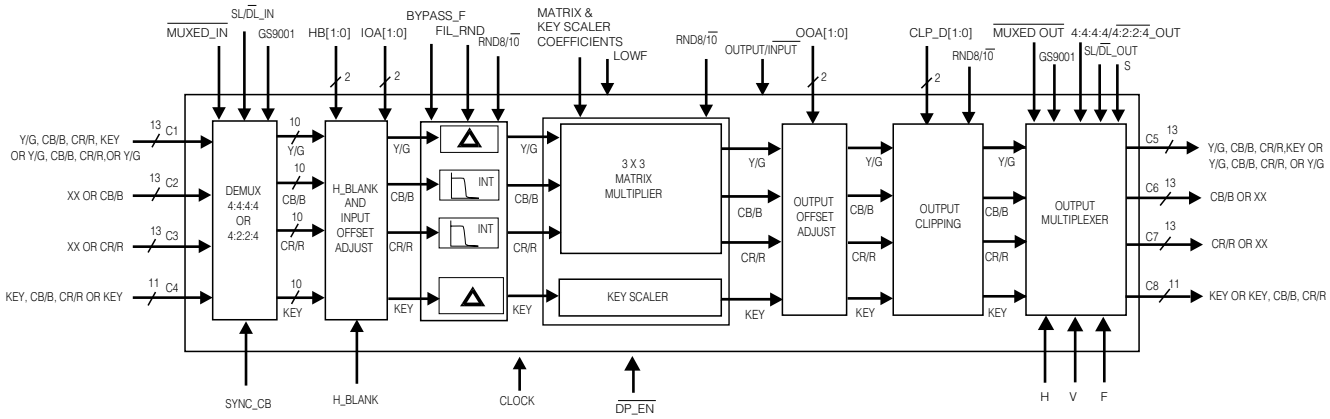


Fig. 5a Functionality of GF9105A Processing Core when INT/$\overline{DEC}$ = 1, HVF_OUT = 0

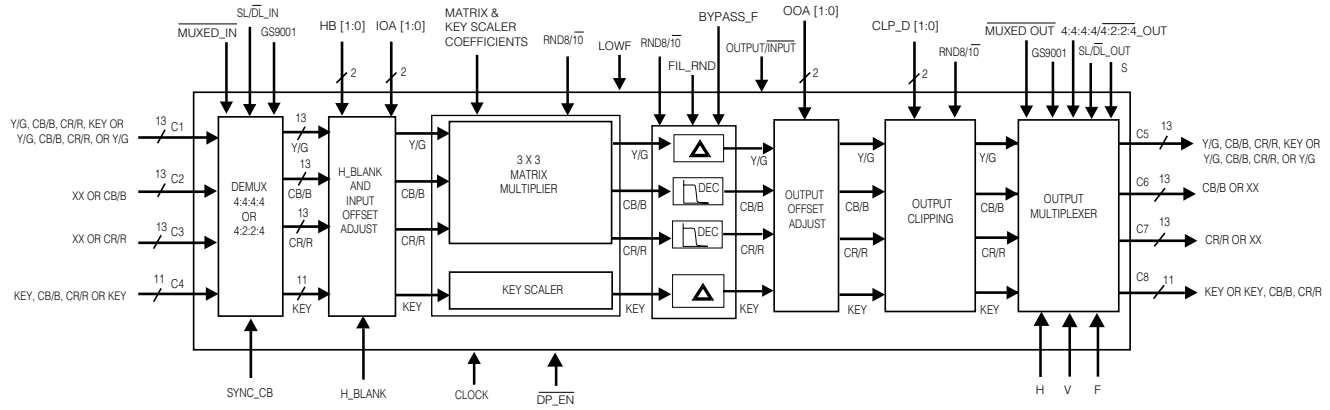


Fig. 5b Functionality of GF9105A Processing Core when INT/$\overline{DEC}$ = 0, HVF_OUT = 0

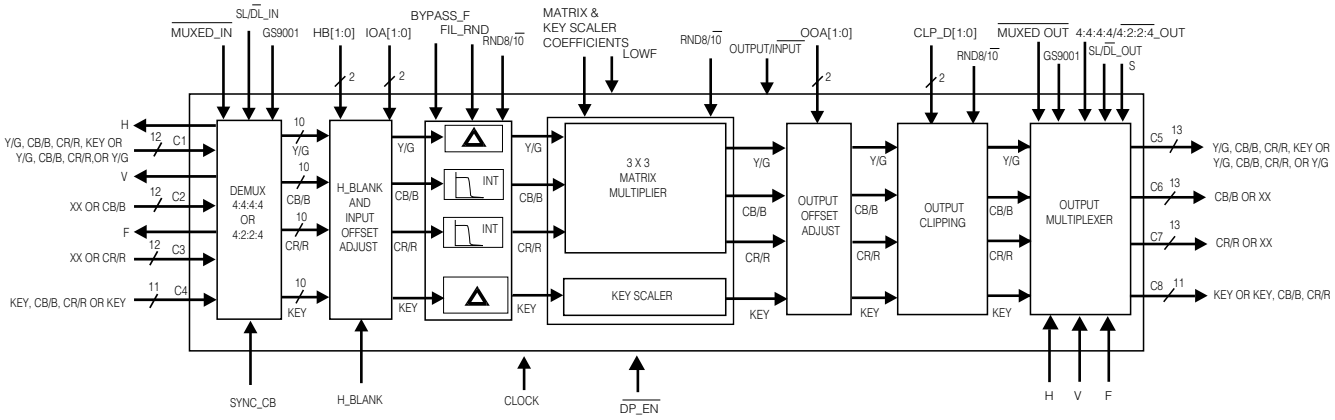


Fig. 5c Functionality of GF9105A Processing Core when INT/$\overline{\text{DEC}}$ = 1, HVF_OUT = 1

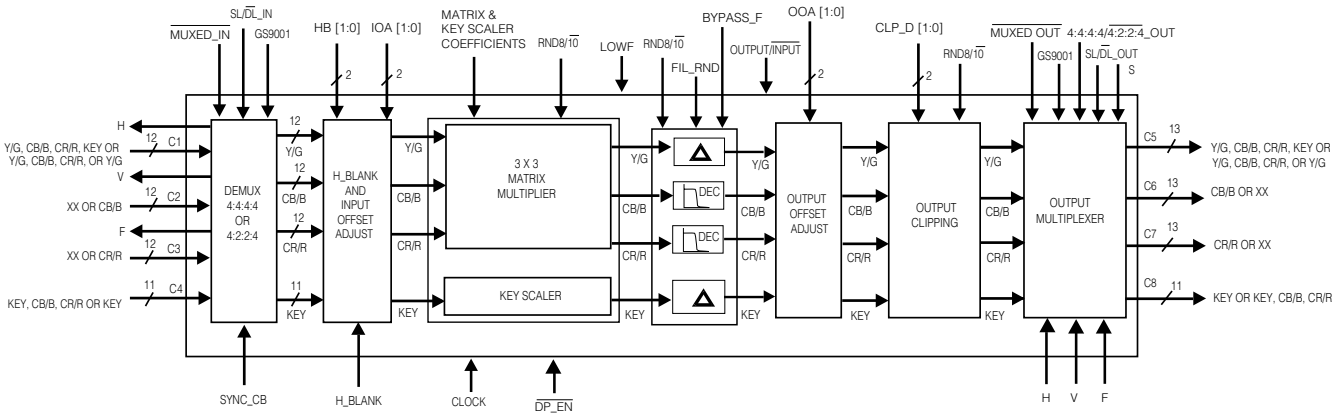


Fig. 5d Functionality of GF9105A Processing Core when INT/$\overline{\text{DEC}}$ = 0, HVF_OUT = 1

GF9105A DETAILED DEVICE DESCRIPTION

INPUT/OUTPUT DATA PORTS

The GF9105A has 8 bi-directional data ports, labelled P1 to P8. P1 to P3 and P5 to P7 are 13-bit data ports while P4 and P8 are 11-bit data ports. The OUTPUT/$\overline{\text{INPUT}}$ control bit and the HVF_OUT control bit (*See Host Programming Section* and figures 4a - 4d) control how P1 to P8 are configured.

When OUTPUT/$\overline{\text{INPUT}}$ is set low and when HVF_OUT is set low, $P1_{12..0}$, $P2_{12..0}$, $P3_{12..0}$, $P4_{10..0}$ are configured as input video data ports and $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as output video data ports (refer to Figure 4a).

When OUTPUT/$\overline{\text{INPUT}}$ is set low and when HVF_OUT is set high, $P1_{11..0}$, $P2_{11..0}$, $P3_{11..0}$, $P4_{10..0}$ are configured as input video data ports and $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as output video data ports. In this mode, $P1_{12}$, $P2_{12}$, $P3_{12}$ are configured as outputs for H, V, and F output data. $P1_{12}$ carries H data, $P2_{12}$ carries V data and $P3_{12}$ carries F data (refer to Figure 4c).

When OUTPUT/$\overline{\text{INPUT}}$ is set high and when HVF_OUT is set low, $P1_{12..0}$, $P2_{12..0}$, $P3_{12..0}$, $P4_{10..0}$ are configured as output video data ports and $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as input video data ports (refer to Figure 4b).

When OUTPUT/$\overline{\text{INPUT}}$ is set high and when HVF_OUT is set high, $P1_{11..0}$, $P2_{11..0}$, $P3_{11..0}$, $P4_{10..0}$ are configured as output video data ports and $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as input video data ports. In this mode, $P1_{12}$, $P2_{12}$, $P3_{12}$ are configured as outputs for HVF output data. $P1_{12}$ carries H data, $P2_{12}$ carries V data and $P3_{12}$ carries F data (refer to Figure 4d).

Note: No bi-directional I/Os should be driven until after the OUTPUT/$\overline{\text{INPUT}}$ and the HVF_OUT control bits have been set (unless $\overline{\text{DP\_EN}}$ is set high to tri-state the outputs). This will ensure that any potential conflicts between input and output data buses are avoided.

OUTPUT/$\overline{\text{INPUT}}$ AND HVF CONTROL BIT

OUTPUT/$\overline{\text{INPUT}}$	HVF_OUT	DESCRIPTION
0	0	$P1_{12..0}$, $P2_{12..0}$, $P3_{12..0}$, $P4_{10..0}$ are configured as input video data ports. $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as output video data ports. Refer to Figure 4a.
0	1	$P1_{11..0}$, $P2_{11..0}$, $P3_{11..0}$, $P4_{10..0}$ are configured as input video data ports. $P1_{12}$, $P2_{12}$, $P3_{12}$ are configured as H, V and F outputs, respectively. $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as output video data ports. Refer to Figure 4c.
1	0	$P1_{12..0}$, $P2_{12..0}$, $P3_{12..0}$, $P4_{10..0}$ are configured as output video data ports. $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as input video data ports. Refer to Figure 4b.
1	1	$P1_{11..0}$, $P2_{11..0}$, $P3_{11..0}$, $P4_{10..0}$ are configured as output video data ports. $P1_{12}$, $P2_{12}$, $P3_{12}$ are configured as H, V and F outputs, respectively. $P5_{12..0}$, $P6_{12..0}$, $P7_{12..0}$, $P8_{10..0}$ are configured as input video data ports. Refer to Figure 4d.

For H, V, F output timing refer to the Timing Reference Signal Section of this data sheet.

DATA PORT ENABLE

$\overline{\text{DP\_EN}}$ is used for synchronously enabling and disabling the bi-directional data ports of the GF9105A. When $\overline{\text{DP\_EN}}$ is set high, the data ports are disabled and set to a high impedance state. When $\overline{\text{DP\_EN}}$ is set low, all data ports are enabled.

$\overline{\text{DP\_EN}}$ CONTROL PIN

$\overline{\text{DP\_EN}}$	DESCRIPTION
0	Output data ports enabled.
1	Output data ports disabled (high impedance state).

INPUT CLOCK (CLK)

For standard video signals, the clock input (CLK) of the GF9105A runs at one of three rates: 13.5/18MHz, 27/36MHz or 54MHz. The 18 MHz and 36 MHz variations on main clock frequencies are used in 16 x 9 video applications where luminance is sampled at 18 MHz. The use of a 27/36MHz clock with the GF9105A is the most common application. These clocks can be used with any format of input or output data with the exception of single link mode. Figures 7a and 7c show multiplexed and non-multiplexed input data with a 27/36MHz clock. When the GF9105A is used with either SMPTE RP174 compliant single link input or output data, the input clock must run at 54 MHz (see Figure 7b).

A 13.5/18 MHz input clock speed can only be used when both the input and output data are in a non multiplexed format (see Figure 7d). This clock rate was added to the GF9105A for use when the device is operating with non-multiplexed input and output data, since in this case a 27.0MHz clock may not be available. To use the 13.5 MHz input clock rate, the LOWF control bit must be set HIGH. When input clock rates of 27.0 MHz or 54.0 MHz are used, the LOWF control bit must be set LOW. Please note, when using the GF9105A with non-multiplexed 4:2:2:4 or 4:4:4:4 input data and an input clock rate of 27/36MHz, two rising edges of the 27/36MHz input clock are required to latch in a 13.5/18MHz input data rate (see Figure 7c).

INPUT CLOCK SUMMARY	
INPUT CLOCK RATE (MHz)	MODES
13.5/18 MHz	Non-multiplexed Input Data AND Non-multiplexed Output Data (LOWF=1)
27/36 MHz	All Input / Output Data Formats EXCEPT Single Link
54 MHz	SMPTE RP174 Single Link Input OR Output Data

BASIC OPERATION OF THE GF9105A

The basic operating mode for the GF9105A is selected via the INT/$\overline{\text{DEC}}$ control bit (*See Host Programming Section*). The effective block diagram of the GF9105A Processing Core depends on the state of INT/$\overline{\text{DEC}}$. When INT/$\overline{\text{DEC}}$ is set high, the internal FIR filters are set for interpolation and are placed in front of the programmable 3X3 color space converter. Refer to Figures 5a and 5c for a functional block diagram of the GF9105A processing core when INT/$\overline{\text{DEC}}$ is set high. When INT/$\overline{\text{DEC}}$ is set low, the internal FIR filters are set for decimation and are placed after the programmable 3X3 color space converter. Refer to Figures 5b and 5d for a functional block diagram of the GF9105A with INT/$\overline{\text{DEC}}$ set low. In these figures, static control bits (signals loaded via the asynchronous parallel interface) are shown at the top of the diagram and control signals with dedicated input pins are shown at the bottom of the diagram.

INT/$\overline{\text{DEC}}$ CONTROL BIT

INT/$\overline{\text{DEC}}$	DESCRIPTION
0	FIR filters set for decimation. FIR filters placed after the 3X3 multiplier as in Figure 5b and 5d.
1	FIR filters set for interpolation. FIR filters placed before the 3x3 multiplier as in Figure 5a and 5c.

There are seven basic blocks that make up the GF9105A. These are:

- Input De-multiplexer
- Horizontal Blanking and Input Offset Adjustment
- FIR Filters
- 3x3 Color Space Converter and KEY Scaler
- Output Offset Adjustment
- Output Clipping
- Output Multiplexer

Since the GF9105A Processing Core functionality depends on the state of INT/$\overline{\text{DEC}}$, device operation will be described first for the case where INT/$\overline{\text{DEC}}$ is set high and then for the case where INT/$\overline{\text{DEC}}$ is set low.

GF9105A OPERATION IN INTERPOLATION MODE (INT/$\overline{\text{DEC}}$ = 1)

Refer to Figures 5a and 5c for a functional block diagram of GF9105A operation with INT/$\overline{\text{DEC}}$ = 1

BIT WEIGHTING

Although the input data ports are physically 13 bits or 11 bits wide, the GF9105A Processing Core is limited to processing 10 or 8-bit unsigned input data while INT/$\overline{\text{DEC}}$ is set high. It should be noted that while INT/$\overline{\text{DEC}}$ is set low, the GF9105A Processing Core will accept up to 13 bit input data. Refer to later sections for a description of Processing Core functionality while INT/$\overline{\text{DEC}}$ is set low.

As mentioned above, the GF9105A is limited to processing 10 or 8-bit unsigned input data while INT/$\overline{\text{DEC}}$ is set high. This input data must be properly embedded within the input data ports. The following table illustrates how to properly embed 10 or 8-bit data within the 13 bit data ports. Note that when OUTPUT/$\overline{\text{INPUT}}$=0 and HVF_OUT=1, $P1_{12}$, $P2_{12}$ and $P3_{12}$ (which corresponds to b_{12}) are outputs rather than inputs. These 3 outputs are used for presenting output H, V and F output signals. The user should be careful to ensure that $P1_{12}$, $P2_{12}$ and $P3_{12}$,are not driven by upstream logic when OUTPUT/$\overline{\text{INPUT}}$=0 and HVF_OUT=1. Other unused inputs should be set low by the user.

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ Embedded 10 bit signal	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P4_{10..0}$ Embedded 10 bit signal	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ Embedded 8 bit signal	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P4_{10..0}$ Embedded 8 bit signal	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

INPUT DE-MULTIPLEXER

The $\overline{\text{MUXED\_IN}}$ and SL/$\overline{\text{DL}}$_IN control bits (*See Host Programming Section*) determine the input data format. The $\overline{\text{MUXED\_IN}}$ control bit is used to identify whether the incoming data is in a multiplexed or non-multiplexed format. The SL/$\overline{\text{DL}}$_IN control bit is used to identify whether the incoming data is in a single link or dual link format.

Dual Link (SL/$\overline{\text{DL}}$_IN = 0)

While $\overline{\text{MUXED\_IN}}$ is set low, input data is assumed to be two 10 bit streams in 4:2:2:4 or 4:4:4:4 data format as shown in Figure 7a. The input de-multiplexer separates the 4:2:2:4 or 4:4:4:4 input signals into four channels of Y/G, C_B/B, C_R/R and KEY data. These four data streams are then passed to the next processing section.

When operating with multiplexed 4:2:2:4 or 4:4:4:4 input data, the 4:2:2 data stream enters the GF9105A Processing Core from Processing Core input port C1. While OUTPUT/$\overline{\text{INPUT}}$=0 Processing Core port C1 corresponds to device data port P1

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ Embedded 10 bit signal	H, V, or F output	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P4_{10..0}$ Embedded 10 bit signal	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ Embedded 8 bit signal	H, V, or F output	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P4_{10..0}$ Embedded 8 bit signal	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ Embedded 10 bit signal	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P8_{10..0}$ Embedded 10 bit signal	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ Embedded 8 bit signal	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P8_{10..0}$ Embedded 8 bit signal	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ Embedded 10 bit signal	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P8_{10..0}$ Embedded 10 bit signal	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ Embedded 8 bit signal	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P8_{10..0}$ Embedded 8 bit signal	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

(refer to Figures 4a and 4c). While OUTPUT/$\overline{\text{INPUT}}$=1 Processing Core port C1 corresponds to device data port P5 (Refer to Figures 4b and 4d).

The KEY:2:2 or KEY:XX:XX data enters the GF9105A Processing Core from Processing Core input port C4. While OUTPUT/$\overline{\text{INPUT}}$=0, Processing Core port C4 corresponds to device data port P4 (Refer to Figures 4a and 4c). While OUTPUT/$\overline{\text{INPUT}}$=1, Processing Core port C4 corresponds to device data port P8 (Refer to Figures 4b and 4d).

When $\overline{\text{MUXED\_IN}}$ is set high, input data is assumed to be 4:2:2:4 or 4:4:4:4 data in a non-multiplexed format as shown in Figure 7c. Since the incoming data is already non-multiplexed, the input data is passed on to the next processing section unmodified. In this mode of operation, input data is presented to all four Processing Core input ports. While OUTPUT/$\overline{\text{INPUT}}$=0, Processing Core ports C1-C4 correspond to device data ports P1-P4 (Refer to Figures 4a and 4c). While OUTPUT/$\overline{\text{INPUT}}$=1 Processing Core ports C1-C4 correspond to device data ports P5-P8 (Refer to Figure 4b and 4d).

Single Link (SL/$\overline{DL}$_IN = 1)

When operating with single link input data, the 4:4:4:4 data stream (SMPTE RP174 compliant) enters the GF9105A Processing Core from Processing Core input C1.

While OUTPUT/$\overline{INPUT}$ = 0 Processing Core Port C1 corresponds to device data port P1 (refer to Figures 4a and 4c). While OUTPUT/$\overline{INPUT}$ = 1 Processing Core Port C1 corresponds to device data port P5 (refer to Figures 4b and 4d). In this mode, the input clock (CLK) is operating at 54 MHz. Also, note that the $\overline{MUXED\_IN}$ control bit must be set low ($\overline{MUXED\_IN}$ = 0).

$\overline{MUXED\_IN}$ AND SL/$\overline{DL}$_IN CONTROL BITS

$\overline{MUXED\_IN}$	SL/$\overline{DL}$_IN	DESCRIPTION
0	0	Input is in a dual link multiplexed format.
0	1	Input is in a single link multiplexed format.
1	XX	Input is in a non-multiplexed format.

SYNCHRONIZATION

In order to properly synchronize the input de-multiplexer, the GF9105A requires a SYNC_CB control signal input. For multiplexed input data, SYNC_CB should change from high to low at the start of an even numbered CB sample. After synchronizing the device with the incoming data stream, SYNC_CB can remain low until re-synchronization is desired. Refer to Figure 7a for timing of SYNC_CB with a dual link multiplexed input data stream. Refer to Figure 7b for timing of SYNC_CB with a single link multiplexed input data signal. The timing shown may be referred to as “standard SYNC_CB timing”.

In order to simplify overall system design, the HSYNC output from the GS9001 EDH Coprocessor may be used as a SYNC_CB signal when operated with a 4:2:2 or dual link 4:4:4:4 input signal. In this mode of operation, the 10 bit multiplexed data entering the GF9105A must be fed from the output of the GS9001 and the GF9105A’s SYNC_CB input must be fed from the GS9001’s HSYNC output (Refer to Figure 8a). To use this mode of operation the GF9105A’s GS9001 control bit (*Refer to Host Programming Section*) must be set high. When operated with a 4:2:2 or a dual link 4:4:4:4 input signal and when the GS9001 control bit is set high, the GS9001’s HSYNC, VSYNC, and FIELD output signals may also be used to drive the GS9105A’s output multiplexer. Refer to the Timing Reference Signal section for information regarding this.

When dealing with single link 4:4:4:4 input or output signals “standard” SYNC_CB timing above must be used. When using standard SYNC_CB and HVF timing, the GS9001 control must be set low. The GS9020 may be used to provide such standard SYNC_CB timing and HVF. When operated in this manner, the 10 bit multiplexed data entering the GF9105A must be fed from the output of the GS9020 and the GF9105A’s SYNC_CB and HVF inputs must be fed from the GS9020’s H, V, F outputs. The same GS9020/GF9105A configuration may also be used when interfacing the GF9105A to a standard 4:2:2 or dual link 4:4:4:4 link input signal. In this case, the GS9001 control bit must still be set low.

GS9001 CONTROL BIT

GS9001	DESCRIPTION
0	Standard SYNC_CB and H,V,F timing. Simple interface to GS9020.
1	Modified SYNC_CB and H, V, F timing. Simple interface to GS9001.

NOTE: Standard SYNC_CB and H, V, F timing must be used when receiving or generating single link 4:4:4:4 signals.

With non-multiplexed input data, SYNC_CB must change from high to low at the start of an even-numbered CB sample. It is important to note that SYNC_CB changes from high to low on an even-numbered CB sample and not an odd-numbered sample. After synchronizing the device with the incoming data stream, the SYNC_CB signal can remain low until re-synchronization is desired. Refer to Figure 7c for timing of SYNC_CB with non-multiplexed input data. Following the input de-multiplexer, data is passed to the Horizontal Blanking section of the device.

HORIZONTAL BLANKING

When H_BLANK is high, all four channels of input are forced to a user selectable set of levels. When H_BLANK is low data is passed through the Horizontal Blanking section of the device unmodified. Refer to Figures 10a and 10b for typical timing of H_BLANK with multiplexed input data and Figure 10c for typical timing with non-multiplexed input data. In these figures, a

prime (′) indicates to which samples the H blanking will be applied. The HB_1 and HB_0 control bits *(See Host Programming Section)* determine which of the four sets of blanking levels are selected.

HB_1 AND HB_0 CONTROL BITS

HB_1	HB_0	DESCRIPTION
0	0	Blanking levels of 64, 512, 512 and 64 applied to Y/G, C_B/B, C_R/R and KEY channels respectively.
0	1	Blanking levels of 64, 64, 64 and 64 applied to Y/G, C_B/B, C_R/R and KEY channels respectively.
1	0	Blanking levels of 0, 0, 0 and 0 applied to Y/G, C_B/B, C_R/R and KEY channels respectively.
1	1	Blanking levels of 0, 512, 512 and 0 applied to Y/G, C_B/B, C_R/R and KEY channels respectively.

INPUT OFFSET ADJUSTMENT

Following the Horizontal Blanking function, a fixed set of offsets may be added to the input data. The IOA_1 and IOA_0 control bits *(See Host Programming Section)* specify which of the four possible input offset adjustments will be applied to the data. As an example, the interpolation/decimation filters operate on two's complement data, so for $Y/C_B/C_R$ input, IOA_1 and IOA_0 should both be set low to remove the inherent offset from the incoming data.

IOA_1 AND IOA_0 CONTROL BITS

IOA_1	IOA_0	DESCRIPTION
0	0	Offsets of -64, -512, -512 and -64 added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
0	1	Offsets of -64, -64, -64 and -64 added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
1	0	Offsets of 0, 0, 0 and 0 added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
1	1	Offsets of 0, -512, -512 and 0 added to the Y/G, C_B/B, C_R/R and KEY channels respectively.

FIR FILTERS

Following the Input Offset Adjustment, data is passed to the FIR filtering section of the device. These filters, when enabled, will up-sample C_B and C_R data by a factor of two so that 4:2:2:4 data is sample-rate converted to 4:4:4:4 data. Subsequent processing of co-sited Y, C_B and C_R samples may take place on such 4:4:4:4 data. The frequency response of these CCIR-601 compliant FIR filters is shown in Figures 6a and 6b and the characteristics are listed in Figure 6c. In order to maintain proper synchronization between all four channels of input data, the Y/G and KEY channels are passed through a digital delay line that matches the FIR filter latency. Output resolution from the FIR filters depends on the state of the RND8/$\overline{10}$ and FIL_RND control bits (*See Host Programming Section*). RND8/$\overline{10}$ should always be set to match the data format being output by the device (high for 8 bit data or low for 10 bit data). FIL_RND should be set low unless the GF9105A is being used in a mode where the 3X3 matrix is set for unity gain bypass mode. (*See 3X3 Color Space Converter and KEY Scaler Section).* In this case, FIL_RND should be set high. The FIR filter only takes 10-bit input in interpolation mode and proper input offset has to be used.

RND8/$\overline{10}$ AND FIL_RND CONTROL BITS

RND8/$\overline{10}$	FIL_RND	DESCRIPTION
0	0	Output has minimum rounding for high accuracy for a non-identity matrix, using 10-bit input data.
0	1	More rounding is performed to increase overall accuracy when matrix is being bypassed, using 10-bit input data.
1	0	Output has minimum rounding for high accuracy for a non-identity matrix, using 8-bit input data.
1	1	More rounding is performed to increase overall accuracy when matrix is being bypassed, using 8-bit input data.

The BYPASS_F control bit *(See Host Programming Section)* can be used to bypass the interpolation filters. When this bit is set low, the filters are enabled and normal operation occurs. When this bit is set high, the filters are bypassed and the data is passed through the filter section unmodified. FIL_RND should be set low when BYPASS_F is set high. Total latency through the filter is independent of the BYPASS_F control signal. Note that after changing the state of BYPASS_F, an initialization period corresponding to the device's latency is required before valid data is available at the output of the device.

BYPASS_F CONTROL BIT

BYPASS_F	DESCRIPTION
0	Filters are enabled. Data is sample-rate converted from 4:2:2:4 to 4:4:4:4 data.
1	Filters are disabled. Data is passed through the filter section unmodified.

3X3 COLOR SPACE CONVERTER AND KEY SCALER

In this section, a 3X3 matrix multiplication (color space conversion) may be performed on the Y/G, C_B/B and C_R/R data. The 3X3 matrix multiplier has 13-bit two's complement coefficients and maintains full precision throughout the 3X3 calculation. The nine 13-bit coefficients (*See Host Programming Section*) used in this 3X3 calculation determine the color space conversion that the GF9105A will perform. These coefficients are referred to as CM_{ij}, where i refers to the row and j refers to the column in which CM_{ij} is found. The matrix multiplication can be shown as:

$$\begin{bmatrix} Y/G_{OUT} \\ C_B/B_{OUT} \\ C_R/R_{OUT} \end{bmatrix} = \begin{bmatrix} CM_{11} & CM_{12} & CM_{13} \\ CM_{21} & CM_{22} & CM_{23} \\ CM_{31} & CM_{32} & CM_{33} \end{bmatrix} \begin{bmatrix} Y/G_{IN} \\ C_B/B_{IN} \\ C_R/R_{IN} \end{bmatrix}$$

The nine matrix coefficients have 13-bit two's complement resolution and cover a range from -4 to +3.9990234375. Bit weighting for the coefficients is as follows:

Coefficient Bit	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Weighting	-2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}

Matrix bypassing can be accomplished by setting FIL_RND high and loading an identity matrix, by setting CM_{11}, CM_{22} and CM_{33} to unity and setting the remaining six coefficients to zero. In this mode, gain through the matrix stage is 1.000.

Typical examples of matrix coefficients that will provide full range RGB to YC_BC_R, and YC_BC_R to full range RGB conversions are:

$$\begin{bmatrix} Y \\ C_B \\ C_R \end{bmatrix} = \begin{bmatrix} 0.5027 & 0.0976 & 0.2561 \\ -0.2899 & 0.4376 & -0.1477 \\ -0.3633 & -0.0711 & 0.4374 \end{bmatrix} \begin{bmatrix} G \\ B \\ R \end{bmatrix}$$

$$\begin{bmatrix} G \\ B \\ R \end{bmatrix} = \begin{bmatrix} 1.1677 & -0.3931 & -0.8164 \\ 1.1677 & 2.0248 & 0 \\ 1.1677 & 0 & 1.6025 \end{bmatrix} \begin{bmatrix} Y \\ C_B \\ C_R \end{bmatrix}$$

KEY signals may also be scaled by a programmable scaling factor. The KEY scaling coefficient *(See HOST Programming Section)* has the same resolution and bit weighting as the nine 3X3 matrix multiplier coefficients.

Typical examples of KEY scaler values that could be used are:

KEY scaler = 0.8563 for full range RGB to YC_BC_R conversions.
KEY scaler = 1.1677 for YC_BC_R to full range RGB conversions.

MATRIX OUTPUT RESOLUTION

Full precision is maintained within the 3X3 matrix multiplier until the output is rounded to a 13-bit or 11-bit word, depending on the state of the RND8/$\overline{10}$ control bit.

3X3 MATRIX MULITPLIER OUTPUT RESOLUTION FOR Y/G, C_B/B AND C_R/R CHANNELS

RND8/$\overline{10}$	DESCRIPTION
0	Matrix output channels rounded to 13 bits.
1	Matrix output channels rounded to 11 bits.

Output from the KEY scaler is also rounded and clipped based on the state of the RND8/$\overline{10}$ control bit.

KEY SCALER OUTPUT

RND8/$\overline{10}$	DESCRIPTION
0	Output of KEY Scaler rounded to 11 bits.
1	Output of KEY Scaler rounded to 9 bits.

OUTPUT OFFSET ADJUSTMENT

Output offset adjustment is provided to allow a specified set of offsets to be added to the data streams. The control bits OOA_1 and OOA_0 *(See Host Programming Section)* determine which set of offsets is applied to the data.

OOA_1 AND OOA_0 CONTROL BITS

OOA_1	OOA_0	DESCRIPTION
0	0	Offsets of 64, 512, 512 and 64 are added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
0	1	Offsets of 64, 64, 64 and 64 are added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
1	0	Offsets of 0, 0, 0 and 0 are added to the Y/G, C_B/B, C_R/R and KEY channels respectively.
1	1	Offsets of 0, 512, 512 and 0 are added to the Y/G, C_B/B, C_R/R and KEY channels respectively.

OUTPUT CLIPPING

In the output clipping block, the data is clipped to a specific number of bits. The CLP_D_1 and CLP_D_0 control bits (See Host Programming Section) determine the clipping mode that will occur.

OUTPUT MULTIPLEXER

The $\overline{MUXED\_OUT}$, 4:4:4:4/$\overline{4:2:2:4}$_OUT, SL/$\overline{DL}$_OUT and HVF_OUT control bits *(See Host Programming Section)* determine the output data format.

Dual Link (SL/$\overline{DL}$_OUT = 0)

When $\overline{MUXED\_OUT}$ and 4:4:4:4/$\overline{4:2:2:4}$_OUT are both set low, the device will multiplex the three channels of Y/G, C_B/B and C_R/R data into a single channel of 4:2:2 data as prescribed by SMPTE 125M. KEY information will be presented in a KEY:2:2 format where the C_B/C_R samples in the key channel are set to color blanking levels as outlined in ITU-R-601. This mode can only be used when the output data has been rounded to 10-bit or 8-bit unsigned data. The 4:2:2 data stream is presented on Processing Core output data port C5 and the KEY:2:2 data is presented on Processing Core output data port C8.

When $\overline{MUXED\_OUT}$ is set low and 4:4:4:4/$\overline{4:2:2:4}$_OUT is set high, the device will multiplex the four channels of Y/G, C_B/B, C_R/R and KEY information into two streams of 4:2:2 and KEY:2:2 data as prescribed by SMPTE 125M. This mode can only be used when the output data has been clipped to 10-bit or 8-bit unsigned data. The 4:2:2 data stream is presented on Processing Core output data port C5 and the KEY:2:2 data is output on Processing Core output data port C8. Timing Reference Signals (TRS) may be inserted into the output data streams with such TRS signals conforming to the EAV/SAV

CLP_D_1 AND CLP_D_0 CONTROL BIT OPERATION

RND8/$\overline{10}$	CLP_D_1	CLP_D_0	DESCRIPTION
0	0	0	Y/G, C_B/B, C_R/R Channels: Clipped to a 13-bit two's complement number (Values -4096 to 4095) KEY Channel: Clipped to an 11-bit two's complement number (Values -1024 to +1023)
0	0	1	Y/G, C_B/B, C_R/R Channels: Clipped to a 12-bit two's complement number (Values -2048 to 2047) KEY Channel: Clipped to an 11-bit two's complement number (Values -1024 to +1023)
0	1	0	Y/G, C_B/B, C_R/R, KEY Channels: Clipped to a 10-bit unsigned number (Values 0 to +1023)
0	1	1	Y/G, C_B/B, C_R/R, KEY Channels: Clipped to a 10-bit unsigned number (Values +4 to +1019)
1	0	0	Y/G, C_B/B, C_R/R Channels: Clipped to a 11-bit two's complement number (Values -1024 to 1023) KEY Channel: Clipped to an 9-bit two's complement number (Values -256 to +255)
1	0	1	Y/G, C_B/B, C_R/R Channels: Clipped to a 10-bit two's complement number (Values -512 to +511) KEY Channel: Clipped to an 9-bit two's complement number (Values -256 to +255)
1	1	0	Y/G, C_B/B, C_R/R, KEY Channels: Clipped to a 8-bit unsigned number (Values 0 to +255)
1	1	1	Y/G, C_B/B, C_R/R, KEY Channels: Clipped to a 8-bit unsigned number (Values +1 to +254)

formats as outlined in SMPTE 125M. (See TRS Insertion Section).

When OUTPUT/$\overline{\text{INPUT}}$ is set high, Processing Core output port C5 corresponds to device data port P1 and Processing Core output port C8 corresponds to device data port P4. While OUTPUT/$\overline{\text{INPUT}}$ is set low, Processing Core output port C5 corresponds to device data port P5 and Processing Core output port C8 corresponds to device data port P8.

Single Link (SL/$\overline{\text{DL}}$_OUT = 1)

When generating single link output data, the 4:4:4:4 data stream (SMPTE RP174 compliant) exits the GF9105A Processing Core from Processing Core output C5. While OUTPUT/$\overline{\text{INPUT}}$ = 0 Processing Core port C5 corresponds to device data port P5(refer to Figure 4a). While OUTPUT/$\overline{\text{INPUT}}$ = 1 Processing Core Port C5 corresponds to device data port P1 (refer to Figure 4b). In this mode, the input clock (CLK) is operating at 54 MHz. Also, note that the $\overline{\text{MUXED\_OUT}}$ control bit must be set LOW ($\overline{\text{MUXED\_OUT}}$ = 0) and the 4:4:4:4/$\overline{4:2:2:4}$_OUT control bit must be set HIGH (4:4:4:4/$\overline{4:2:2:4}$_OUT = 1)

.

$\overline{\text{MUXED\_OUT}}$, 4:4:4:4/$\overline{4:2:2:4}$_OUT AND SL/$\overline{\text{DL}}$_OUT CONTROL BITS

$\overline{\text{MUXED\_OUT}}$	4:4:4:4/$\overline{4:2:2:4}$_OUT	SL/$\overline{\text{DL}}$_OUT	DESCRIPTION
0	0	0	Output data in a 4:2:2:4 dual link multiplexed format.
0	1	0	Output data in a 4:4:4:4 dual link multiplexed format.
0	1	1	Output data in a 4:4:4:4 single link multiplexed format.
1	0	XX	Output 4:2:2:4 data in a non-multiplexed format.
1	1	XX	Output 4:4:4:4 data in a non-multiplexed format.

When the device is configured for outputting non-multiplexed data and RND8/$\overline{10}$ is set low, 13-bit two's complement,12-bit two's complement, or 10-bit unsigned data may be output on Processing Core output data ports C5-C7 and 11-bit two's complement or 10-bit unsigned data output on the Processing Core output data port C8. The output data will be embedded within the physical 13-bit output ports as shown in the following tables. Note that when HVF_OUT=1 and OUTPUT/$\overline{\text{INPUT}}$=1 b_{12} of the GF9105As 13-bit two's complement output is not available. In this case, the 13-bit output data is clipped to a 12-bit two's complement number. Bit 12 (b_{12}) of the 13 bit physical interface is used to output the H, V and F output signals. In this case, 13 bit output data is clipped 13 bit to a 12 bit two's complement number.

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 13-bit Two's Complement output	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 12 bit Two's Complement output (b_{11} extended)	b_{11}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 10 bit unsigned output	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P8_{10..0}$ 11-bit Two's Complement output	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P8_{10..0}$ 10 bit unsigned output	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12}$, $P2_{12\ or}$ $P3_{12}$	H, V or F output	-	-	-	-	-	-	-	-	-	-	-	-
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 13-bit Two's Complement output	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 12-bit Two's Complement output (b_{11} extended)	b_{11}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 10 bit unsigned output	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P8_{10..0}$ 11 bit Two's Complement output	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P8_{10..0}$ 10 bit unsigned output	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0

When the device is configured for outputting non-multiplexed data and RND8/$\overline{10}$ is set high, the output bit weighting is slightly modified. For non-multiplexed output formats, the device may output 11-bit two's complement,10-bit two's complement or 8-bit unsigned data on Processing Core output data ports C5-C7, and 9-bit two's complement or 8-bit unsigned data may be output on Processing Core output data port C8. Note that when HVF_OUT=1 and OUTPUT/$\overline{\text{INPUT}}$=1 the MSB of the 11-bit two's complement output is not available. In this case, the output data is clipped to a 10-bit two's complement number (-512 to + 511). Bit 12 (b_{12}) of the physical interface is used to output the H, V and F output signals.

The output data will be embedded within the physical 13-bit output ports as shown below.

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 13 bit Two's Complement output	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 12-bit Two's Complement output (b_{11} extended)	b_{11}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 10 bit unsigned output	0	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P4_{10..0}$ 11 bit Two's Complement output	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P4_{10..0}$ 10 bit unsigned output	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 12 bit Two's Complement output	H, V or F output	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 10 bit unsigned output	H, V or F output	0	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P4_{10..0}$ 11 bit Two's Complement output	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P4_{10..0}$ 10 bit unsigned output	NA	NA	0	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 11 bit Two's Complement output	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 10 bit Two's Complement output (b_9 extended)	b_9	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 8 bit unsigned output	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P8_{10..0}$ 9 bit Two's Complement output	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P8_{10..0}$ 8 bit unsigned output	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

When the device is configured for outputting multiplexed data, 8-bit or 10-bit unsigned data is transferred to the output data ports. Consult the tables of the Bit Weighting section for embedding 8 or 10 bits within 13 bit data ports. Note that when HVF_OUT=1 and OUTPUT/$\overline{\text{INPUT}}$=1, the MSB of the GF9105As 13 bit of the physical interfaces are used to output the H, V and F output signals.

OUTPUT/$\overline{\text{INPUT}}$ = 0, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12}$, $P2_{12}$ or $P3_{12}$	H, V or F output	-	-	-	-	-	-	-	-	-	-	-	-
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 11 bit Two's Complement output	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 10 bit Two's Complement output (b_9 extended)	b_9	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P5_{12..0}$ to $P7_{12..0}$ 8 bit unsigned output	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P8_{10..0}$ 9 bit Two's Complement output	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P8_{10..0}$ 8 bit unsigned output	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 11 bit Two's Complement output	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 10 bit Two's Complement output (b_{11} extended)	b_9	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 8 bit unsigned output	0	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P4_{10..0}$ 9 bit Two's Complement output	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P4_{10..0}$ 8 bit unsigned output	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 10 bit Two's Complement output	H, V or F output	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P1_{12..0}$ to $P3_{12..0}$ 8 bit unsigned output	H, V or F output	0	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P4_{10..0}$ 9 bit Two's Complement output	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Output Port: $P4_{10..0}$ 8 bit unsigned output	NA	NA	0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

GF9105A OPERATION IN DECIMATION MODE (INT/$\overline{DEC}$=0)

Refer to Figure 5b for a functional block diagram of the GF9105A operation with INT/$\overline{DEC}$=0

BIT WEIGHTING

When using multiplexed input data, the Processing Core is limited to processing either 8-bit or 10-bit unsigned input data. The input data should be embedded within the 13-bit data port as shown in the tables of the Bit Weighting subsection of the Interpolation Mode Section. Note that when HVF_OUT=1, $P1_{12}$, $P2_{12}$ and $P3_{12}$ (which corresponds to b_{12}) are outputs rather than inputs. These 3 outputs are used for presenting H, V and F output signals. The user should be careful to ensure that $P1_{12}$, $P2_{12}$ and $P3_{12}$ are not driven by upstream logic when HVF_OUT=1. Other unused inputs should be set low.

When using non-multiplexed input data, the GF9105A Processing Core can accept up to 13-bit two's complement data from Processing Core input ports C1-C3 and up to 11-bit two's complement data from Processing Core input port C4. Note that signed or unsigned numbers that fit within the relevant 13-bit or 11-bit dynamic range may also be presented to the device inputs. This type of input data must still be formatted as a 13-bit or 11-bit two's complement number, with appropriate sign extensions. Input bit weighting is as shown below.

OUTPUT/$\overline{INPUT}$ = 0, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ 13 bit Two's Complement input (10 bit based data)	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{12..0}$ to $P3_{12..0}$ 11 bit Two's Complement input (8 bit based data)	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P4_{10..0}$ 11 bit Two's Complement input (10 bit based data)	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P4_{10..0}$ 9 bit unsigned input (8 bit based data)	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{INPUT}$ = 0, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Output Port: $P1_{12}$ $P2_{12}$ or $P3_{12}$	H, V or F output	-	-	-	-	-	-	-	-	-	-	-	-
Input Port: $P1_{11..0}$ to $P3_{11..0}$ 12 bit Two's Complement input (10 bit based data)	-	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P1_{11..0}$ to $P3_{11..0}$ 10 bit Two's Complement input (8 bit based data)	-	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P4_{10..0}$ 11 bit Two's Complement input (10 bit based data)	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P4_{10..0}$ 9 bit unsigned input (8 bit based data)	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 0	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ 13 bit Two's Complement input (10 bit based data)	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ 11 bit Two's Complement input (8 bit based data)	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P8_{10..0}$ 11 bit Two's Complement input (10 bit based data)	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P8_{10..0}$ 9 bit unsigned input (8 bit based data)	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

OUTPUT/$\overline{\text{INPUT}}$ = 1, HVF_OUT = 1	13 BIT PHYSICAL INTERFACE												
DATA PORT REFERENCE	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ 13 bit Two's Complement input (10 bit based data)	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P5_{12..0}$ to $P7_{12..0}$ 11 bit Two's Complement input (8 bit based data)	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0
Input Port: $P8_{10..0}$ 11 bit Two's Complement input (10 bit based data)	NA	NA	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
Input Port: $P8_{10..0}$ 9 bit unsigned input (8 bit based data)	NA	NA	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	0	0

Input De-multiplexer

Refer to the Input De-multiplexer discussion in the interpolation mode section.

Horizontal Blanking

Refer to the Horizontal Blanking discussion in the interpolation mode section.

Input Offset Adjustment

Refer to the Input Offset Adjustment discussion in the interpolation mode section.

3X3 Color Space Converter and KEY Scaler

Refer to the 3X3 Color Space Converter and KEY scaler discussion in the interpolation mode section.

MATRIX OUTPUT RESOLUTION

Full precision is maintained throughout the 3X3 matrix multiplication. To ensure that maximum precision is maintained by the GF9105A, rounding of the Y/G, C_B/B and C_R/R channels depends on the state of the RND8/$\overline{10}$ and BYPASS_F control bits *(See HOST Programming Section)*.

3X3 MATRIX MULTIPLIER RESOLUTION FOR Y/G, C_B/B AND C_R/R CHANNELS

RND8/$\overline{10}$	BYPASS_F	DESCRIPTION
0	X	LSBs are rounded off leaving 10-bit core data and 2 MSB extension bits.
1	0	Minimal rounding is performed, leaving the 8-bit core data and MSB/LSB extensions for high accuracy when filter is not bypassed.
1	1	More rounding is performed, leaving 8-bit core data and MSB extension bits to increase overall accuracy when filter is being bypassed.

FIR FILTERS

With INT/$\overline{DEC}$ set low, the internal FIR filters will be set for decimation of up to 12 input bits, and the C_B/B and C_R/R channels will be decimated by a factor of two. As a result, 4:4:4:4 data will be sample rate converted to 4:2:2:4 data. The frequency response of the decimation filters are shown in Figure 6a and Figure 6b and the characteristics are listed in Figure 6c.

Resolution out of the FIR filters is 13 bits when the device is operated with 10-bit input data and 11 bits when the device is operated with 8-bit data. The FIL_RND control bit *(See HOST Programming Section)* should always be set low while INT/$\overline{DEC}$ is set low.

FILTER OUTPUT ROUNDING FOR C_B/B AND C_R/R CHANNELS

RND8/$\overline{10}$	DESCRIPTION
0	C_B/B and C_R/R channels rounded to 13-bit output resolution.
1	C_B/B and C_R/R channels rounded to 11-bit output resolution.

The BYPASS_F control bit (*See Host Programming Section)* can be used to bypass the decimation filters. When this bit is set low, the filters are enabled and normal operation occurs. When this bit is set high, the filters are bypassed and the data is passed through the filter section unmodified. Total latency through the filter is independent of the BYPASS_F control signal. Note that after changing the state of BYPASS_F, an initialization period corresponding to the latency of the chip is required before valid data is available at the output of the device.

BYPASS_F CONTROL BIT OPERATION

BYPASS_F	DESCRIPTION
0	Filters are enabled. Data is sample-rate converted from 4:4:4:4 to 4:2:2:4 data.
1	Filters are disabled. Data is passed through the filter section unmodified.

Output Offset Adjustment

Refer to the Output Offset Adjustment discussion in the interpolation mode section.

Output Clipping

Refer to the Output Clipping discussion in the interpolation mode section.

Output Multiplexer

Refer to the Output Multiplexer discussion in the interpolation mode section.

TIMING REFERENCE SIGNAL (TRS)

Timing Reference Signals (TRS) may be inserted into the output data stream of the GF9105A. In order for the TRS signals to be inserted, the GF9105A's H, V and F inputs must be driven with external Horizontal (H), Vertical (V) and Field (F) signals. Such signals should be synchronized with the incoming data stream. A low to high transition of H triggers the insertion of an EAV sequence and a high to low transition triggers the insertion of an SAV sequence. Figures 9a, 9b and 9c show the standard timing (GS9001 control bit is set low) relationships between input data and the H, V and F inputs for multiplexed data, non-multiplexed data, and single link (4:4:4:4) data, respectively.

When the GS9001 control bit is set high and when operating with a multiplexed 4:2:2 data stream or a dual link (4:4:4:4) data stream, HVF input signals required for TRS insertion may be supplied by the GS9001. In this case, the multiplexed data being fed to the GF9105A comes from the GS9001output data bus and the H input of the GF9105A is fed from the HSYNC output of the GS9001. In addition, the V and F inputs of the GF9105A are fed from the VBLANK and the FIELD outputs of the GS9001. The relative timing of the input data and the H, V and F input signals in this mode of operation is shown in Figure 9d.

The H, V and F output signals of the GF9105A are derived from the H, V and F input signals. Figures 9e, 9f and 9g show the timing relationship between the data output and the H, V and F output signals for multiplexed, non-multiplexed and single link output data. These timing relationships will be valid provided the timing relationships between the input data and the input H, V and F input signals are maintained as shown in Figures 9a through to 9e. Note the GS9001 bit does not affect the output H, V and F timing.

DEVICE LATENCY

When the device is working with dual link input and output data, latency through the device is 68 clock cycles and is constant regardless of which mode the device is in. When the device is working with single link input or output data, latency through the device is 136 clock cycles and is constant regardless of which mode the device is in. The latency is counted by starting at the clock cycle that latches in the input data, and counting the number of clock cycles that occur until the corresponding output data is clocked out of the device, as illustrated in Figure 13.

HOST PROGRAMMING

The GF9105A has a host interface that allows programming of the 9 matrix coefficients, the key scaler coefficient, and several static control bits that are used to set the operating mode of the GF9105A. This data is loaded into 23 memory locations. The host interface consists of a 5-bit address bus (ADDR[4:0]), an 8-bit bi-directional coefficient port (COEFF_PORT[7:0]), a read/write pin (R/$\overline{W}$), and a chip select pin ($\overline{CS}$).

To write to a specific memory location, the R/$\overline{W}$ pin must be set low (putting the coefficient port in input mode). In addition, the address and coefficient buses must be set. Following this, the $\overline{CS}$ pin should be changed from high to low. Data will then be clocked into the specified address.

The settings of a specific memory location can be observed by performing a read operation. This is carried out by setting the R/$\overline{W}$ pin high (thus putting the coefficient bus in output mode) and setting the address bus before changing the $\overline{CS}$ pin from high to low to clock-in the address. This causes the data stored in the corresponding address to be output on the coefficient bus.

The standard timing for host writing and reading is shown in Figures 11a and 11b. This is the simplest method of using the host interface because R/$\overline{W}$ and the address bus (and coefficient bus when writing) all change at the same time, a minimum of 20 ns before and after the falling edge of $\overline{CS}$. The maximum frequency for $\overline{CS}$ using this mode of operation is 25 MHz.

Faster (more advanced) reading and writing can be achieved by meeting certain timing requirements, as shown in Figures 12a and 12b. The R/$\overline{W}$ signal setup time must be met before the first falling edge of $\overline{CS}$. In addition, normal setup and hold times must be provided on the address bus (and the data bus when writing) with respect to the falling edge of $\overline{CS}$. The maximum frequency using this timing is 40 MHz.

Note that the coefficient (COEFF_PORT[7:0]) I/O are tri-stated when $\overline{CS}$=1 or when R/$\overline{W}$=0.

Since the memory is random access, it is not necessary to write to or read from memory locations sequentially. The memory can be considered as separate from the GF9105A Processing Core and can be programmed independently of the system clock.

Since the nine matrix coefficients and the KEY scaler coefficient are 13 bits wide and the memory locations are only 8 bits wide, each coefficient requires 2 memory locations. For each coefficient, the 5 LSBs are loaded into the MSBs of the first memory location and the 8 MSBs are loaded into the second memory location.

For example, when loading a 13-bit coefficient into address N and address N+1, bit placement shall be as follows:

The memory is organized such that the 9 matrix coefficients and the key scaler coefficient occupy addresses 0 through 19 (ADDR[4:0]=00000 through ADDR[4:0]=10011). Addresses 20 (ADDR[4:0]=10100), 21 (ADDR[4:0]=10101), and 22 (ADDR[4:0]=10110) contain the static control bits that control the operation of the GF9105A. Note that even if only one control bit is to be altered, the entire word must be reprogrammed.

ADDRESSING OF SPLIT-UP COEFFICIENTS

ADDRESS	COEFFICIENT PORT ASSIGNMENT
ADDR[4:0] = N	COEFF_PORT[7] = b4 COEFF_PORT[6] = b3 COEFF_PORT[5] = b2 COEFF_PORT[4] = b1 COEFF_PORT[3] = b0 COEFF_PORT[2] = X (don't care) COEFF_PORT[1] = X (don't care) COEFF_PORT[0] = X (don't care)
ADDR[4:0] = N+1	COEFF_PORT[7] = b12 COEFF_PORT[6] = b11 COEFF_PORT[5] = b10 COEFF_PORT[4] = b9 COEFF_PORT[3] = b8 COEFF_PORT[2] = b7 COEFF_PORT[1] = b6 COEFF_PORT[0] = b5

MEMORY LOCATION ASSIGNMENTS FOR PROGRAMMING THE HOST INTERFACE

ADDRESS PORT	COEFFICIENT PORT ASSIGNMENT
ADDR[4:0] = 00000	COEFF_PORT[7:3] = CM_{11}[4:0]
ADDR[4:0] = 00001	COEFF_PORT[7:0] = CM_{11}[12:5]
ADDR[4:0] = 00010	COEFF_PORT[7:3] = CM_{12}[4:0]
ADDR[4:0] = 00011	COEFF_PORT[7:0] = CM_{12}[12:5]
ADDR[4:0] = 00100	COEFF_PORT[7:3] = CM_{13}[4:0]
ADDR[4:0] = 00101	COEFF_PORT[7:0] = CM_{13}[12:5]
ADDR[4:0] = 00110	COEFF_PORT[7:3] = CM_{21}[4:0]
ADDR[4:0] = 00111	COEFF_PORT[7:0] = CM_{21}[12:5]
ADDR[4:0] = 01000	COEFF_PORT[7:3] = CM_{22}[4:0]
ADDR[4:0] = 01001	COEFF_PORT[7:0] = CM_{22}[12:5]
ADDR[4:0] = 01010	COEFF_PORT[7:3] = CM_{23}[4:0]
ADDR[4:0] = 01011	COEFF_PORT[7:0] = CM_{23}[12:5]
ADDR[4:0] = 01100	COEFF_PORT[7:3] = CM_{31}[4:0]
ADDR[4:0] = 01101	COEFF_PORT[7:0] = CM_{31}[12:5]
ADDR[4:0] = 01110	COEFF_PORT[7:3] = CM_{32}[4:0]
ADDR[4:0] = 01111	COEFF_PORT[7:0] = CM_{32}[12:5]
ADDR[4:0] = 10000	COEFF_PORT[7:3] = CM_{33}[4:0]
ADDR[4:0] = 10001	COEFF_PORT[7:0] = CM_{33}[12:5]
ADDR[4:0] = 10010	COEFF_PORT[7:3] = KEY[4:0]
ADDR[4:0] = 10011	COEFF_PORT[7:0] = KEY[12:5]

MEMORY LOCATION ASSIGNMENTS FOR PROGRAMMING THE HOST INTERFACE

ADDRESS PORT	COEFFICIENT PORT ASSIGNMENT
ADDR[4:0] = 10100	COEFF_PORT[7] = OUTPUT/$\overline{\text{INPUT}}$ COEFF_PORT[6] = INT/$\overline{\text{DEC}}$ COEFF_PORT[5] = BYPASS_F COEFF_PORT[4] = $\overline{\text{MUXED\_IN}}$ COEFF_PORT[3] = $\overline{\text{MUXED\_OUT}}$ COEFF_PORT[2] = RND8/$\overline{10}$ COEFF_PORT[1] = FIL_RND COEFF_PORT[0] = 4:4:4:4/$\overline{\text{4:2:2:4}}$_OUT
ADDR[4:0] = 10101	COEFF_PORT[7] = HB_1 COEFF_PORT[6] = HB_0 COEFF_PORT[5] = IOA_1 COEFF_PORT[4] = IOA_0 COEFF_PORT[3] = OOA_1 COEFF_PORT[2] = OOA_0 COEFF_PORT[1] = CLP_D_1 COEFF_PORT[0] = CLP_D_0
ADDR[4:0] = 10110	COEFF_PORT[7] = GS9001 COEFF_PORT[6] = SL/$\overline{\text{DL}}$_IN COEFF_PORT[5] = SL/$\overline{\text{DL}}$_OUT COEFF_PORT[4] = S* COEFF_PORT[3] = 0 (RESERVED) COEFF_PORT[2] = HVF_OUT COEFF_PORT[1] = 0 (RESERVED) COEFF_PORT[0] = LOWF

With single link output data, the S control bit should be set LOW for GBR signals (S=0) and set HIGH for Y, C_B, C_R signals (S=1).

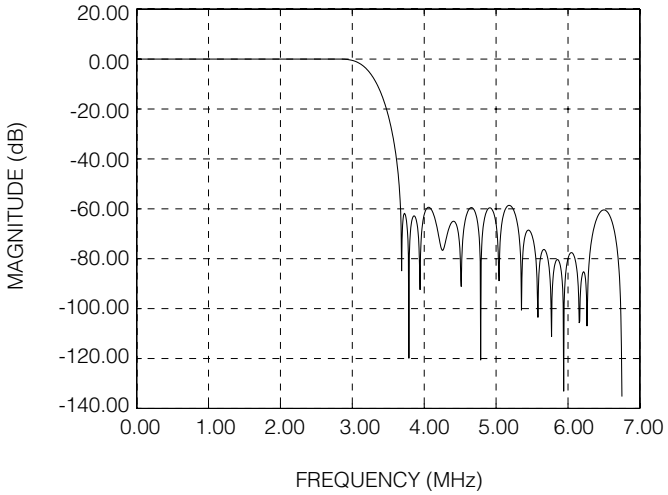


Fig. 6a Interpolation/Decimation filter Frequency Response
(Sampling at 13.5 MHz)

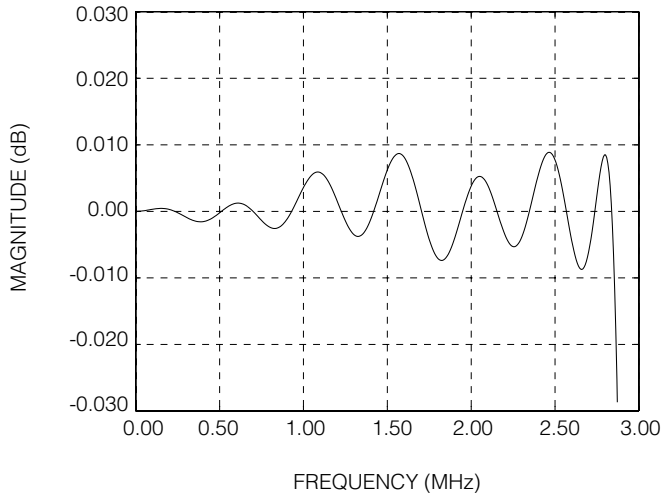


Fig. 6b Interpolation/Decimation Filter Pass band
(Sampling at 13.5 MHz)

PARAMETER	VALUE
Filter Order	57
Pass Band Ripple	< ±0.0089 dB
Pass Band Edge	2.850 MHz
DC Gain	0.000 dB
3.375 MHz (f_S/4) Attenuation	12.058 dB
Minimum Stop Band Attenuation	58.615 dB
Stop Band Edge	3.669 MHz

Fig. 6c Interpolation/Decimation filter Characteristics at Sampling Frequency of 13.5 MHz

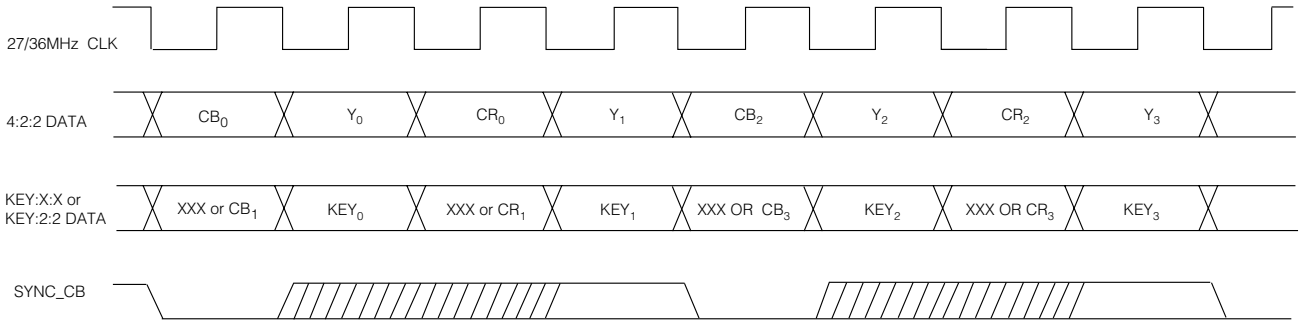


Fig. 7a Timing of SYNC_CB Signal with Dual Link 4:2:2:4 or Dual Link 4:4:4:4 Input Data

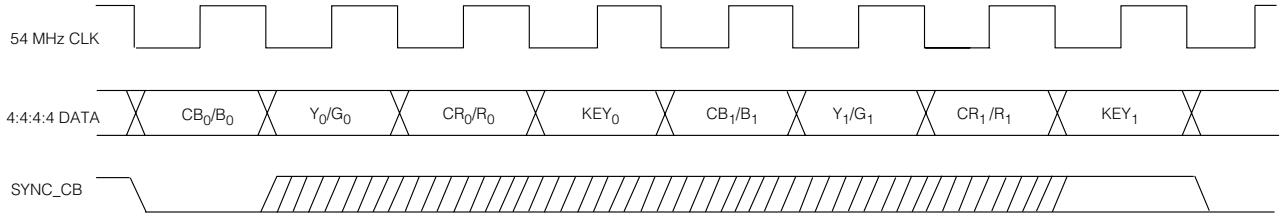


Fig. 7b Timing of SYNC_CB Signal with Single Link Multiplexed 4:4:4:4 Input Data

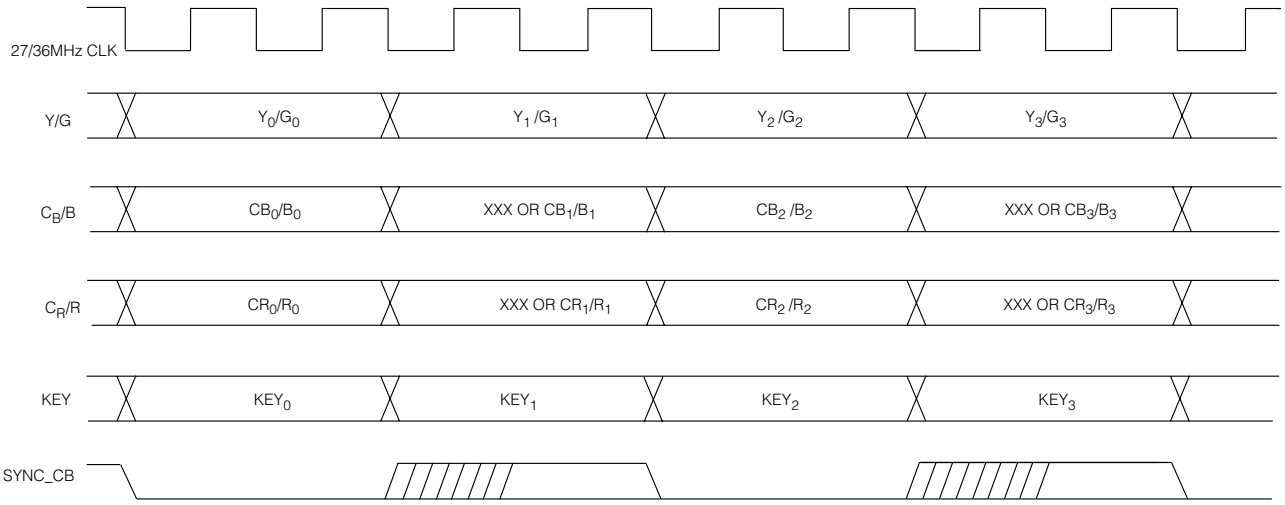


Fig. 7c Timing of SYNC_CB Signal with Non-Multiplexed 4:2:2:4 or 4:4:4:4 Input Data

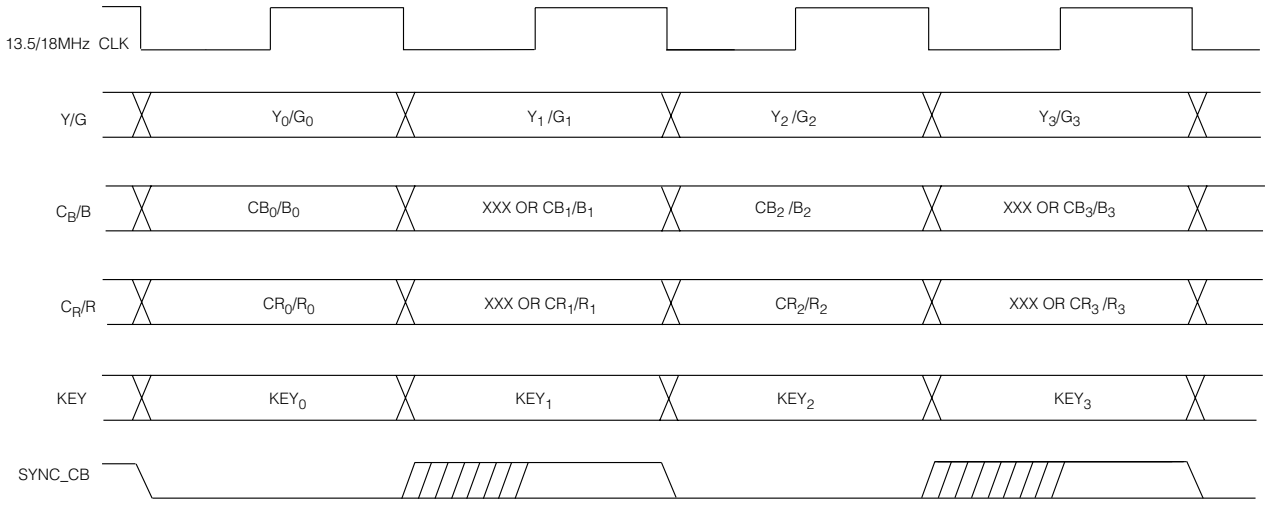


Fig. 7d Timing of SYNC_CB Signal with Non-Multiplexed 4:2:2:4 or 4:4:4:4 Input Data (Low Frequency Mode)

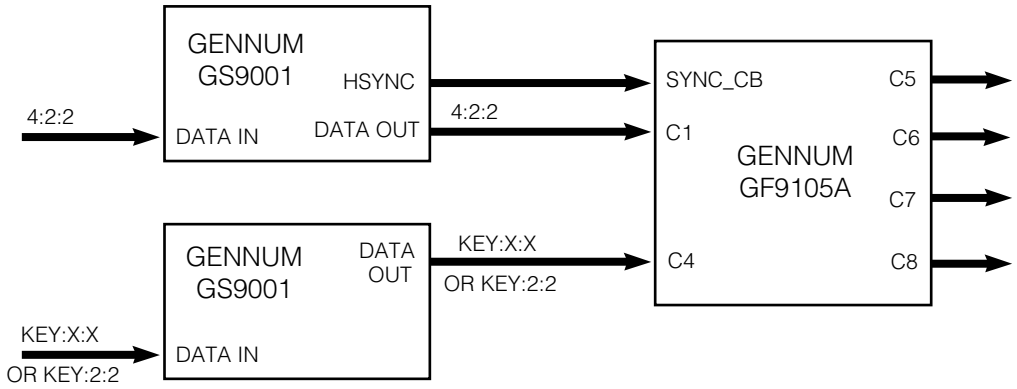


Fig. 8a GF9105A Optionally Coupled to the GS9001 EDH Coprocessor for Multiplexed Input and Non-Multiplexed Output Data, GS9001 Control Bit set High

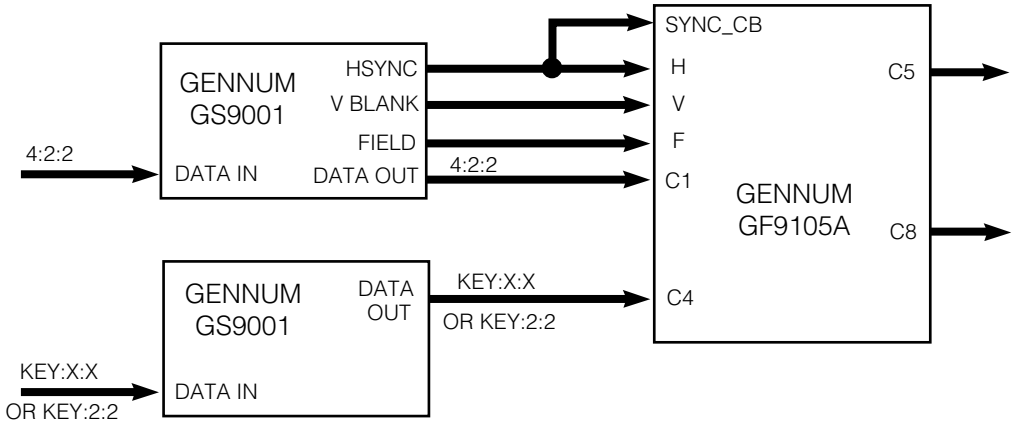


Fig. 8b GF9105A Optionally Coupled to the GS9001 EDH Coprocessor for Multiplexed Input and Output Data, GS9001 Control Bit set High

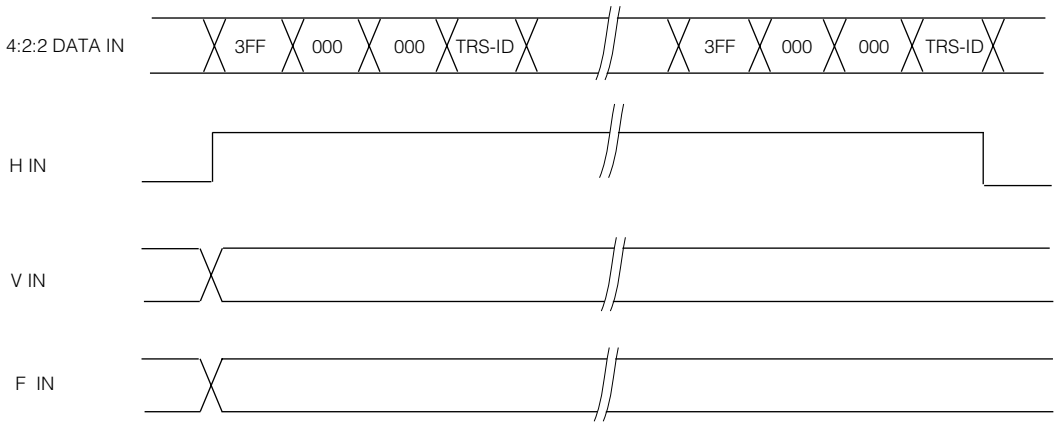
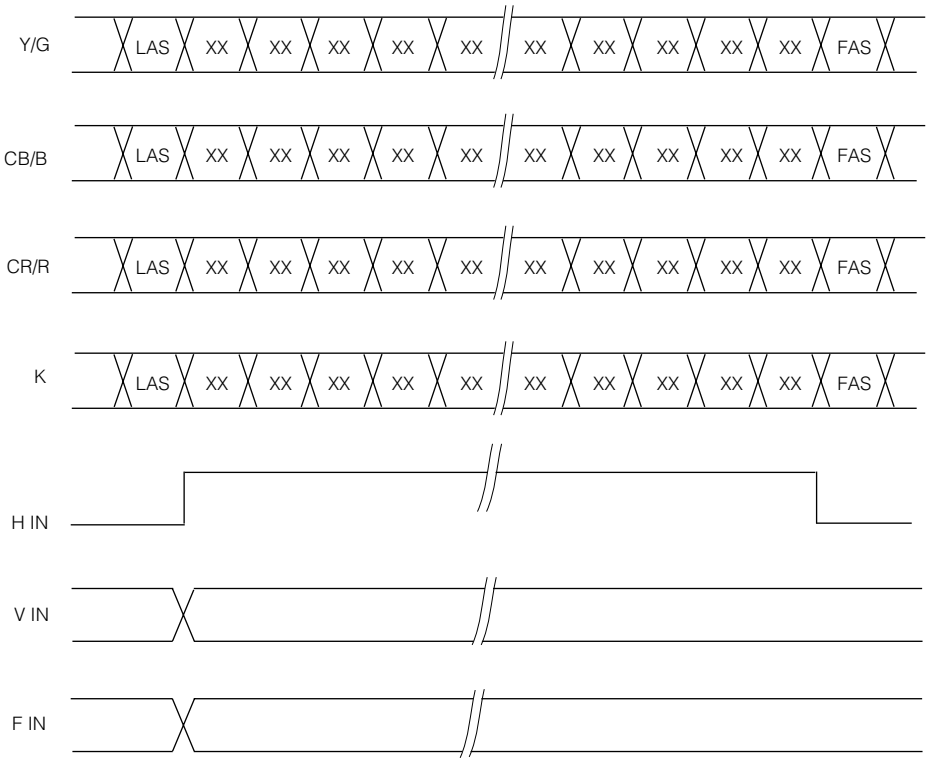


Fig. 9a Relative Timing of Multiplexed Input Data and H, V and F Inputs (GS9001 = 0)



LAS = Last Active Sample
FAS = First Active Sample

Fig. 9b Relative Timing of Non-Multiplexed Input Data and H, V and F Inputs

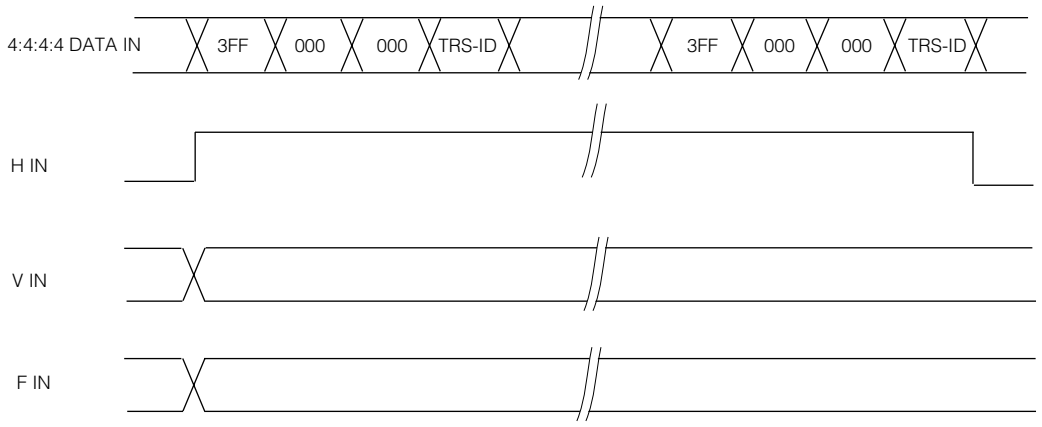


Fig. 9c Relative Timing of Single Link Input Data and H, V and F Inputs

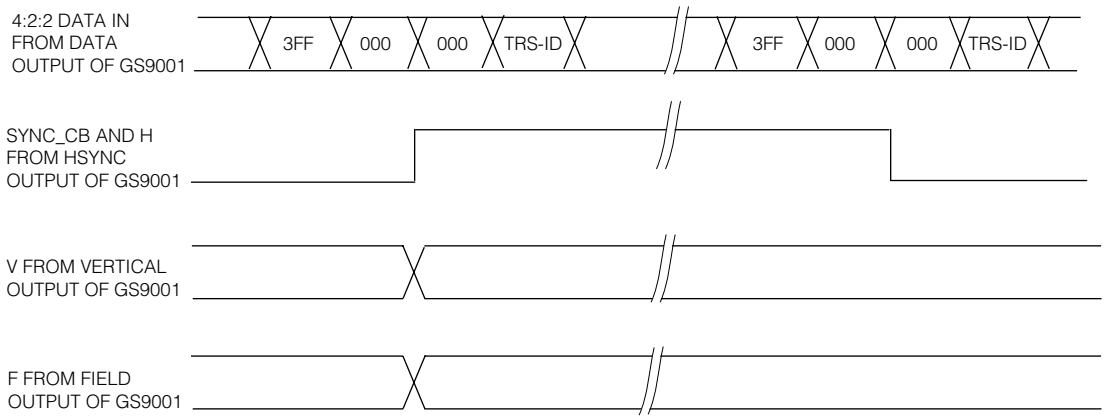


Fig. 9d Relative Timing of Data, SYNC_CB, H, V and F Inputs (GS9001 = 1)

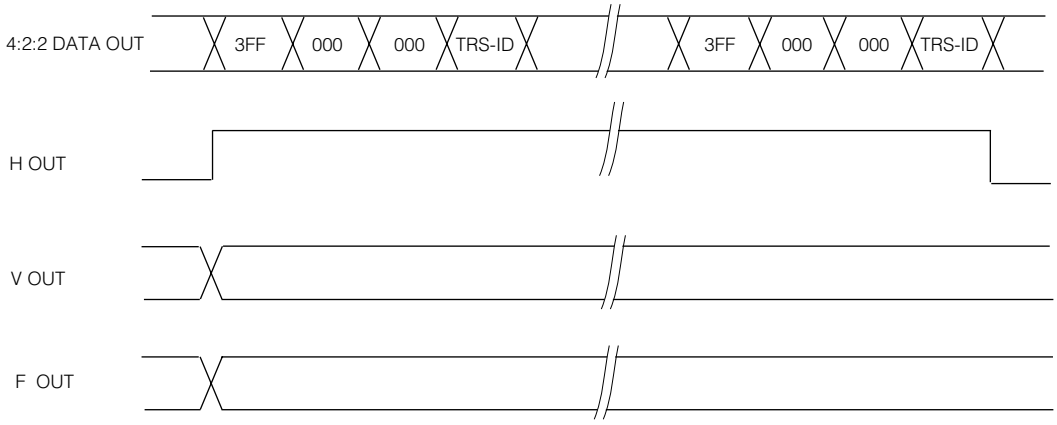


Fig. 9e Relative Timing of Dual Link 4:2:2:4 or Dual Link 4:4:4:4 Multiplexed Output Data and H, V and F Output Signals

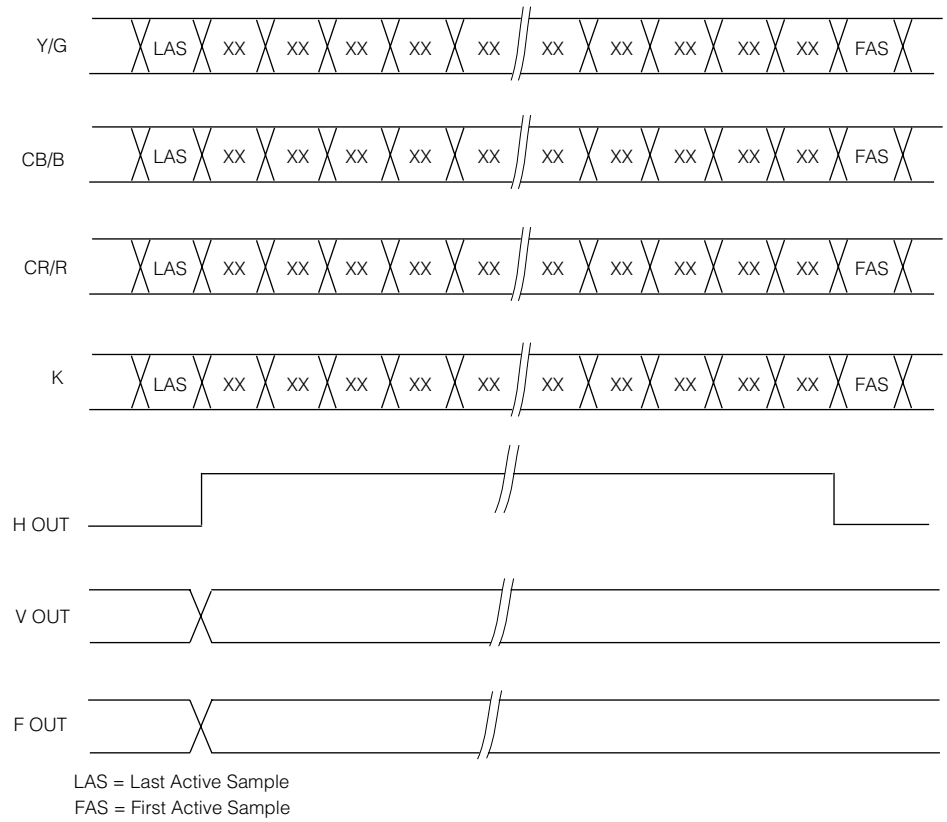


Fig. 9f Relative Timing of Non-Multiplexed Output Data and H, V and F Output Signals

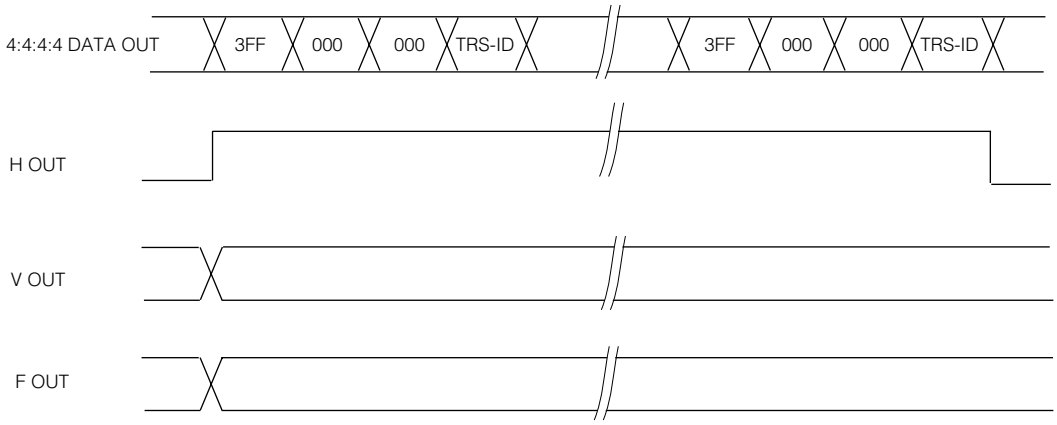


Fig. 9g Relative Timing of Single Link 4:4:4:4 Multiplexed Output Data and H, V and F Output Signals

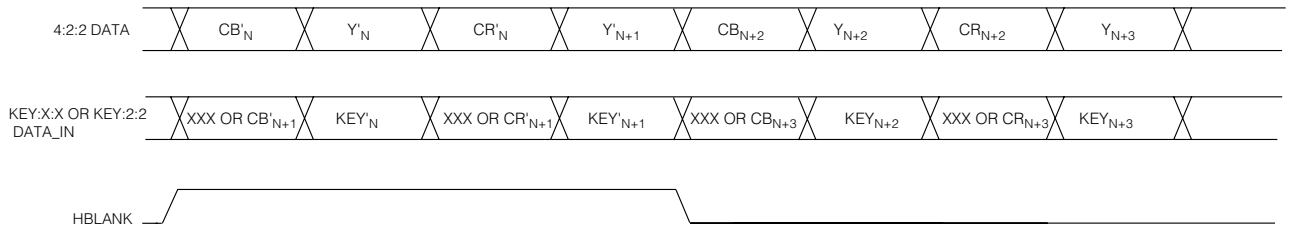


Fig. 10a Typical Timing of H_BLANK Signal with Dual Link Multiplexed 4:2:2:4 or 4:4:4:4 Input Data

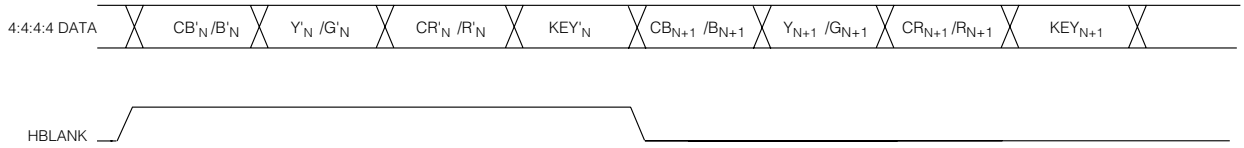


Fig. 10b Typical Timing of H_BLANK Signal with Single Link Multiplexed 4:4:4:4 Input Data

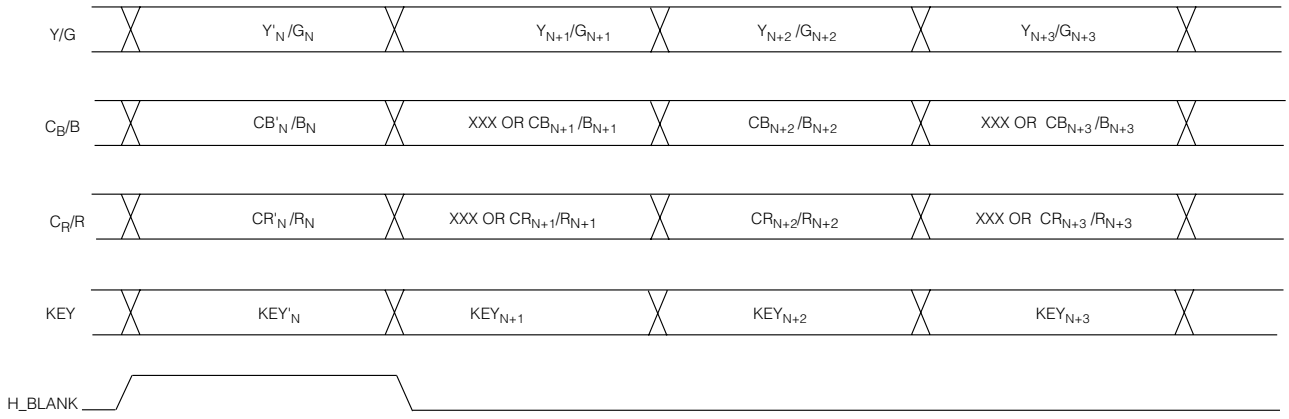


Fig. 10c Typical Timing of H_BLANK Signal with Non-Multiplexed 4:2:2:4 or 4:4:4:4 Input Data

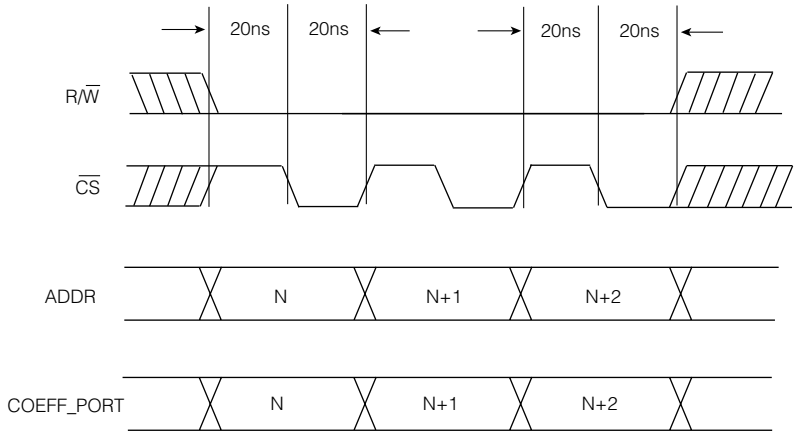


Fig. 11a Standard Host Interface Timing for Writing to the GF9105A

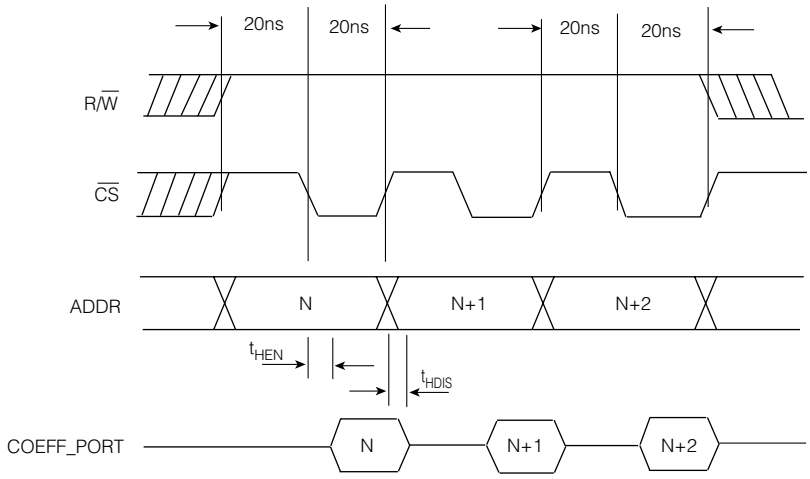


Fig. 11b Standard Host Interface Timing for Reading from the GF9105A

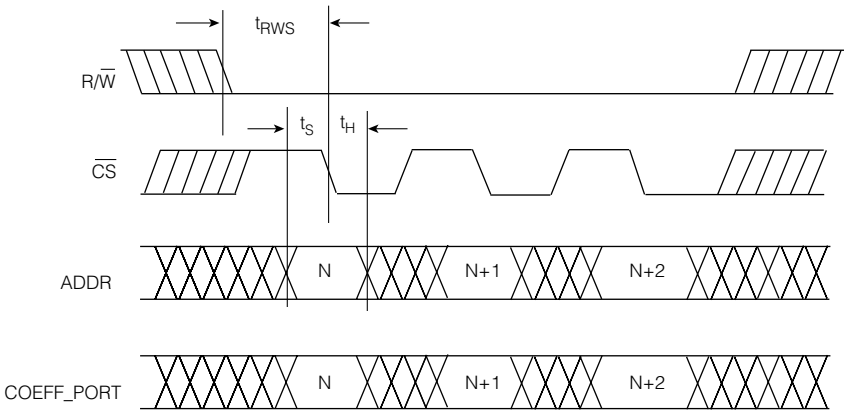


Fig. 12a Advanced Host Interface Timing for Writing to the GF9105A

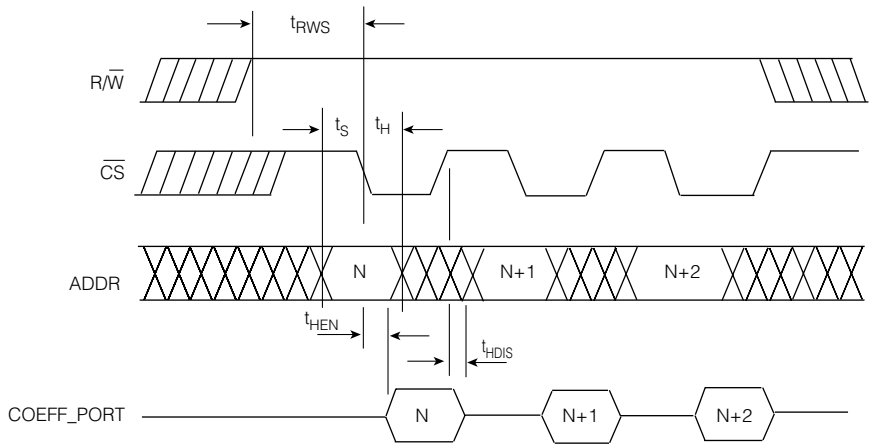


Fig. 12b Advanced Host Interface Timing for Reading from the GF9105A

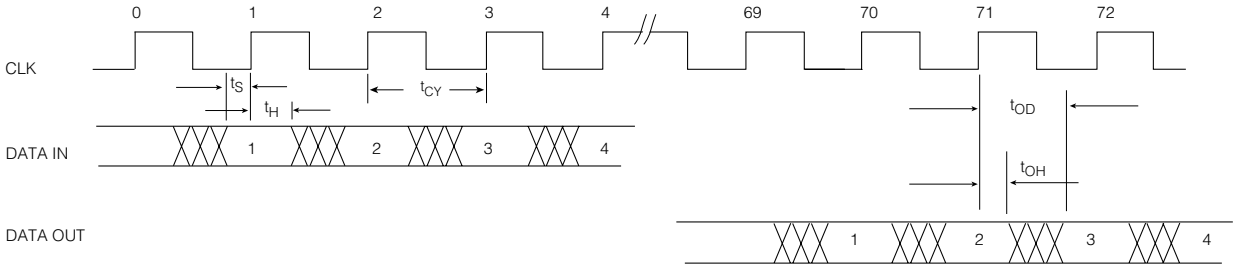


Fig. 13 Illustration of Device Latency and I/O Timing

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage (V_{DD})	-0.3 to +7.0 V
Input Voltage Range (any input)	-0.5 V to (V_{DD}+0.5) V
Operating Temperature Range	0°C to 70°C 0 MHz <= f_{CLK} <= 54MHz
Storage Temperature Range	-65°C <= T_S <= 150°C
Lead Temperature (soldering, 10 seconds)	260°C

ELECTRICAL CHARACTERISTICS

Conditions: V_{DD} = 5 V, T_A = 0° to 70° C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current Quiescent	I_{DDQ}	V_{DD} = Max, V_{IN} = 0V	-	0.5		mA
Supply Current Unloaded	I_{DDU}	V_{DD} = Max, $\overline{DP\_EN}$ = V_{DD}, f = 27 MHz	-	73	-	mA
Input Voltage, Logic Low	V_{IL}		-	-	0.8	V
Input Voltage, Logic High	V_{IH}		2	-	-	V
Output Voltage, Logic Low	V_{OL}	V_{DD} = Min, I_{OL} = 2 mA	-	-	0.4	V
Output Voltage, Logic High	V_{OH}	V_{DD} = Min, I_{OH} = -2 mA	2.4	-	-	V
Input Capacitance	C_{IN}	T_A = 25°C, f = 1 MHz	-	-	10	pF
Output Capacitance	C_{OUT}	T_A = 25°C, f = 1MHz	-	-	10	pF

SWITCHING CHARACTERISTICS

Conditions: V_{DD} = 5 V, T_A = 0° to 70° C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Setup Time	t_S		6	-	-	ns
Input Hold Time	t_H		2	-	-	ns
Output Delay Time	t_{OD}	V_{DD} = Min, C_L = 25 pF	-	-	13	ns
Output Hold Time	t_{OH}	V_{DD} = Max, C_L = 25 pF	4	-	-	ns
Output Enable Time	t_{EN}	V_{DD} = Min, C_L = 25 pF	-	-	12	ns
Output Disable Time	t_{DIS}	V_{DD} = Min, C_L = 25 pF	-	-	12	ns
Host Interface R/$\overline{W}$ Setup Time	t_{RWS}		20	-	-	ns
Host Interface Output Enable Time	t_{HEN}	V_{DD} = Min, C_L = 25 pF	-	-	12	ns
Host Interface Output Disable Time	t_{HDIS}	V_{DD} = Max, C_L = 25 pF	-	-	12	ns

SWITCHING CHARACTERISTICS

Conditions: V_{DD} = 5 V, T_A = 0° to 70° C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Cycle Time	t_{CY}	Non-Multiplexed Input Data AND Non-Multiplexed Output Data LOWF=1	55	-	-	ns
		All Input/Output Data Formats Except Single Link	27	-	-	ns
		SMPTE RP174 Single Link Input OR Output Data	18	-	-	ns
Clock Pulse Width Low	t_{PWL}	As a percentage of Min. Clock Cycle Time	40	-	60	%
Clock Pulse Width High	t_{PWH}	As a percentage of Min. Clock Cycle Time	40	-	60	%
Device Latency[1]		Low Frequency Mode (LOWF = 1)	34	34	34	clks
		Dual link input and output data	68	68	68	clks
		Single link input or output data	136	136	136	clks

Note 1: Latency is defined as the number of clock cycles between the time when the data is latched into the device and when the corresponding output data is clocked out of the device. Refer to Figure 13.

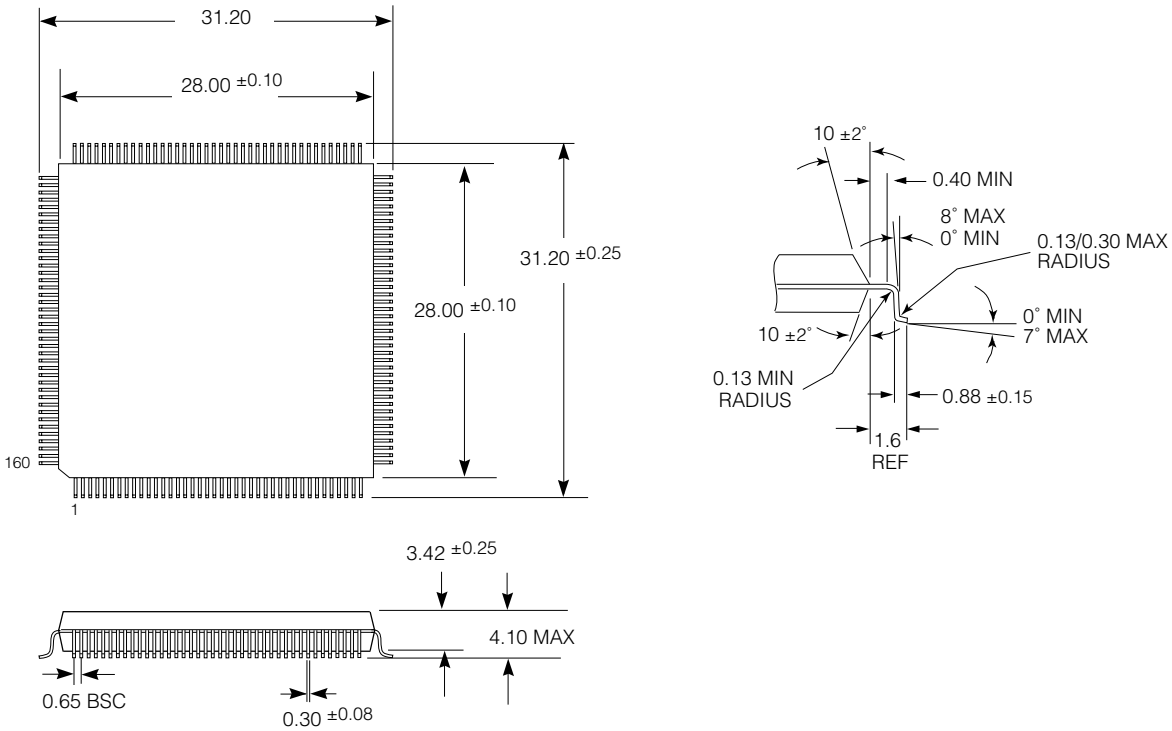


Fig. 14 160 Pin MQFP

CAUTION

ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION

DATA SHEET

The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

REVISION NOTES:

Updated Input Clock (CLK) information.

For latest product information, visit www.gennum.com

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