MCP6546/7/8/9

Open-Drain Output Sub-Microamp Comparators

Features

- Low Quiescent Current: 600 nA/comparator (typ.)
- Rail-to-Rail Input: V_{SS} - 0.3V to V_{DD} + 0.3V
- Open-Drain Output: V_{OUT} ≤10V
- Propagation Delay 4 µs (typ.)
- Wide Supply Voltage Range: 1.6V to 5.5V
- Single available in SOT-23-5, SC-70-5 packages
- Available in Single, Dual and Quad
- Chip Select ($\overline{CS}$) with MCP6548
- Low Switching Current
- Internal Hysteresis: 3.3 mV (typ.)
- Industrial Temperature: -40°C to +85°C

Typical Applications

- Laptop Computers
- Mobile Phones
- Metering Systems
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Windowed Comparators
- Multi-vibrators

Related Devices

- CMOS/TTL-Compatible Output: MCP6541/2/3/4

Description

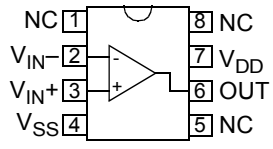
The Microchip Technology Inc. MCP6546/7/8/9 family of comparators is offered in single (MCP6546), single with chip select (MCP6548), dual (MCP6547) and quad (MCP6549) configurations. The outputs are open-drain and are capable of driving heavy DC or capacitive loads.

These comparators are optimized for low power, single-supply application with greater than rail-to-rail input operation. The output limits supply current surges and dynamic power consumption while switching. The open-drain output of the MCP6546/7/8/9 family can be used as a level-shifter for up to 10V using a pull-up resistor. It can also be used as a wired-OR logic. The internal Input hysteresis eliminates output switching due to internal noise voltage, reducing current draw. These comparators operate with a single-supply voltage as low as 1.6V and draw less than 1 µA/comparator of quiescent current.

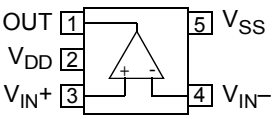
The related MCP6541/2/3/4 family of comparators from Microchip has a push-pull output that supports rail-to-rail output swing and interfaces with CMOS/TTL logic.

Package Types

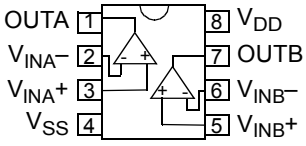
MCP6546
PDIP, SOIC, MSOP



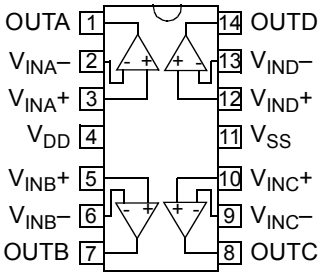
MCP6546-R
SOT-23-5



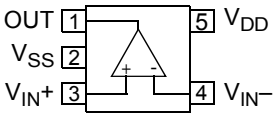
MCP6547
PDIP, SOIC, MSOP



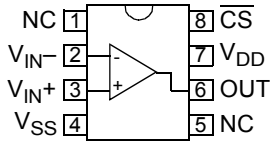
MCP6549
PDIP, SOIC, TSSOP



MCP6546
SOT-23-5, SC-70-5



MCP6548
PDIP, SOIC, MSOP



1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V
Open-Drain output..... V_{SS} +10.5V
All inputs and outputs ..... V_{SS} –0.3V to V_{DD} +0.3V
Difference Input voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current .....continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage temperature .....-65°C to +150°C
Maximum Junction Temperature (T_J) .....+150°C
ESD protection on all pins (HBM;MM).....4 kV;200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

NAME	FUNCTION
V_{IN}+, V_{INA}+, V_{INB}+, V_{INC}+, V_{IND}+	Non-Inverting Inputs
V_{IN}–, V_{INA}–, V_{INB}–, V_{INC}–, V_{IND}–	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
OUT, OUTA, OUTB, OUTC, OUTD	Outputs
$\overline{CS}$	Chip Select
NC	Not Connected

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = V_{SS}, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD} (Refer to Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.6	—	5.5	V	
Quiescent Current per comparator	I_Q	0.3	0.6	1	µA	I_{OUT} = 0
Input						
Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 5.3V
Common Mode Rejection Ratio	CMRR	50	65	—	dB	V_{DD} = 5V, V_{CM} = 2.5V to 5.3V
Common Mode Rejection Ratio	CMRR	55	70	—	dB	V_{DD} = 5V, V_{CM} = -0.3V to 2.5V
Power Supply Rejection Ratio	PSRR	63	80	—	dB	V_{CM} = V_{SS}
Input Offset Voltage	V_{OS}	-7.0	±1.5	+7.0	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3	—	µV/°C	T_A = -40°C to +85°C, V_{CM} = V_{SS}
Input Hysteresis Voltage	V_{HYST}	1.5	3.3	6.5	mV	V_{CM} = V_{SS} **(Note 1)**
Drift with Temperature	$\Delta V_{HYST}/\Delta T_A$	—	10	—	µV/°C	T_A = -40°C to +25°C, V_{CM} = V_{SS}
Drift with Temperature	$\Delta V_{HYST}/\Delta T_A$	—	5	—	µV/°C	T_A = +25°C to +85°C, V_{CM} = V_{SS}
Input Bias Current	I_B	—	1	—	pA	V_{CM} = V_{SS}
Over Temperature	I_B	—	—	100	pA	T_A = -40°C to +85°C, V_{CM} = V_{SS} **(Note 3)**
Input Offset Current	I_{OS}	—	±1	—	pA	V_{CM} = V_{SS}
Common Mode Input Impedance	Z_{CM}	—	10^{13}||4	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Open-Drain Output						
Output Pull-Up Voltage	V_{PU}	V_{DD}	—	10	V	(**Note 2**)
High-Level Output Current	I_{OH}	-100	—	—	nA	V_{DD} = 1.6V to 5.5V, V_{PU} = 10V **(Note 2)**
Low-Level Output Voltage	V_{OL}	V_{SS}	—	V_{SS} + 0.2	V	I_{OUT} = 2 mA, V_{PU} = V_{DD} = 5V
Short-Circuit Current	I_{SC}	—	±50	—	mA	V_{PU} = V_{DD} = 5.0V **(Note 2)**
Output Pin Capacitance	C_{OUT}	—	8	—	pF	

Note 1: The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: Do not short the output above V_{SS} + 10V. Limit the output current to Absolute Maximum Rating of 30 mA. The comparator does not function properly when V_{PU} < V_{DD}.

3: Input bias current overtemperature is not tested for the SC-70-5 package.

AC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, Step = 200 mV, Overdrive = 100 mV, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF (Refer to Figure 1-2 and Figure 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Fall Time	t_F	—	0.7	—	µs	**(Note 1)**
Propagation Delay (High-to-Low)	t_{PHL}	—	4.0	8.0	µs	
Propagation Delay (Low-to-High)	t_{PLH}	—	3.0	8.0	µs	**(Note 1)**
Propagation Delay Skew	t_{PDS}	—	-1.0	—	µs	**(Notes 1 and 2)**
Maximum Toggle Frequency	f_{MAX}	—	225	—	kHz	V_{DD} = 1.6V
	f_{MAX}	—	165	—	kHz	V_{DD} = 5.5V
Input Noise Voltage	E_N	—	200	—	μV_{P-P}	10 Hz to 100 kHz

Note 1: t_R and t_{PLH} depend on the load (R_L and C_L); these specifications are valid for the indicated load only.

2: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

SPECIFICATIONS FOR MCP6548 CHIP SELECT

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = V_{SS}, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF (Refer to Figures 1-1 and 1-3).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	5	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	1	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, V_{DD} Current	I_{DD}	—	18	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Input High, GND Current	I_{SS}	—	-20	—	pA	$\overline{CS}$ = V_{DD}
Comparator Output Leakage	$I_{O(LEAK)}$	—	1	—	pA	V_{OUT} = V_{SS}+10V
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Comparator Output Low Turn-on Time	t_{ON}	—	2	50	ms	$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = V_{DD}/2, V_{IN}– = V_{DD}
$\overline{CS}$ High to Comparator Output High Z Turn-off Time	t_{OFF}	—	10	—	µs	$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = V_{DD}/2, V_{IN}– = V_{DD}
$\overline{CS}$ Hysteresis	V_{CS_HYST}	—	0.6	—	V	V_{DD} = 5V

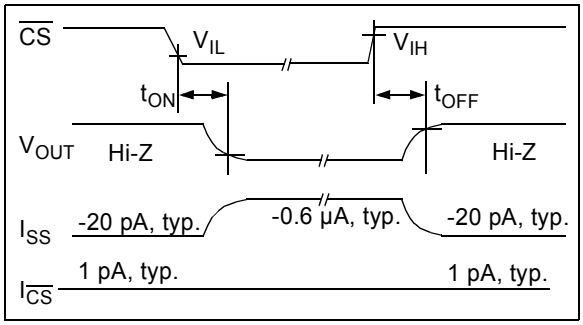


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ pin on the MCP6548.*

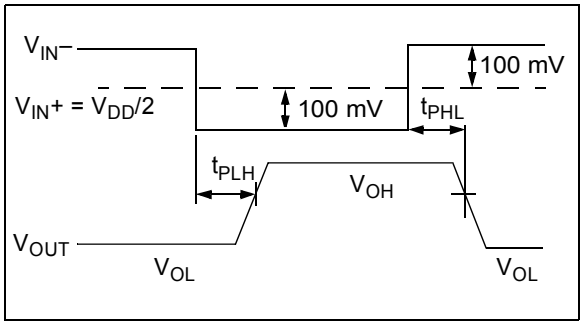


FIGURE 1-2: *Propagation Delay Timing Diagram.*

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.6V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC-70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The MCP6546/7/8/9 operates over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.2 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

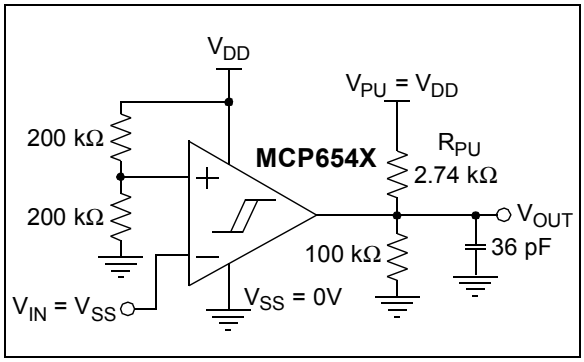


FIGURE 1-3: *AC and DC Test circuit for the open- drain output comparators.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

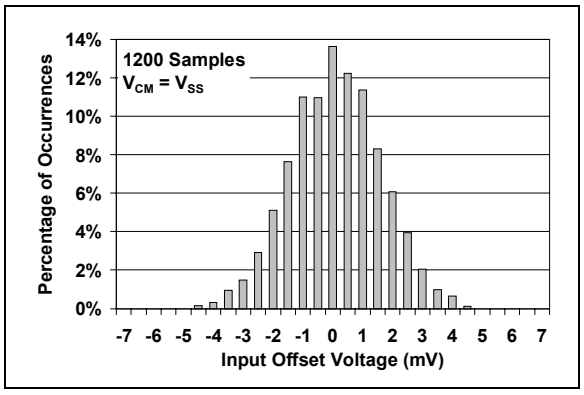


FIGURE 2-1: *Input Offset Voltage Histogram at $V_{CM} = V_{SS}$.*

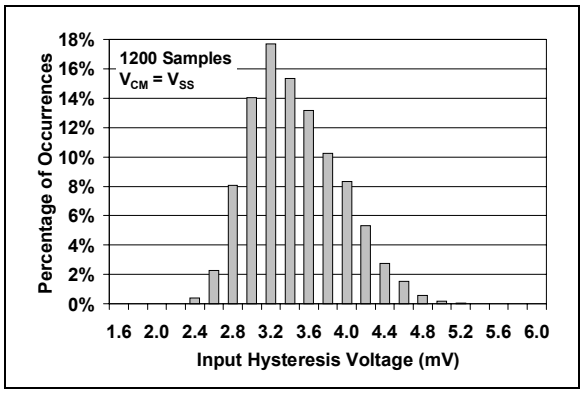


FIGURE 2-4: *Input Hysteresis Voltage Histogram at $V_{CM} = V_{SS}$.*

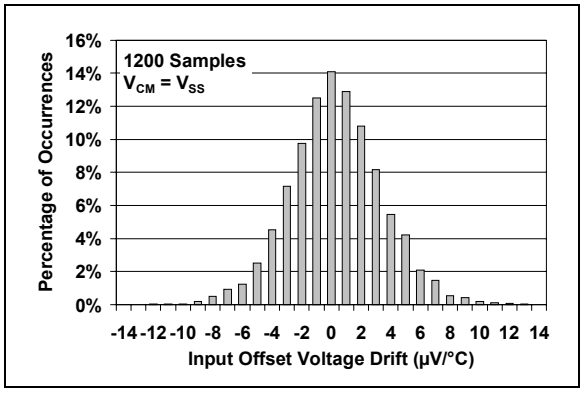


FIGURE 2-2: *Input Offset Voltage Drift Histogram at $V_{CM} = V_{SS}$.*

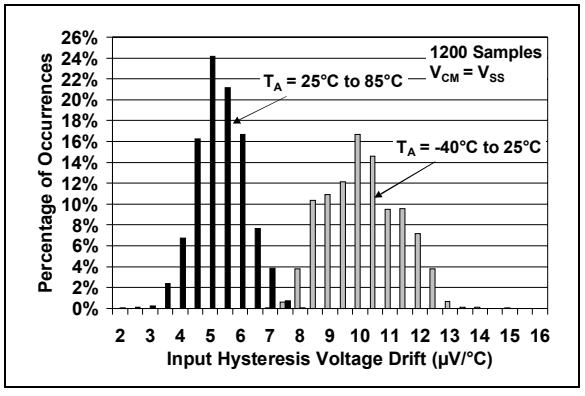


FIGURE 2-5: *Input Hysteresis Voltage Drift Histogram.*

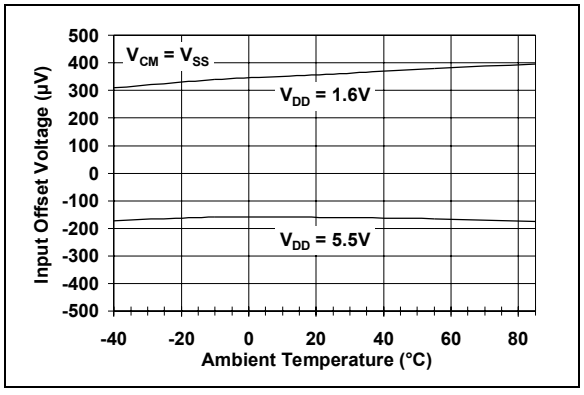


FIGURE 2-3: *Input Offset Voltage vs. Ambient Temperature at $V_{CM} = V_{SS}$.*

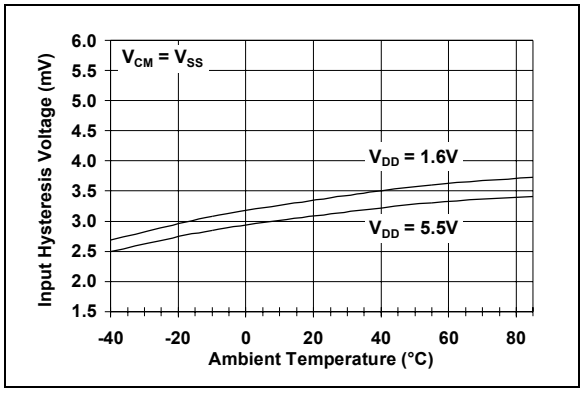


FIGURE 2-6: *Input Hysteresis Voltage vs. Ambient Temperature at $V_{CM} = V_{SS}$.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

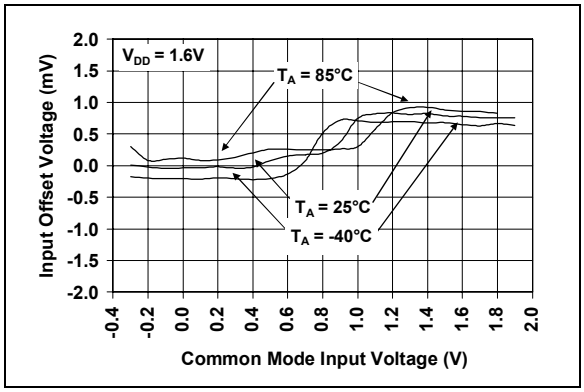


FIGURE 2-7: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

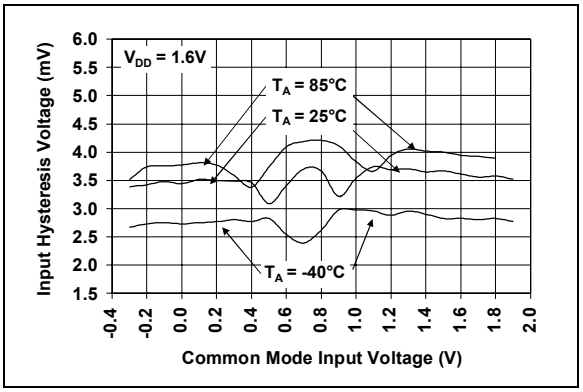


FIGURE 2-10: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

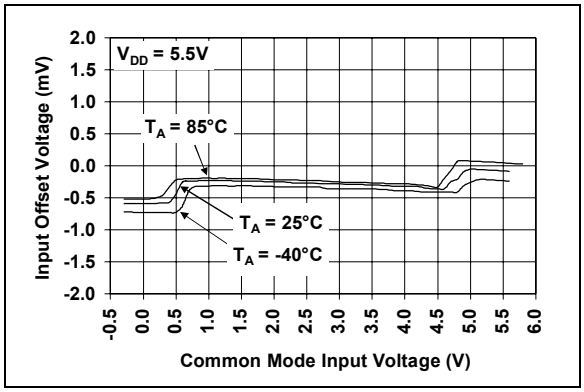


FIGURE 2-8: *Input Offset Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

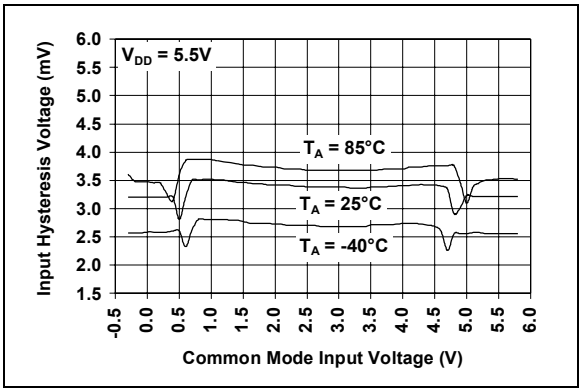


FIGURE 2-11: *Input Hysteresis Voltage vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

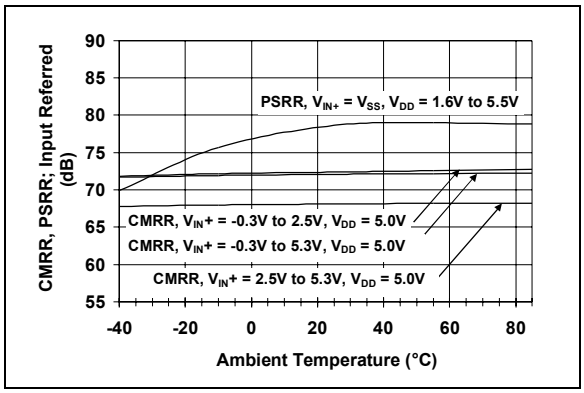


FIGURE 2-9: *CMRR, PSRR vs. Ambient Temperature at V_{CM} = V_{SS}.*

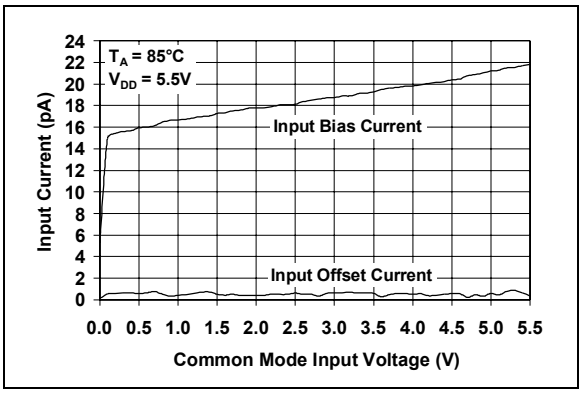


FIGURE 2-12: *Input Bias Current, Input Offset Current vs. Common Mode Input Voltage at +85°C.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

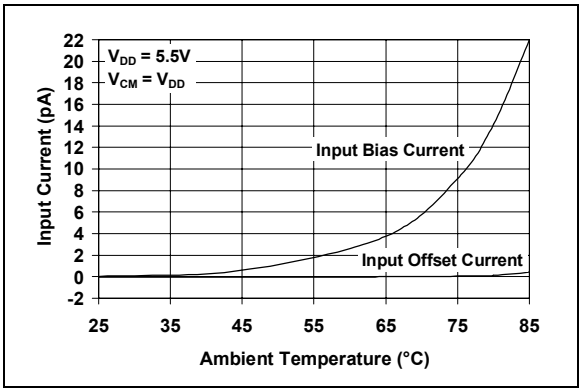


FIGURE 2-13: *Input Bias Current, Input Offset Current vs. Ambient Temperature.*

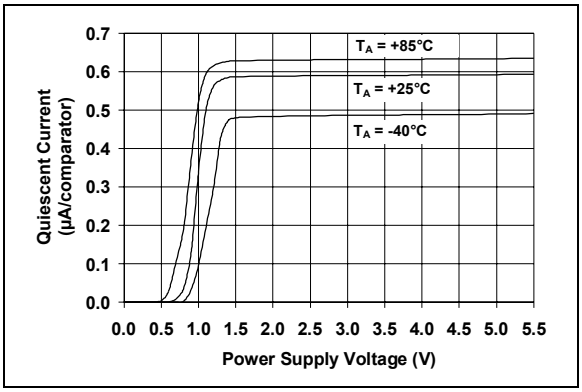


FIGURE 2-16: *Quiescent Current vs. Power Supply Voltage.*

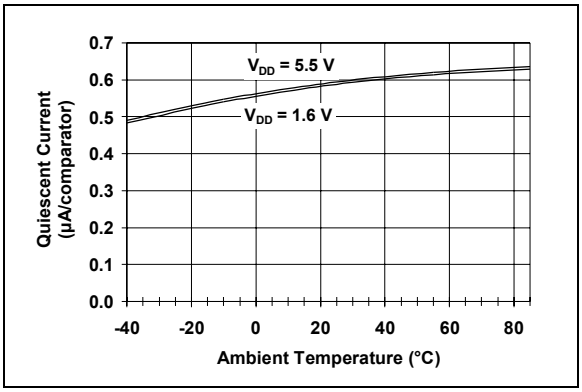


FIGURE 2-14: *Quiescent Current vs. Ambient Temperature vs. Power Supply Voltage.*

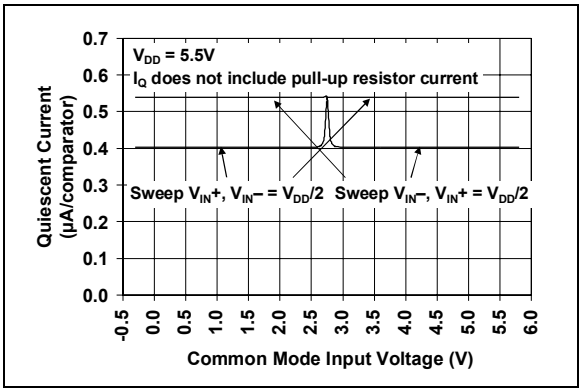


FIGURE 2-17: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 5V.*

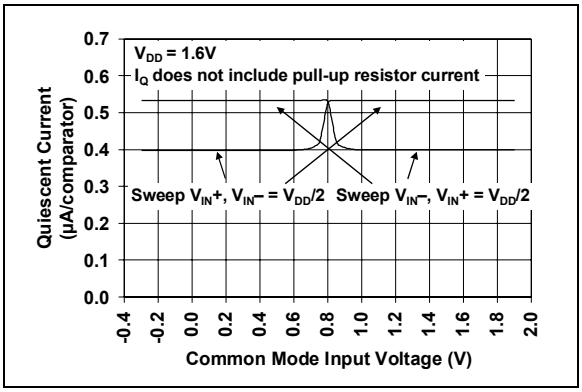


FIGURE 2-15: *Quiescent Current vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

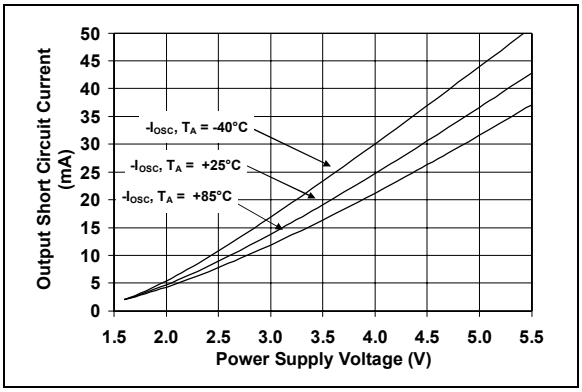


FIGURE 2-18: *Output Short-Circuit Current vs. Power Supply Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

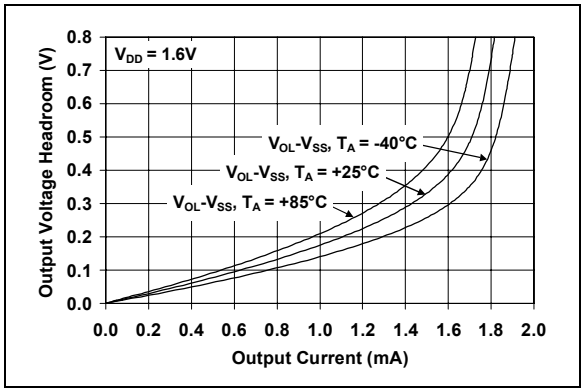


FIGURE 2-19: *Output Voltage Headroom vs. Output Current at V_{DD} = 1.6V.*

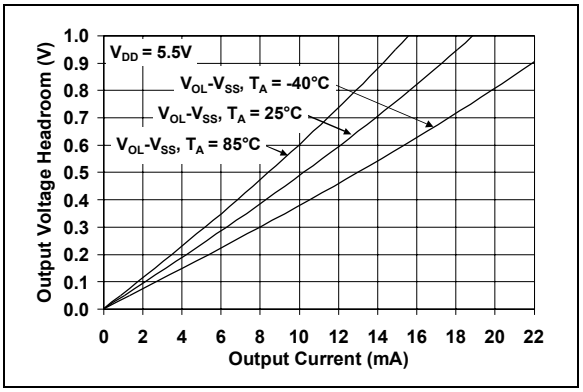


FIGURE 2-22: *Output Voltage Headroom vs. Output Current at V_{DD} = 5.5V.*

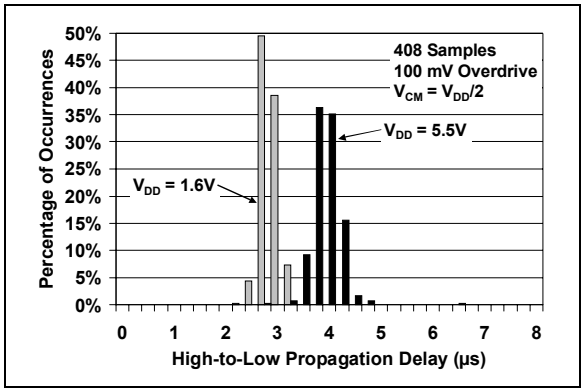


FIGURE 2-20: *High-to-Low Propagation Delay Histogram.*

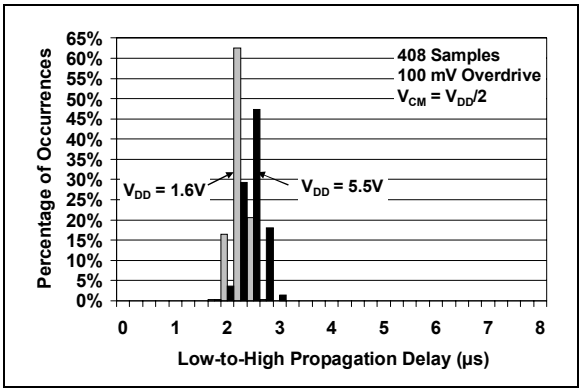


FIGURE 2-23: *Low-to-High Propagation Delay Histogram.*

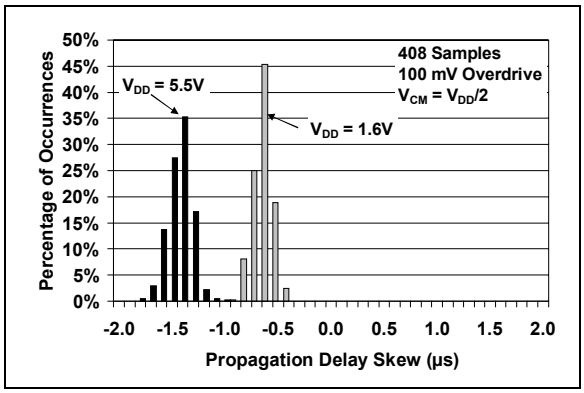


FIGURE 2-21: *Propagation Delay Skew Histogram.*

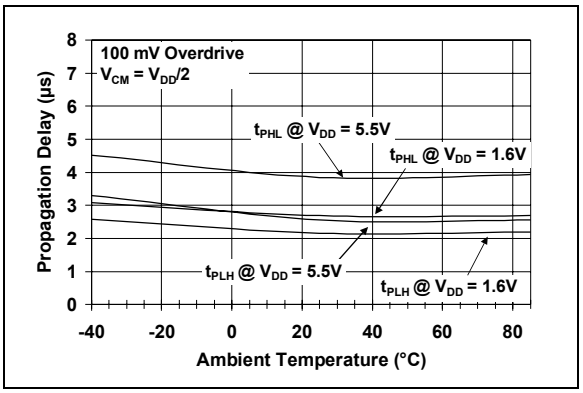


FIGURE 2-24: *Propagation Delay vs. Ambient Temperature.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_{PU} = 2.74 kΩ to V_{PU} = V_{DD}, and C_L = 36 pF.

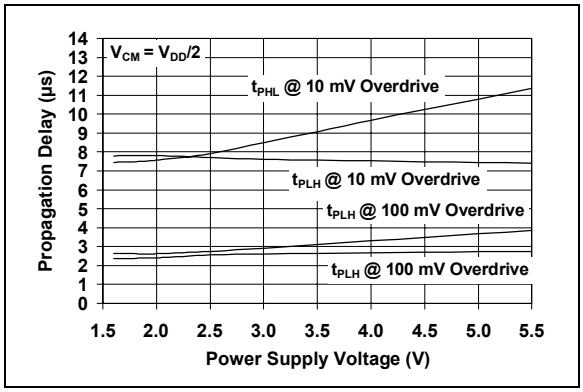


FIGURE 2-25: *Propagation Delay vs. Power Supply Voltage.*

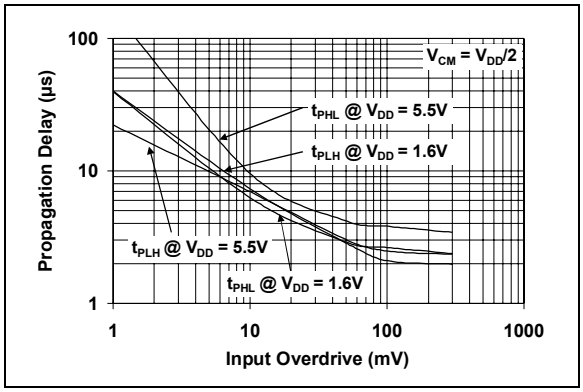


FIGURE 2-28: *Propagation Delay vs. Input Overdrive.*

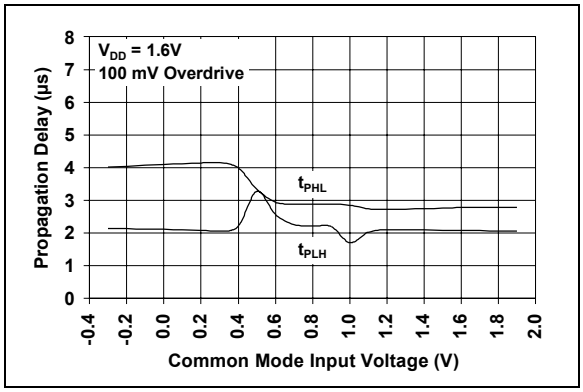


FIGURE 2-26: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 1.6V.*

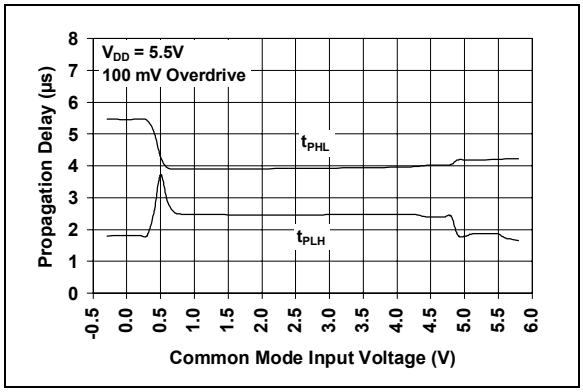


FIGURE 2-29: *Propagation Delay vs. Common Mode Input Voltage at V_{DD} = 5.5V.*

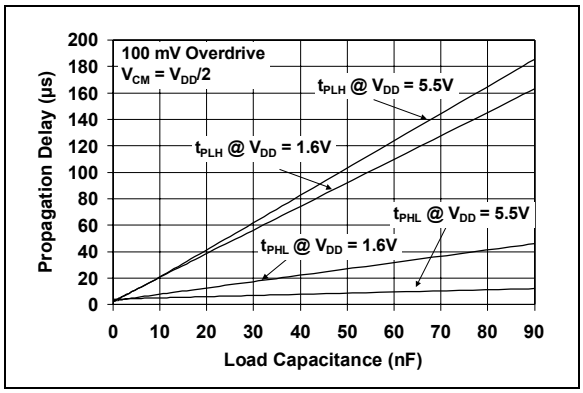


FIGURE 2-27: *Propagation Delay vs. Load Capacitance.*

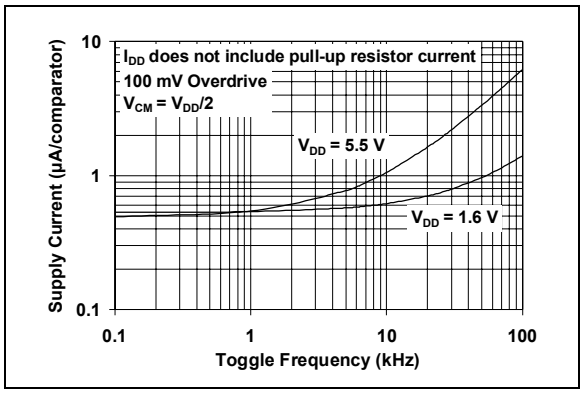


FIGURE 2-30: *Supply Current vs. Toggle Frequency.*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

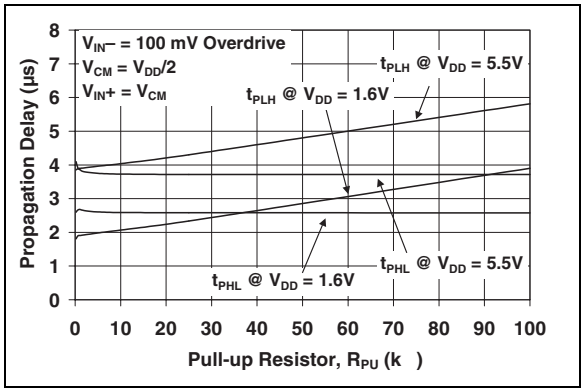


FIGURE 2-31: *Propagation Delay vs. Pull-up Resistor.*

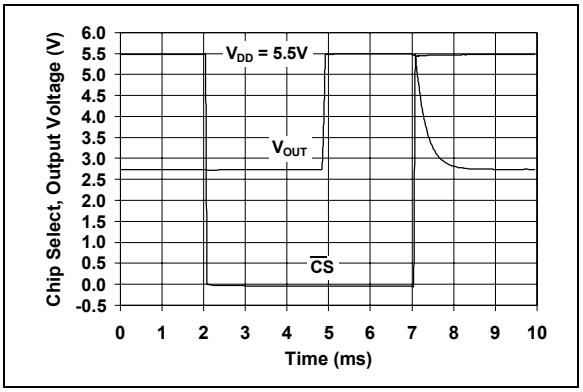


FIGURE 2-34: *Chip Select ($\overline{CS}$) Step Response (MCP6548 only).*

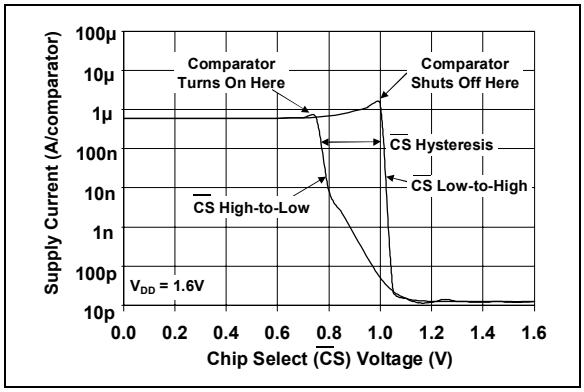


FIGURE 2-32: *Supply Current (shoot through current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 1.6V (MCP6548 only).*

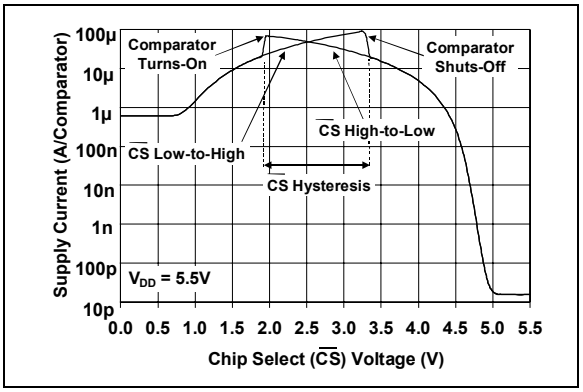


FIGURE 2-35: *Supply Current (shoot through current) vs. Chip Select ($\overline{CS}$) Voltage at V_{DD} = 5.5V (MCP6548 only).*

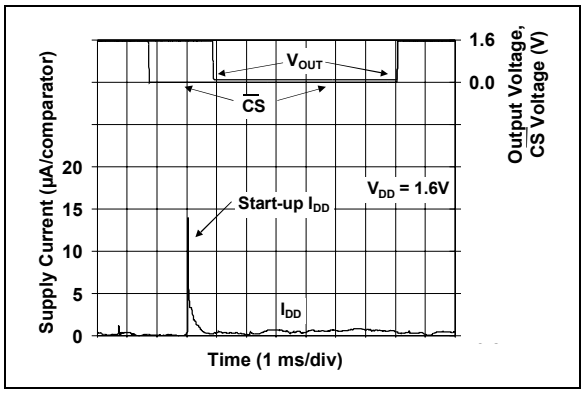


FIGURE 2-33: *Supply Current (charging current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 1.6V (MCP6548 only).*

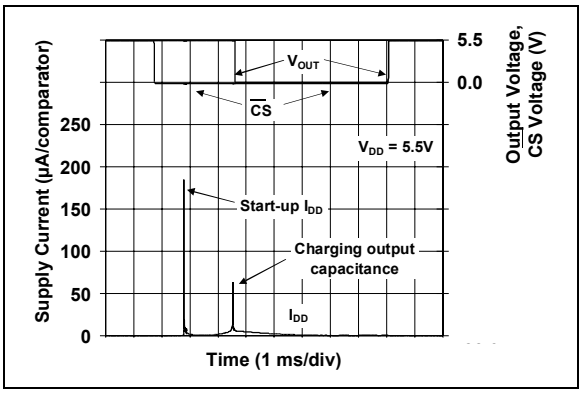


FIGURE 2-36: *Supply Current (charging current) vs. Chip Select ($\overline{CS}$) pulse at V_{DD} = 5.5V (MCP6548 only).*

Note: Unless otherwise indicated, V_{DD} = +1.6V to +5.0V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}– =$ GND, R_{PU} = 2.74 kΩ to $V_{PU} = V_{DD}$, and C_L = 36 pF.

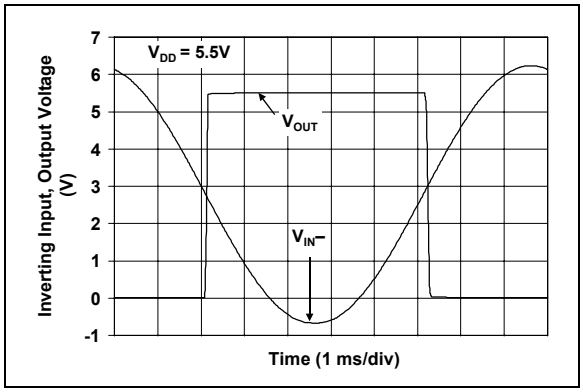


FIGURE 2-37: *The MCP6546/7/8/9 comparators show no phase reversal.*

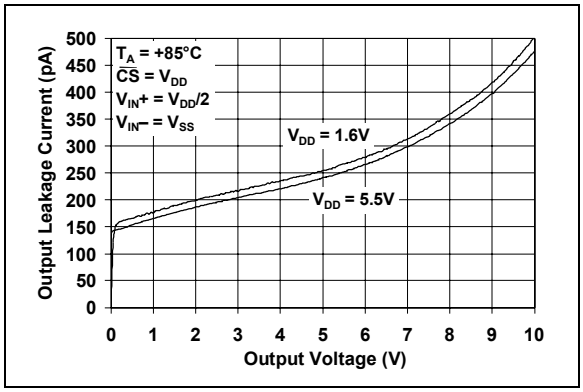


FIGURE 2-38: *Output Leakage Current ($\overline{CS} = V_{DD}$) vs. Output Voltage (MCP6548 only)*

3.0 APPLICATIONS INFORMATION

The MCP6546/7/8/9 family of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of applications requiring very low power consumption.

3.1 Comparator Inputs

The MCP6546/7/8/9 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-37 shows an input voltage exceeding both supplies with no resulting phase inversion.

The input stage of this family of devices uses two differential input stages in parallel: one operates at low input voltages and the other at high input voltages. With this topology, the input voltage is 0.3V above V_{DD} and 0.3V below V_{SS}. Therefore, the input offset voltage is measured at both V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The maximum operating input voltages that can be applied are V_{SS} - 0.3V and V_{DD} + 0.3V. Voltages on the inputs that exceed this absolute maximum rating can cause excessive current to flow and permanently damage the device. In applications where the input pin exceeds the specified range, external resistors can be used to limit the current below ±2 mA, as shown in Figure 3-1.

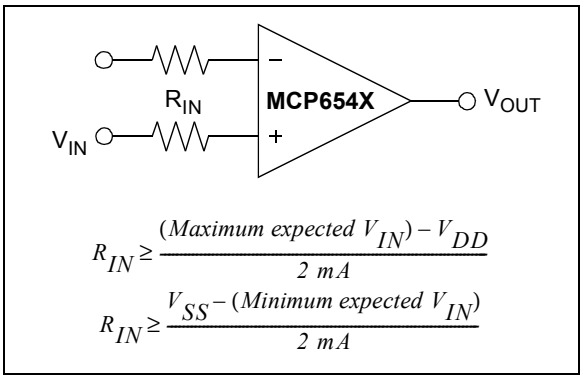


FIGURE 3-1: *An input resistor (R_{IN}) should be used to limit excessive input current if either of the inputs exceeds the absolute maximum specification.*

3.2 Open-Drain Output

The open-drain output is designed to make level-shifting and wired-OR logic easy to implement. The output can go as high as 10V for 9V battery-powered applications. The output stage minimizes switching current (shoot-through current from supply-to-supply) when the output changes state. See Figures 2-15, 2-17 and 2-32 through 2-36, for more information.

3.3 MCP6548 Chip Select ($\overline{CS}$)

The MCP6548 is a single comparator with a chip select ($\overline{CS}$) option. When $\overline{CS}$ is pulled high, the total current consumption drops to 20 pA (typ). 1 pA (typ) flows through the $\overline{CS}$ pin, 1 pA (typ) flows through the output pin and 18 pA (typ) flows through the V_{DD} pin, as shown in Figure 1-1. When this happens, the comparator output is put into a high-impedance state. By pulling $\overline{CS}$ low, the comparator is enabled. If the $\overline{CS}$ pin is left floating, the comparator will not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

The internal $\overline{CS}$ circuitry is designed to minimize glitches when cycling the $\overline{CS}$ pin. This helps conserve power, which is especially important in battery-powered applications.

3.4 Externally Set Hysteresis

Greater flexibility in selecting hysteresis, or input trip points, is achieved by using external resistors.

Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points. Hysteresis reduces output chattering when one input is slowly moving past the other, thus reducing dynamic supply current. It also helps in systems where it is best not to cycle between states too frequently (e.g., air conditioner thermostatic control). The MCP6546/7/8/9 family has internally-set hysteresis that is small enough to maintain input offset accuracy (<7 mV), and large enough to eliminate output chattering caused by the comparator's own input noise voltage (200 µVp-p).

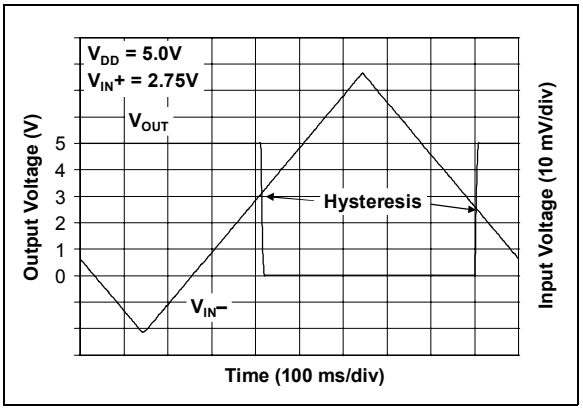


FIGURE 3-2: *The MCP6546/7/8/9 comparators' internal hysteresis eliminates output chatter caused by input noise voltage.*

3.4.1 INVERTING CIRCUIT

Figure 3-3 shows an inverting circuit for a single-supply application using three resistors, besides the pull-up resistor. The resulting hysteresis diagram is shown in Figure 3-4.

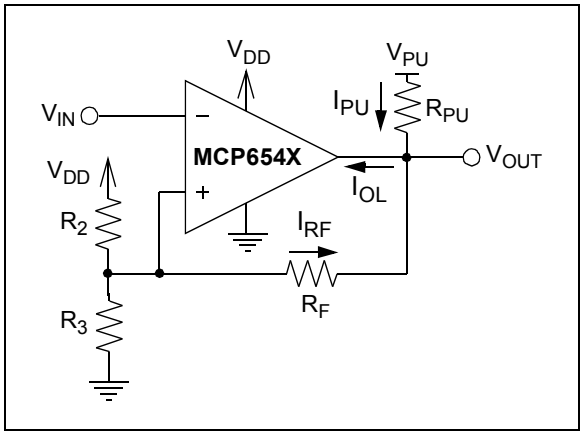


FIGURE 3-3: *Inverting circuit with hysteresis.*

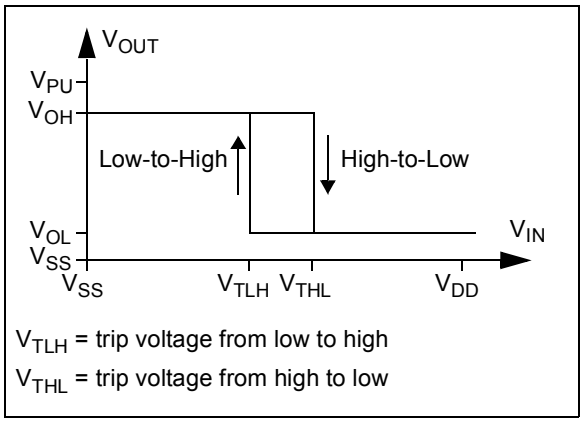


FIGURE 3-4: *Hysteresis diagram for the inverting circuit.*

In order to determine the trip voltages (V_{THL} and V_{TLH}) for the circuit shown in Figure 3-3, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{DD}, as shown in Figure 3-5.

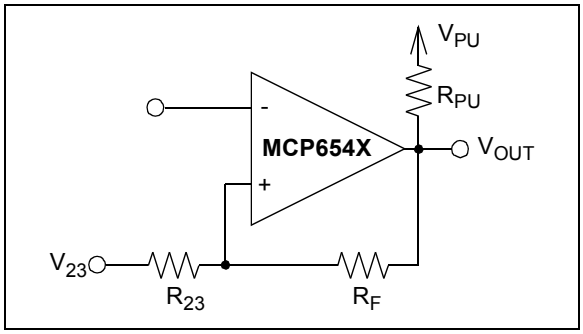


FIGURE 3-5: *Thevenin Equivalent Circuit.*

Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION

$$V_{THL} = V_{PU}\left(\frac{R_{23}}{R_{23} + R_F + R_{PU}}\right) + V_{23}\left(\frac{R_F + R_{PU}}{R_{23} + R_F + R_{PU}}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

V_{TLH} = trip voltage from low to high

V_{THL} = trip voltage from high to low

Figure 2-19 and Figure 2-22 can be used to determine typical values for V_{OL}. This voltage is dependent on the output current I_{OL} as shown in Figure 3-3. This current can be determined using the equation below:

EQUATION

$$I_{OL} = I_{PU} + I_{RF}$$

$$I_{OL} = \left(\frac{V_{PU} - V_{OL}}{R_{PU}}\right) + \left(\frac{V_{23} - V_{OL}}{R_{23} + R_F}\right)$$

V_{OH} can be calculated using the equation below:

EQUATION

$$V_{OH} = (V_{PU} - V_{23}) \times \left(\frac{R_{23} + R_F}{R_{23} + R_F + R_{PU}}\right)$$

As explained in Section 3.1, “Comparator Inputs”, it is important to keep the non-inverting input below V_{DD}+0.3V when $V_{PU} > V_{DD}$.

3.5 Supply Bypass

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

3.6 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-27). The supply current increases with increasing toggle frequency (Figure 2-30), especially with higher capacitive loads.

3.7 Battery Life

In order to maximize battery life in portable applications, use large resistors and small capacitive loads. Also, avoid toggling the output more than necessary and do not use chip select ($\overline{CS}$) to conserve power for short periods of time. Capacitive loads will draw additional power at start-up.

3.8 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low-humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA. If current-to-flow, this is greater than the MCP6546/7/8/9 family's bias current at 25°C (1 pA, typ).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-6.

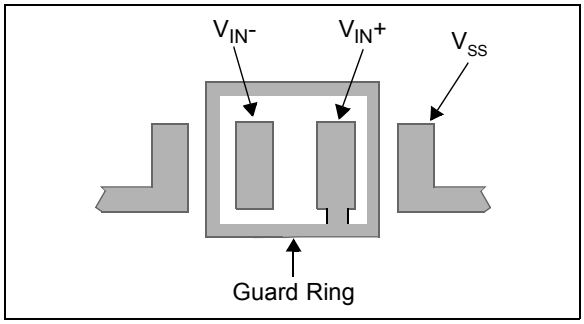


FIGURE 3-6: *Example Guard Ring Layout for Inverting Circuit.*

1. Inverting Configuration (Figures 3-3 and 3-6):
   a. Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin (V_{IN}–) to the input pad without touching the guard ring.

3.9 Typical Applications

3.9.1 PRECISE COMPARATOR

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6041) to gain-up the input signal before it reaches the comparator. Figure 3-7 shows an example of this approach.

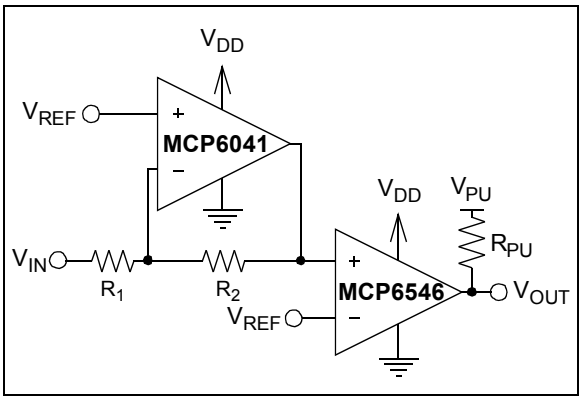


FIGURE 3-7: *Precise Inverting Comparator.*

3.9.2 WINDOWED COMPARATOR

Figure 3-8 shows one approach to designing a windowed comparator. The wired-OR connection produces a high output (logic 1) when the input voltage is between V_{RB} and V_{RT} (where $V_{RT} > V_{RB}$).

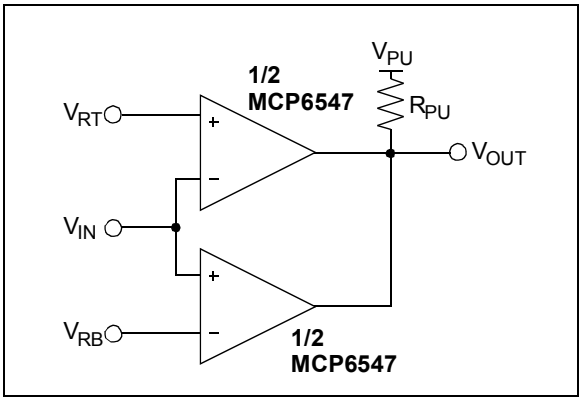
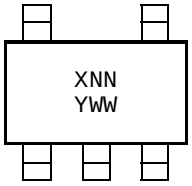


FIGURE 3-8: *Windowed comparator.*

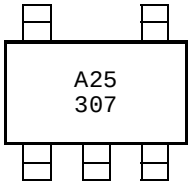
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

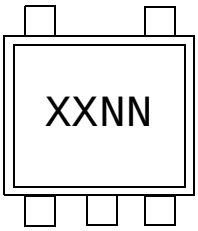
5-Lead SC-70 (**MCP6546**)



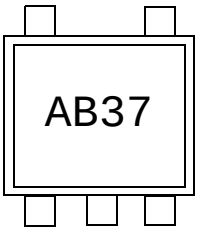
Example:



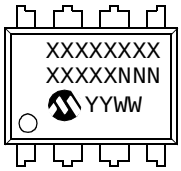
5-Lead SOT-23 (**MCP6546**)



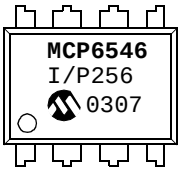
Example:



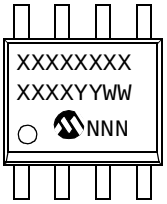
8-Lead PDIP (300 mil)



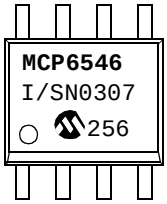
Example:



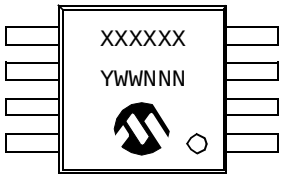
8-Lead SOIC (150 mil)



Example:



8-Lead MSOP



Example:

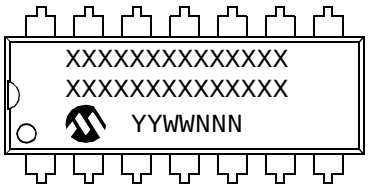
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

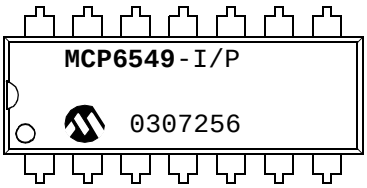
***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Package Marking Information (Continued)

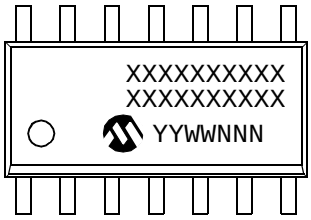
14-Lead PDIP (300 mil) (**MCP6549**)



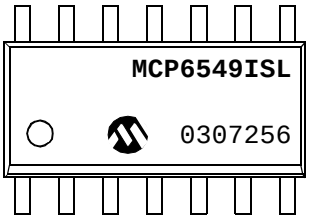
Example:



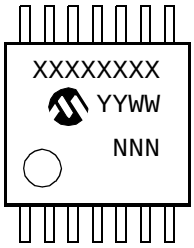
14-Lead SOIC (150 mil) (**MCP6549**)



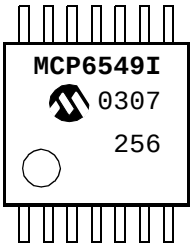
Example:



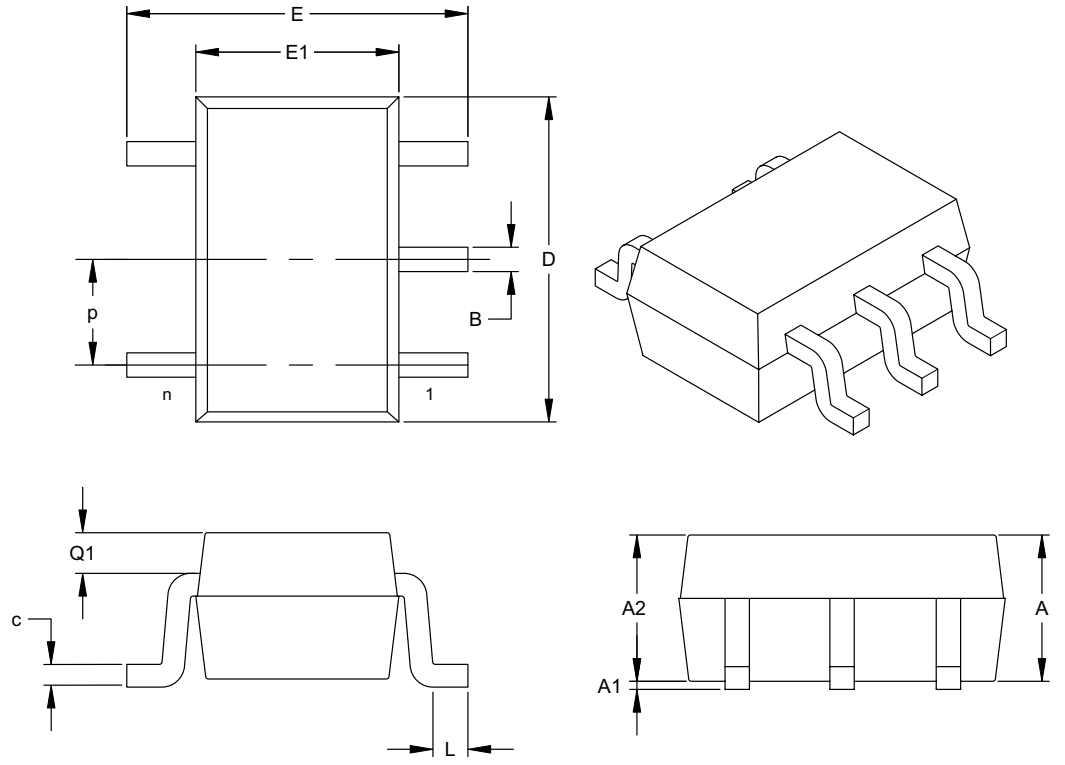
14-Lead TSSOP (**MCP6549**)



Example:



5-Lead Plastic Package (LT) (SC-70)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.026 (BSC)			0.65 (BSC)	
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

*Controlling Parameter

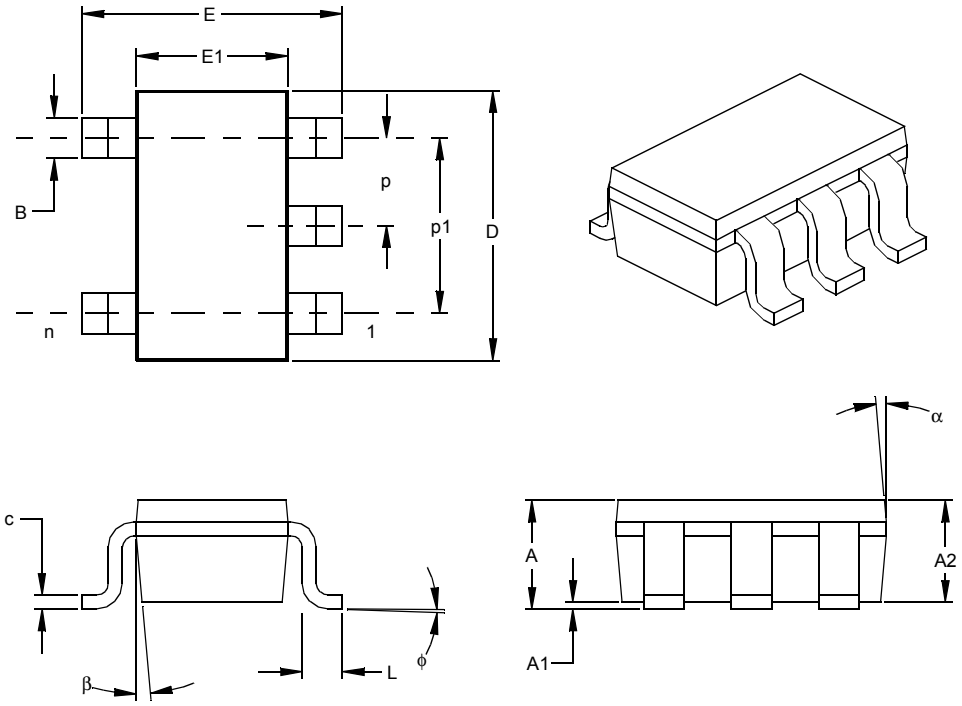
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

5-Lead Plastic Small Outline Transistor (OT) (SOT23)

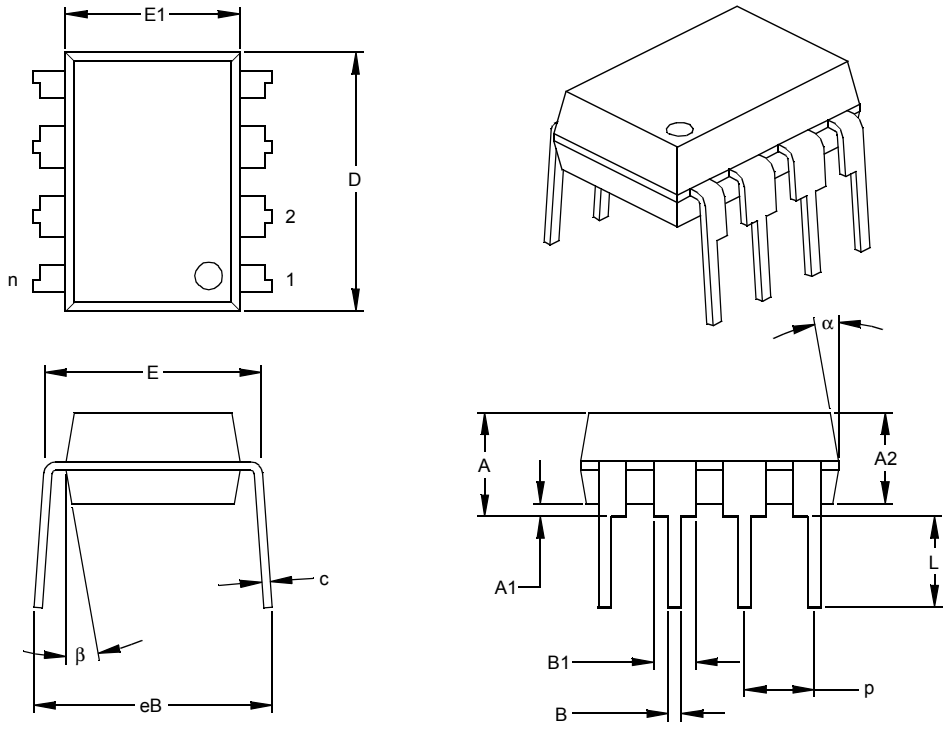


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

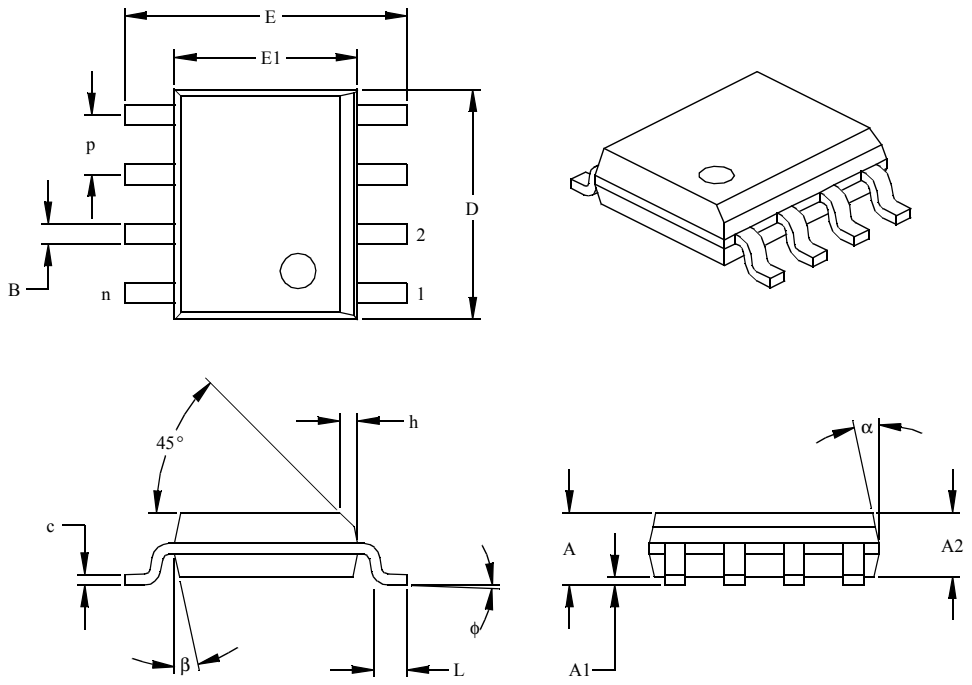


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	a	5	10	15	5	10	15
Mold Draft Angle Bottom	b	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

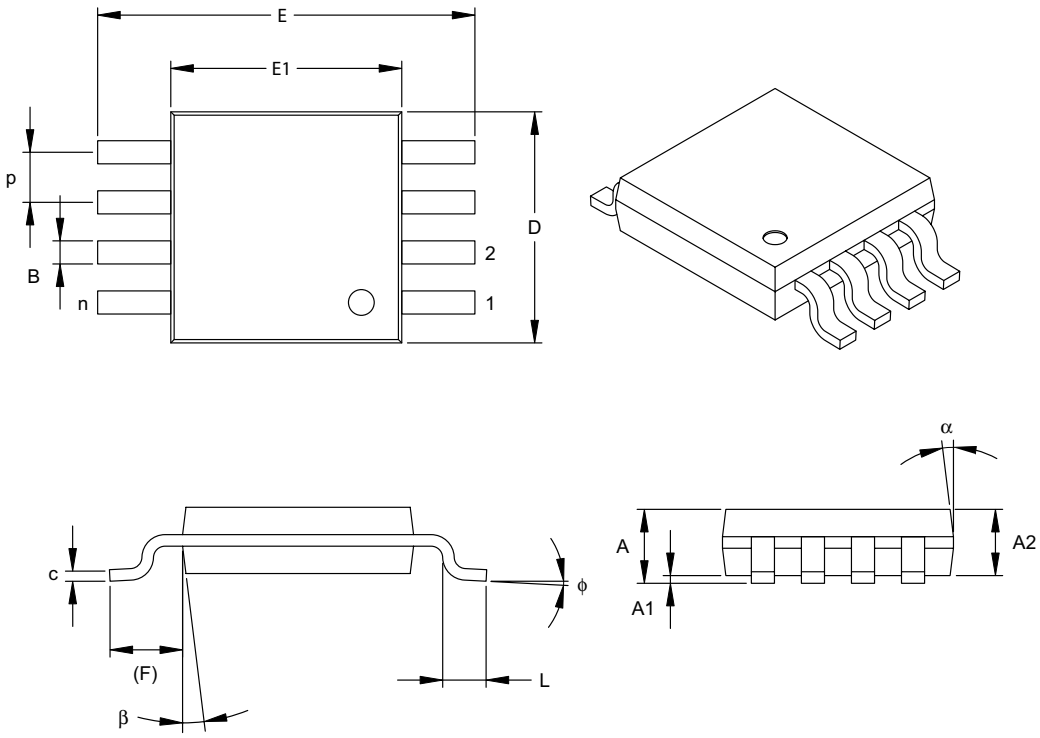


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

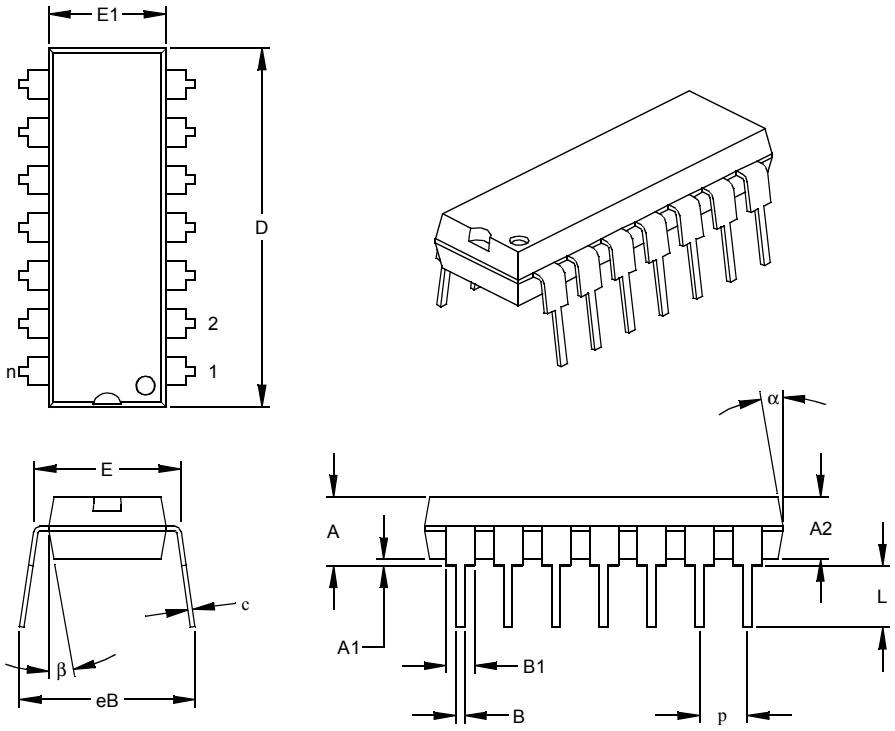
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

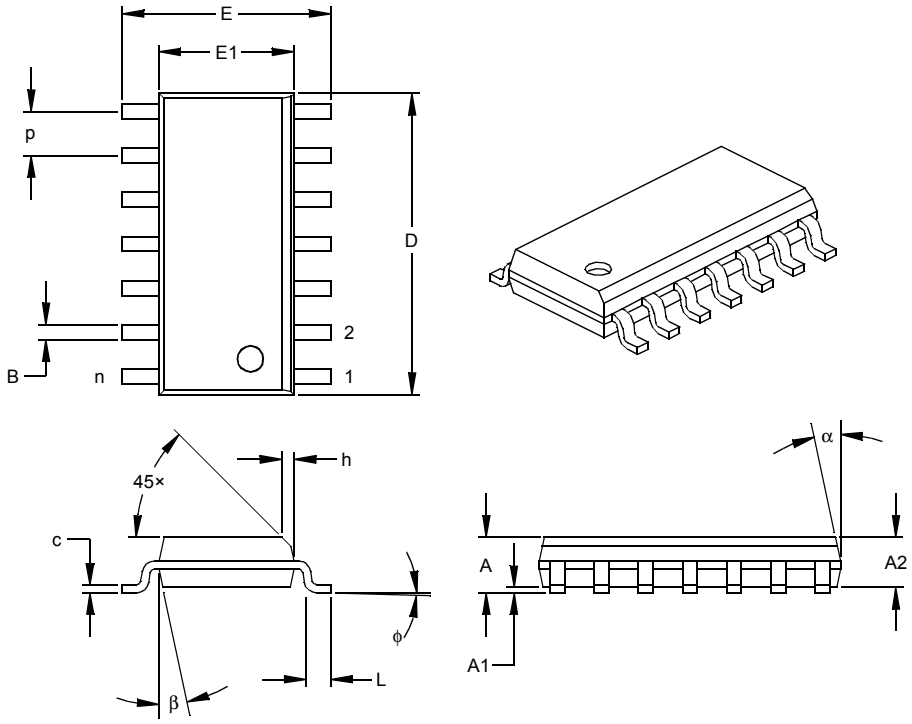
14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

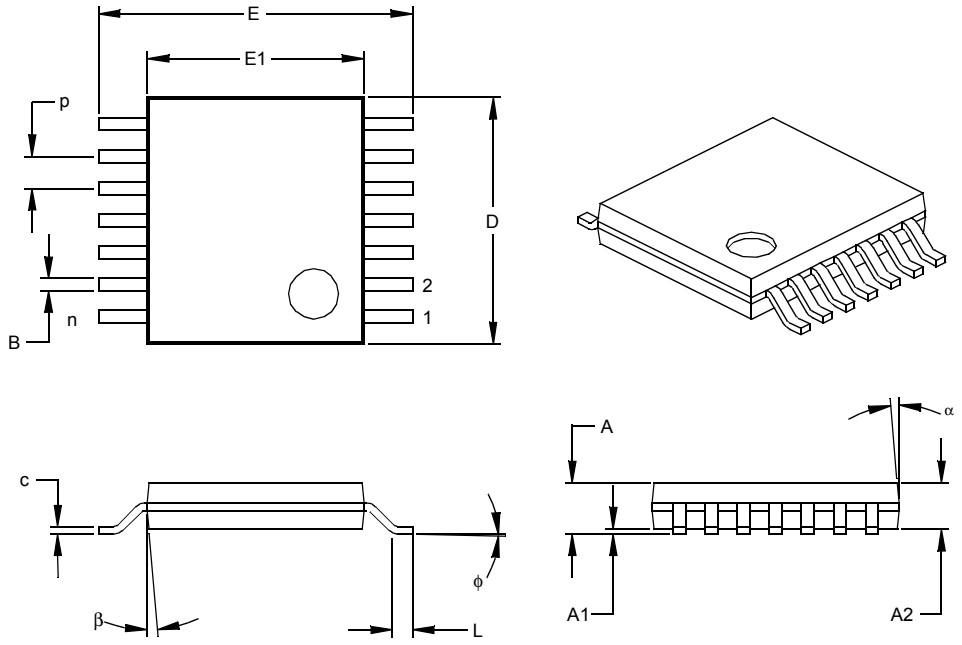


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP6546:	Single Comparator
	MCP6546T:	Single Comparator (Tape and Reel) (SC-70, SOT-23, SOIC, MSOP)
	MCP6546RT:	Single Comparator (Rotated - Tape and Reel) (SOT-23 only)
	MCP6547:	Dual Comparator
	MCP6547T:	Dual Comparator (Tape and Reel for SOIC and MSOP)
	MCP6548:	Single Comparator with $\overline{CS}$
	MCP6548T:	Single Comparator with $\overline{CS}$ (Tape and Reel for SOIC and MSOP)
	MCP6549:	Quad Comparator
	MCP6549T:	Quad Comparator (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	LT =	Plastic Package (SC-70), 5-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead
	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead (MCP6549)
	ST =	Plastic TSSOP (4.4mm Body), 14-lead (MCP6549)

Examples:

a)	MCP6546T-I/LT:	Tape and Reel, Industrial Temperature, 5LD SC-70.
b)	MCP6546T-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT-23.
c)	MCP6546-I/P:	Industrial Temperature, 8LD PDIP.
d)	MCP6546RT-I/OT:	Tape and Reel, Industrial Temperature, 5LD SOT23.
a)	MCP6547-I/MS:	Industrial Temperature, 8LD MSOP.
b)	MCP6547T-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP.
c)	MCP6547-I/P:	Industrial Temperature, 8LD PDIP.
a)	MCP6548-I/SN:	Industrial Temperature, 8LD SOIC.
b)	MCP6548T-I/SN:	Tape and Reel, Industrial Temperature, 8LD SOIC.
c)	MCP6548-I/P:	Industrial Temperature, 8LD PDIP.
a)	MCP6549T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC.
b)	MCP6549T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC.
c)	MCP6549-I/P:	Industrial Temperature, 14LD PDIP.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System
Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV MSC The Netherlands Accredited by the RvA — DNV — ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde
Room 401, Hongjian Building
No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands
P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/28/03