

## Monolithic 2A Step-Down Regulator

The EL7532 is a synchronous, integrated FET 2A step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a single Li-Ion battery source. The output can be externally set from 0.8V to  $V_{IN}$  with a resistive divider.

The EL7532 features PWM mode control. The operating frequency is typically 1.5MHz. Additional features include a 100ms Power-On-Reset output,  $<1\mu\text{A}$  shut-down current, short-circuit protection, and over-temperature protection.

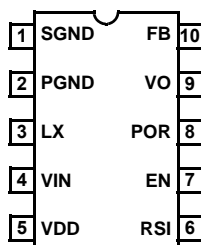
The EL7532 is available in the 10-pin MSOP package, making the entire converter occupy less than 0.18 in<sup>2</sup> of PCB area with components on one side only. The package is specified for operation over the full -40°C to +85°C temperature range.

## Ordering Information

PART NUMBER (BRAND)	PACKAGE	TAPE & REEL	PKG. DWG. #
EL7532IY (BABAA)	10-Pin MSOP	-	MDP0043
EL7532IY-T7 (BABAA)	10-Pin MSOP	7"	MDP0043
EL7532IY-T13 (BABAA)	10-Pin MSOP	13"	MDP0043
EL7532IYZ (BAARA) (Note)	10-Pin MSOP (Pb-free)	-	MDP0043
EL7532IYZ-T7 (BAARA) (Note)	10-Pin MSOP (Pb-free)	7"	MDP0043
EL7532IYZ-T13 (BAARA) (Note)	10-Pin MSOP (Pb-free)	13"	MDP0043

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinout



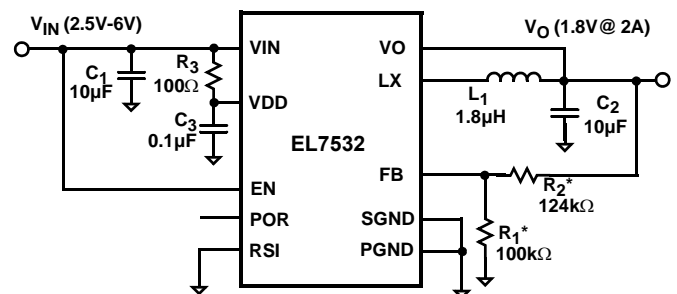
## Features

- 2A continuous current (from -40°C to +85°C)
- Less than 0.18 in<sup>2</sup> footprint for the complete 2A converter
- Max height 1.1mm MSOP10
- 1.5MHz (typ.) switching frequency
- 100ms Power-On-Reset output (POR)
- Internally-compensated voltage mode controller
- Up to 94% efficiency
- $<1\mu\text{A}$  shut-down current
- Overcurrent and over temperature protection
- Pb-Free plus anneal available (RoHS compliant)

## Applications

- PDA and pocket PC computers
- Bar code readers
- ADSL Modems
- Portable instruments
- Li-Ion battery powered devices
- ASIC/FPGA/DSP supplies
- Set Top Boxes

## Typical Application Schematic



$$* V_O = 0.8V * (1 + R_2 / R_1)$$

**Absolute Maximum Ratings** ( $T_A = 25^{\circ}\text{C}$ )

$V_{IN}, V_{DD}$ , POR to SGND	-0.3V to +6.5V
LX to PGND	-0.3V to ( $V_{IN} + 0.3\text{V}$ )
RSI, EN, $V_O$ , FB to SGND	-0.3V to ( $V_{IN} + 0.3\text{V}$ )
PGND to SGND	-0.3V to +0.3V
Peak Output Current	2.4A
ESD Classification	
Human Body Model (Per JESD22-A114-B)	Class 2

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}\text{C/W}$ )
MSOP10 Package (Note 1)	115
Operating Ambient Temperature	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
Storage Temperature	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Junction Temperature	+125 $^{\circ}\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**NOTE:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

**Electrical Specifications**  $V_{DD} = V_{IN} = V_{EN} = 3.3\text{V}$ ,  $C1 = C2 = 10\mu\text{F}$ ,  $L = 1.8\mu\text{H}$ ,  $V_O = 1.8\text{V}$ , unless otherwise specified.

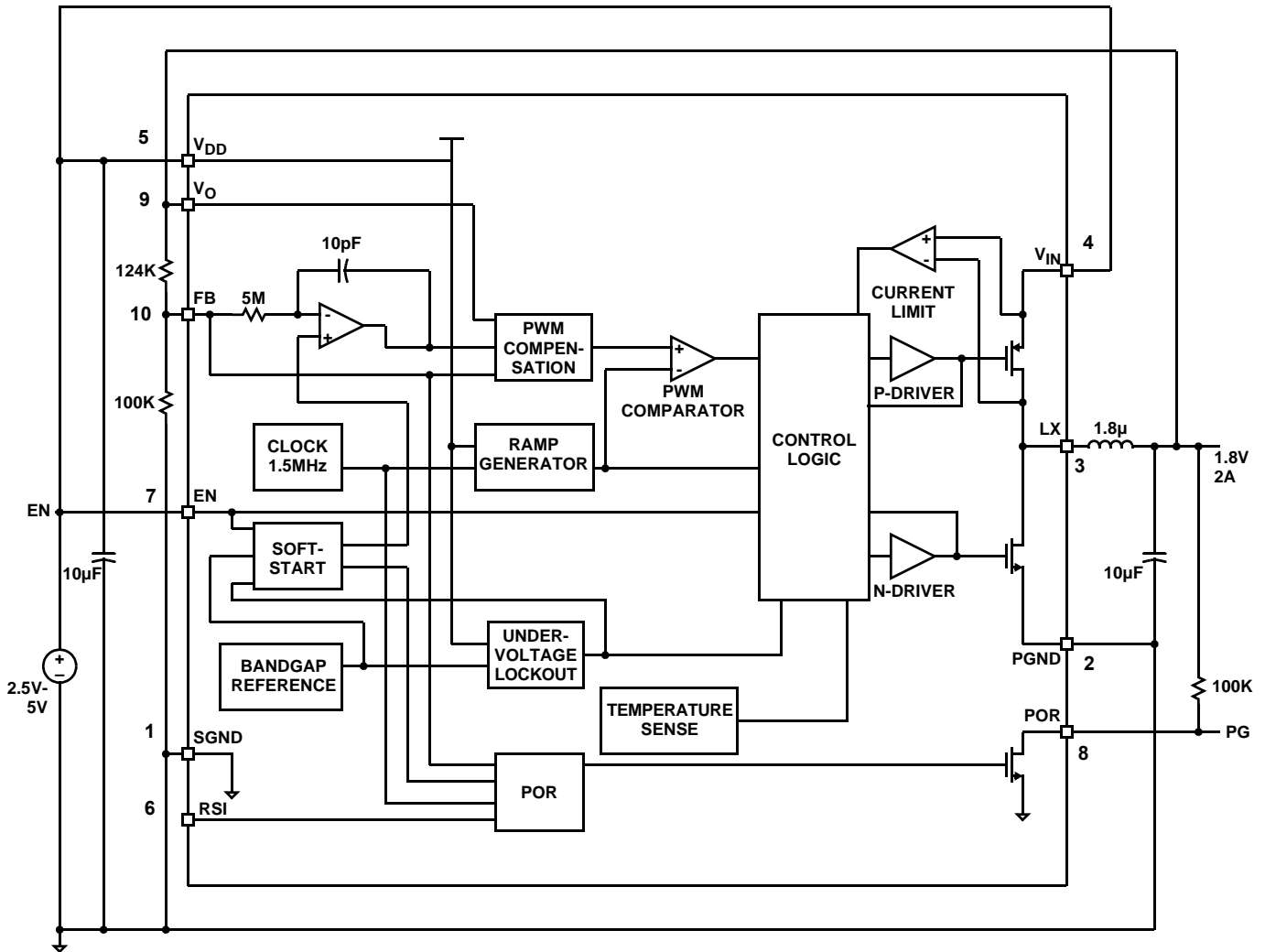
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC CHARACTERISTICS</b>						
$V_{FB}$	Feedback Input Voltage		790	800	810	mV
$I_{FB}$	Feedback Input Current				250	nA
$V_{IN}, V_{DD}$	Input Voltage		2.5		5.5	V
$V_{IN,OFF}$	Minimum Voltage for Shutdown	$V_{IN}$ falling	2		2.2	V
$V_{IN,ON}$	Maximum Voltage for Startup	$V_{IN}$ rising	2.2		2.4	V
$I_{DD}$	Supply Current	PWM, $V_{IN} = V_{DD} = 5\text{V}$		400	500	$\mu\text{A}$
		EN = 0, $V_{IN} = V_{DD} = 5\text{V}$		0.1	1	$\mu\text{A}$
$R_{DS(ON)-PMOS}$	PMOS FET Resistance	$V_{DD} = 5\text{V}$ , wafer test only		52	80	$\text{m}\Omega$
$R_{DS(ON)-NMOS}$	NMOS FET Resistance	$V_{DD} = 5\text{V}$ , wafer test only		35	65	$\text{m}\Omega$
$I_{LMAX}$	Current Limit (GBD)			3		A
$T_{OT,OFF}$	Over-temperature Threshold (GBD)	T rising		145		$^{\circ}\text{C}$
$T_{OT,ON}$	Over-temperature Hysteresis (GBD)	T falling		130		$^{\circ}\text{C}$
$I_{EN}, I_{RSI}$	EN, RSI Current	$V_{EN}, V_{RSI} = 0\text{V}$ and 3.3V	-1		1	V
$V_{EN1}, V_{RSI1}$	EN, RSI Rising Threshold	$V_{DD} = 3.3\text{V}$			2.4	V
$V_{EN2}, V_{RSI2}$	EN, RSI Falling Threshold	$V_{DD} = 3.3\text{V}$	0.8			V
$V_{POR}$	Minimum $V_{FB}$ for POR, WRT Targeted $V_{FB}$ Value	$V_{FB}$ rising			95	%
		$V_{FB}$ falling	86			%
$V_{OLPOR}$	POR Voltage Drop	$I_{SINK} = 5\text{mA}$		35	70	mV
$V_{LINEREG}$	Line Regulation (GBD)	$V_{IN} = 2.5\text{V}$ to 6V, $I_{OUT} = 2\text{A}$ , $V_{OUT} = 1.8\text{V}$		0.1		%/V
$V_{LOADREG}$	Load Regulation (GBD)	$V_{IN} = 3.3\text{V}$ , $V_{OUT} = 1.8\text{V}$ , $I_{OUT} = 0$ to 2A		0.5		%
<b>AC CHARACTERISTICS</b>						
$F_{PWM}$	PWM Switching Frequency		1.35	1.5	1.65	MHz
$t_{RSI}$	Minimum RSI Pulse Width (GBD)	Guaranteed by design		25	50	ns
$t_{SS}$	Soft-start Time (GBD)			650		$\mu\text{s}$
$t_{POR}$	Power On Reset Delay Time (GBD)		80	100	120	ms

GBD = Guaranteed By Design

**Pin Descriptions**

PIN NUMBER	PIN NAME	PIN FUNCTION
1	SGND	Negative supply for the controller stage
2	PGND	Negative supply for the power stage
3	LX	Inductor drive pin; high current digital output with average voltage equal to the regulator output voltage
4	VIN	Positive supply for the power stage
5	VDD	Power supply for the controller stage
6	RSI	Resets POR timer; Connect to ground if not used
7	EN	Enable; Can be connected directly to the VIN for enable
8	POR	Power on reset open drain output; Leave open if not used
9	VO	Output voltage sense pin
10	FB	Voltage feedback input; connected to an external resistor divider between V <sub>O</sub> and SGND for variable output

**Block Diagram**



Typical Performance Curves

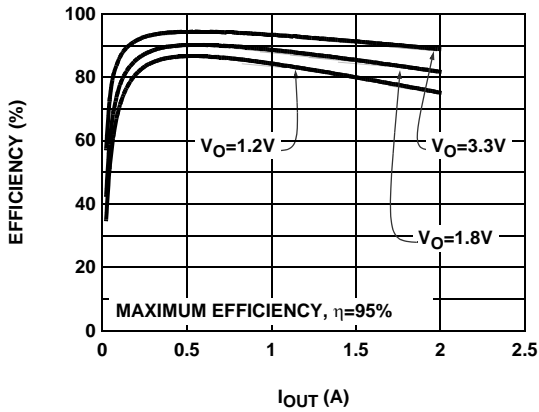


FIGURE 1. EFFICIENCY vs IOUT @ VIN=5V

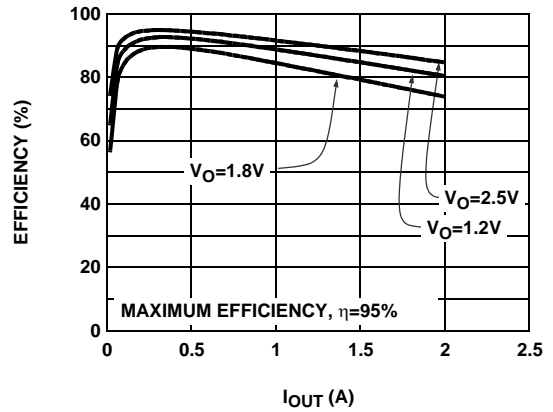


FIGURE 2. EFFICIENCY vs IOUT @ VIN=3.3V

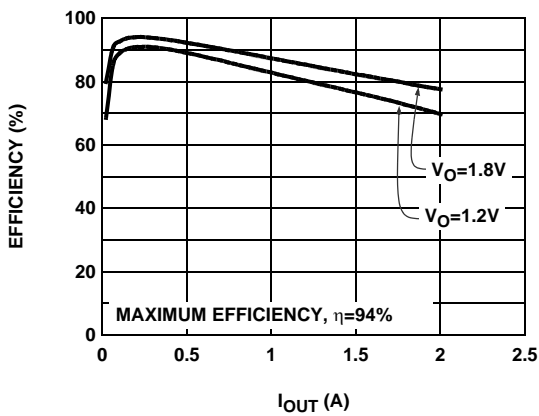


FIGURE 3. EFFICIENCY vs IOUT @ VIN=2.5V

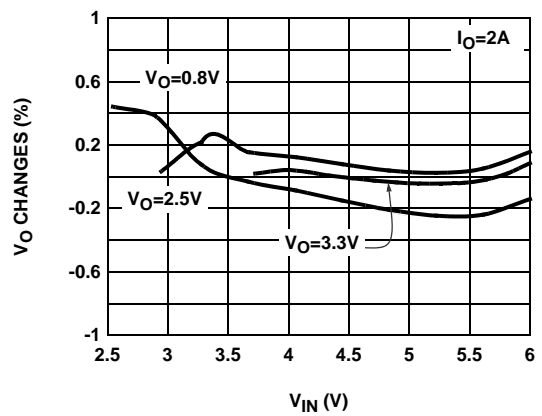


FIGURE 4. LINE REGULATION

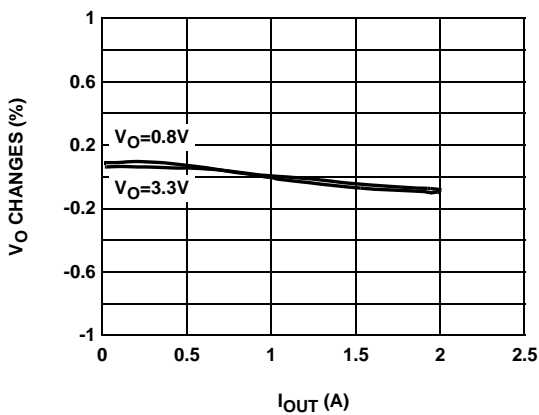


FIGURE 5. LOAD REGULATION @ VIN=5V

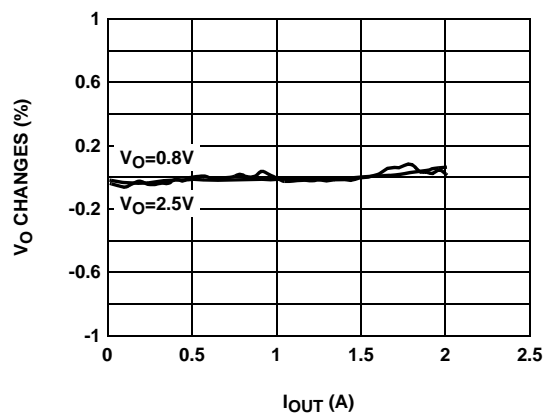


FIGURE 6. LOAD REGULATION @ VIN=3.3V

Typical Performance Curves (Continued)

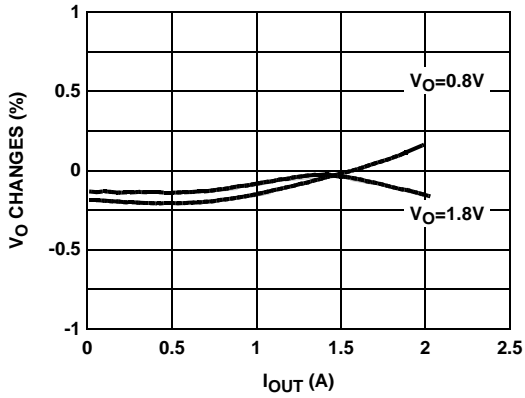


FIGURE 7. LOAD REGULATION @  $V_{IN}=2.5V$

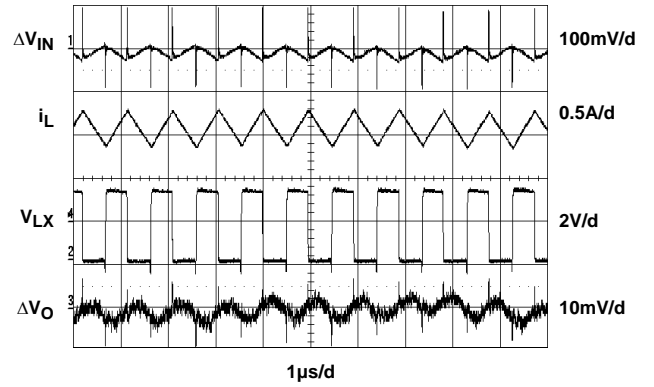


FIGURE 8. LOAD REGULATION @  $V_{IN}=2.5V$

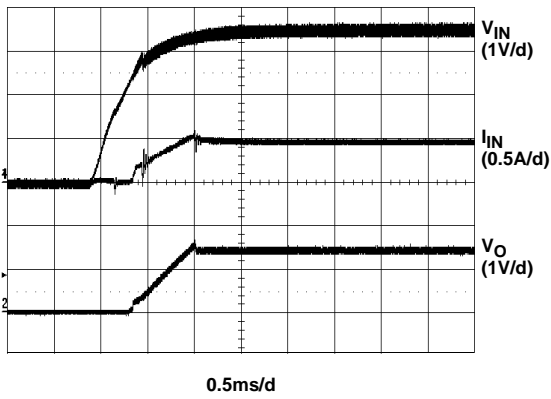


FIGURE 9. START-UP 1

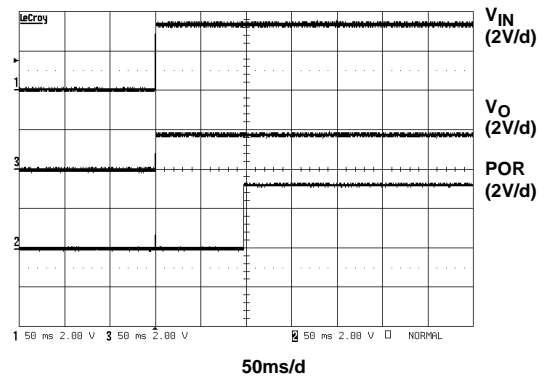


FIGURE 10. START-UP 2

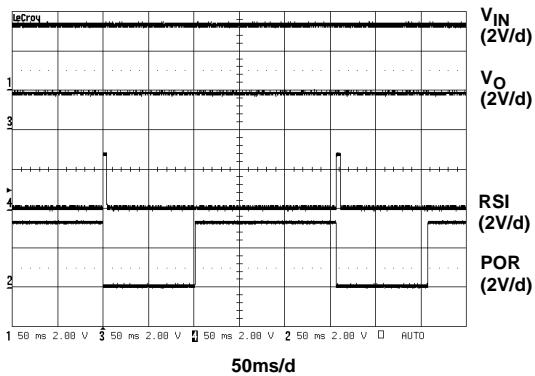


FIGURE 11. POR FUNCTION

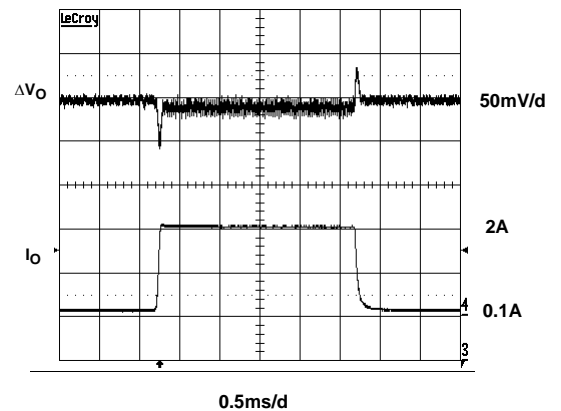


FIGURE 12. TRANSIENT RESPONSE

Typical Performance Curves (Continued)

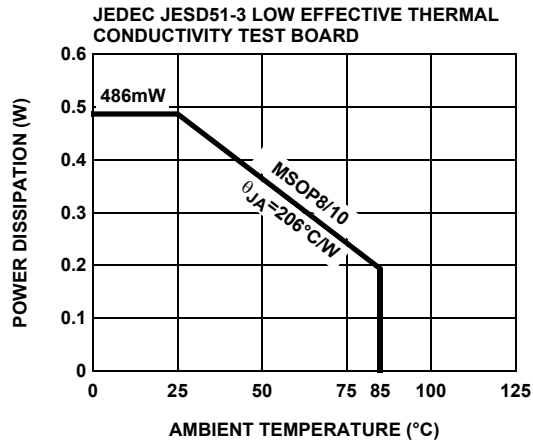


FIGURE 13. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

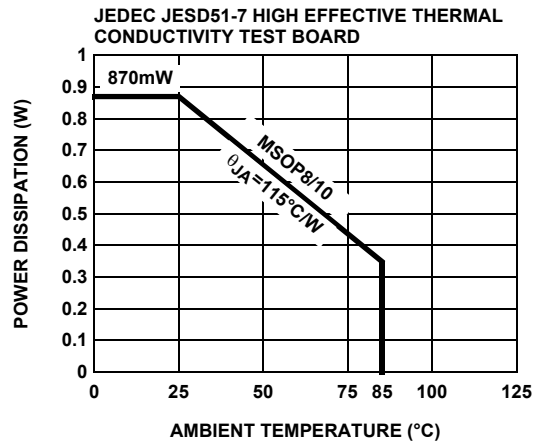


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

## Applications Information

### Product Description

The EL7532 is a synchronous, integrated FET 2A step-down regulator which operates from an input of 2.5V to 6V. The output voltage is user-adjustable with a pair of external resistors.

The internally-compensated controller makes it possible to use only two ceramic capacitors and one inductor to form a complete, very small footprint 2A DC-DC converter.

### Start-Up and Shut-Down

When the EN pin is tied to  $V_{IN}$ , and  $V_{IN}$  reaches approximately 2.4V, the regulator begins to switch. The output voltage is gradually increased to ensure proper soft-start operation.

When the EN pin is connected to a logic low, the EL7532 is in the shut-down mode. All the control circuitry and both MOSFETs are off, and  $V_{OUT}$  falls to zero. In this mode, the total input current is less than 1 $\mu$ A.

When the EN reaches logic HI, the regulator repeats the start-up procedure, including the soft-start function.

### PWM Operation

In the PWM mode, the P channel MOSFET and N channel MOSFET always operate complementary. When the PMOSFET is on and the NMOSFET off, the inductor current increases linearly. The input energy is transferred to the output and also stored in the inductor. When the P channel MOSFET is off and the N channel MOSFET on, the inductor current decreases linearly, and energy is transferred from the inductor to the output. Hence, the average current through the inductor is the output current. Since the inductor and the output capacitor act as a low pass filter, the duty cycle ratio is approximately equal to  $V_O$  divided by  $V_{IN}$ .

The output LC filter has a second order effect. To maintain the stability of the converter, the overall controller must be compensated. This is done with the fixed internally compensated error amplifier and the PWM compensator. Because the compensations are fixed, the values of input and output capacitors are 10 $\mu$ F to 22 $\mu$ F ceramic. The inductor is nominally 1.8 $\mu$ H, though 1.5 $\mu$ H to 2.2 $\mu$ H can be used.

### 100% Duty Ratio Operation

EL7532 utilizes CMOS power FET's as the internal synchronous power switches. The upper switch is a PMOS and lower switch a NMOS. This not only saves a boot capacitor, it also allows 100% turn-on of the upper PFET switch, achieving  $V_O$  close to  $V_{IN}$ . The maximum achievable  $V_O$  is,

$$V_O = V_{IN} - (R_L + R_{DSON1}) \times I_O$$

Where  $R_L$  is the DC resistance on the inductor and  $R_{DSON1}$  the PFET on-resistance, nominal 70m $\Omega$  at room temperature with tempco of 0.2m $\Omega$ /°C.

As the input voltage drops gradually close or even below the preset  $V_O$ , the converter gets into 100% duty ratio. At this condition, the upper PFET needs some minimum turn-off time if it is turned off. This off-time is related to input/output conditions. This makes the duty ratio appear randomly and increases the output ripple somewhat until the 100% duty ratio is reached. A larger output capacitor could reduce the random-looking ripple. Users need to verify if this condition has an adverse effect on the overall circuit if close to 100% duty ratio is expected.

### RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for about 100ms after  $V_O$  reaches the preset voltage. When the active-HI reset signal RSI is issued, POR goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected. (Please refer to the timing diagram). When the function is not used, connect RSI to ground and leave open the pull-up resistor  $R_4$  at POR pin.

The POR output also serves as a 100ms delayed Power Good signal when the pull-up resistor  $R_4$  is installed. The RSI pin needs to be directly (or indirectly through a resistor  $R_6$ ) connected to Ground for this to function properly.

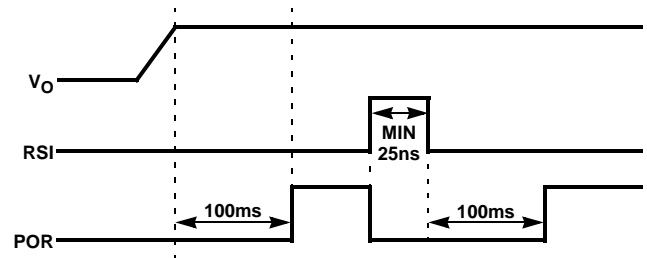


FIGURE 15. RSI & POR TIMING DIAGRAM

### Output Voltage Selection

Users can set the output voltage of the converter with a resistor divider, which can be chosen based on the following formula:

$$V_O = 0.8 \times \left( 1 + \frac{R_2}{R_1} \right)$$

### Component Selection

Because of the fixed internal compensation, the component choice is relatively narrow. We recommend 10 $\mu$ F to 22 $\mu$ F multi-layer ceramic capacitors with X5R or X7R rating for both the input and output capacitors, and 1.5 $\mu$ H to 2.2 $\mu$ H inductance for the inductor.

At extreme conditions ( $V_{IN} < 3V$ ,  $I_O > 0.7A$ , and junction temperature higher than  $75^{\circ}C$ ), input cap  $C_1$  is recommended to be  $22\mu F$ . Otherwise, if any of the above 3 conditions is not true,  $C_1$  can remain as low as  $10\mu F$ .

The RMS current present at the input capacitor is decided by the following formula:

$$I_{INRMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O$$

This is about half of the output current  $I_O$  for all the  $V_O$ . This input capacitor must be able to handle this current.

The inductor peak-to-peak ripple current is given as:

$$\Delta I_{IL} = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times f_S}$$

- L is the inductance
- $f_S$  the switching frequency (nominally 1.5MHz)

The inductor must be able to handle  $I_O$  for the RMS load current, and to assure that the inductor is reliable, it must handle the 3A surge current that can occur during a current limit condition.

### Current Limit and Short-Circuit Protection

The current limit is set at about 3A for the PMOS. When a short-circuit occurs in the load, the preset current limit restricts the amount of current available to the output, which causes the output voltage to drop below the preset voltage. In the meantime, the excessive current heats up the regulator until it reaches the thermal shut-down point.

### Thermal Shut-Down

Once the junction reaches about  $145^{\circ}C$ , the regulator shuts down. Both the P channel and the N channel MOSFETs turn off. The output voltage will drop to zero. With the output MOSFETs turned off, the regulator will soon cool down. Once the junction temperature drops to about  $130^{\circ}C$ , the regulator will restart again in the same manner as the EN pin connects to logic HI.

### Thermal Performance

The EL7532 is in a fused-lead MSOP10 package. Compared to the regular MSOP10 package, the fused-lead package provides lower thermal resistance. The typical  $\theta_{JA}$  of  $115^{\circ}C/W$  (See Thermal Information section in spec table) can be improved by maximizing the copper area around the pins. A  $\theta_{JA}$  of  $100^{\circ}C/W$  can be achieved on a 4-layer board and  $125^{\circ}C/W$  on a 2-layer board. Refer to Intersil's Tech Brief, TB379, for more information on thermal resistance.

### Layout Considerations

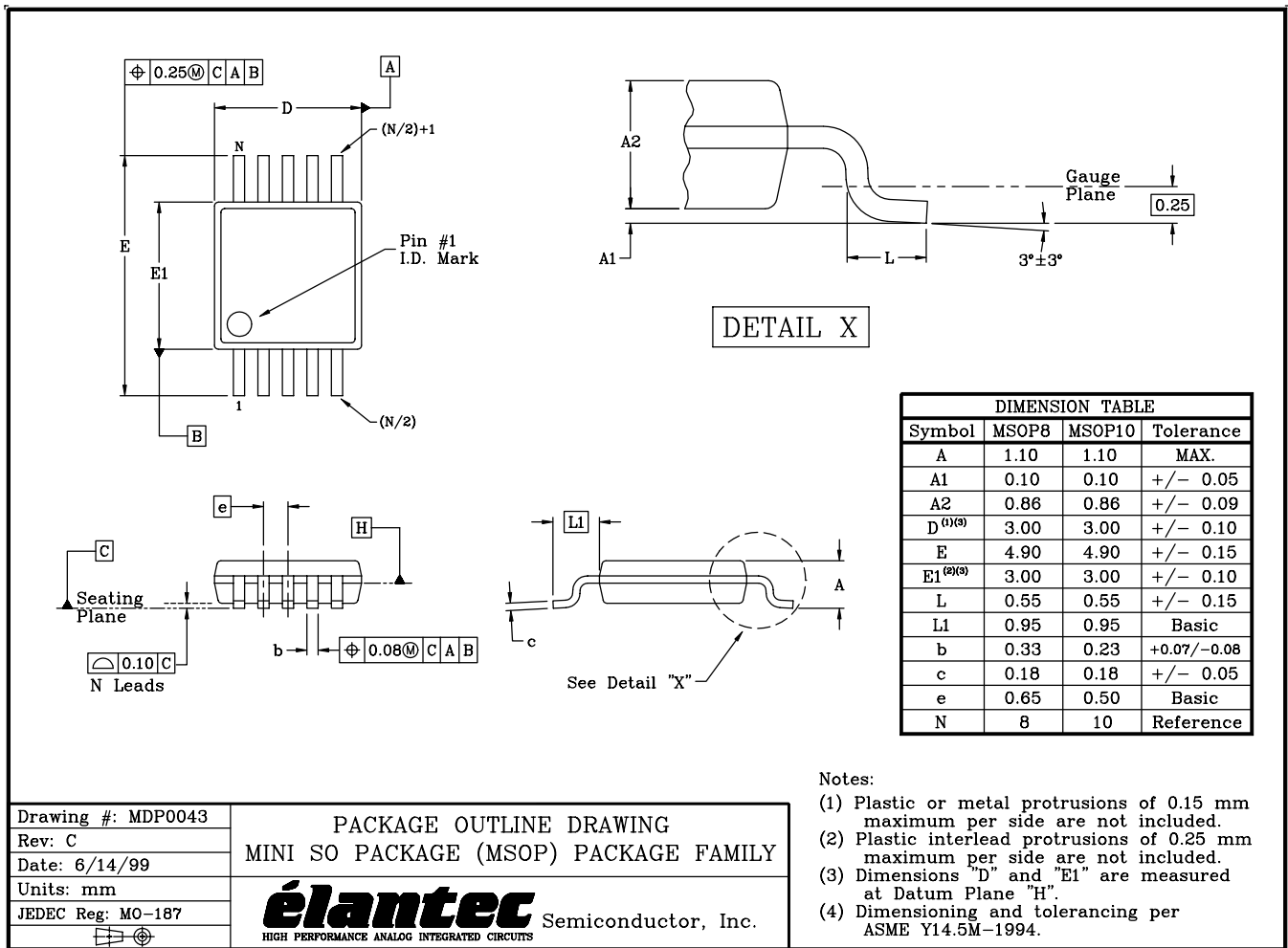
The layout is very important for the converter to function properly. The following PC layout guidelines should be followed:

- Separate the Power Ground ( $\downarrow$ ) and Signal Ground ( $\frac{\perp}{\perp}$ ); connect them only at one point right at the pins
- Place the input capacitor as close to  $V_{IN}$  and PGND pins as possible
- Make the following PC traces as small as possible:
  - from  $L_X$  pin to L
  - from  $C_O$  to PGND
- If used, connect the trace from the FB pin to  $R_1$  and  $R_2$  as close as possible
- Maximize the copper area around the PGND pin
- Place several via holes under the chip to additional ground plane to improve heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the EL7532 Application Brief.



MSOP Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <<http://www.intersil.com/design/packages/index.asp>>

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