M50753-PGYS

PIGGYBACK for M50753-XXXSP

DESCRIPTION

The M50753-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50753-XXXSP. The M50753-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50753-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50753-PGYS simplifies the development of programs for the M50753-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50753-XXXSP are:

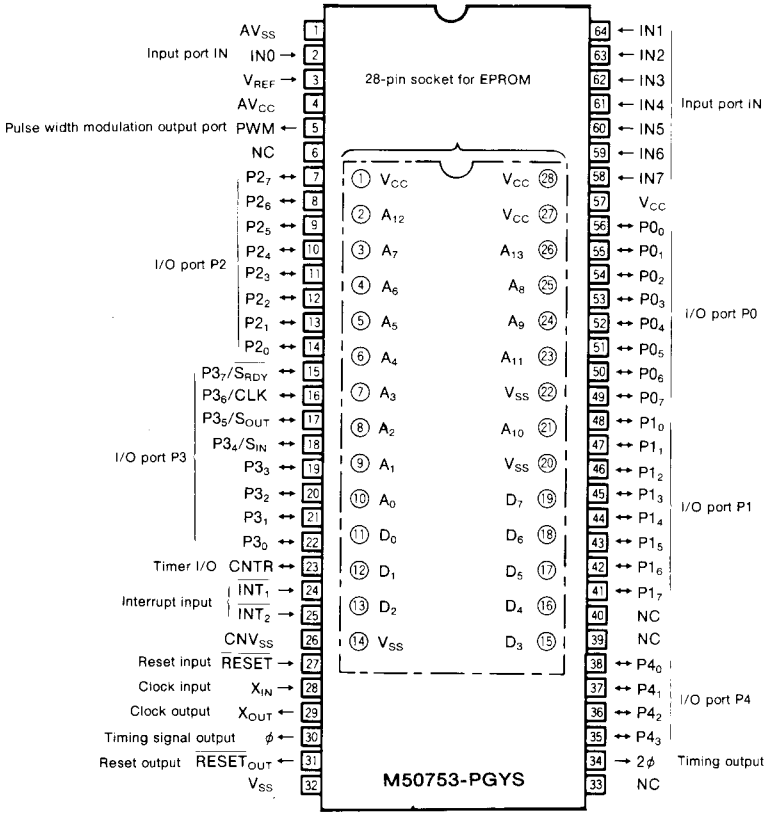
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "◡" indicates sockets for EPROM.
NC: No connection.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ, 2ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_3$	I/O port P4	I/O	Port P4 is an 4-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.
IN0~IN7	Analog input port IN	Input	This is an 8-bit analog input port for the A-D converter, and can be used as normal input port.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin the for the A-D converter.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D converter.
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D or D-A converter.
A_0~A_{13}	Output port A	Output	Port A carries the output address to the EPROM loaded on the top side of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM loaded on the top side of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50753-PGYS and the M50753-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8K bytes. Other than this, the M50753-PGYS has the same functions as the M50753-XXXSP has.

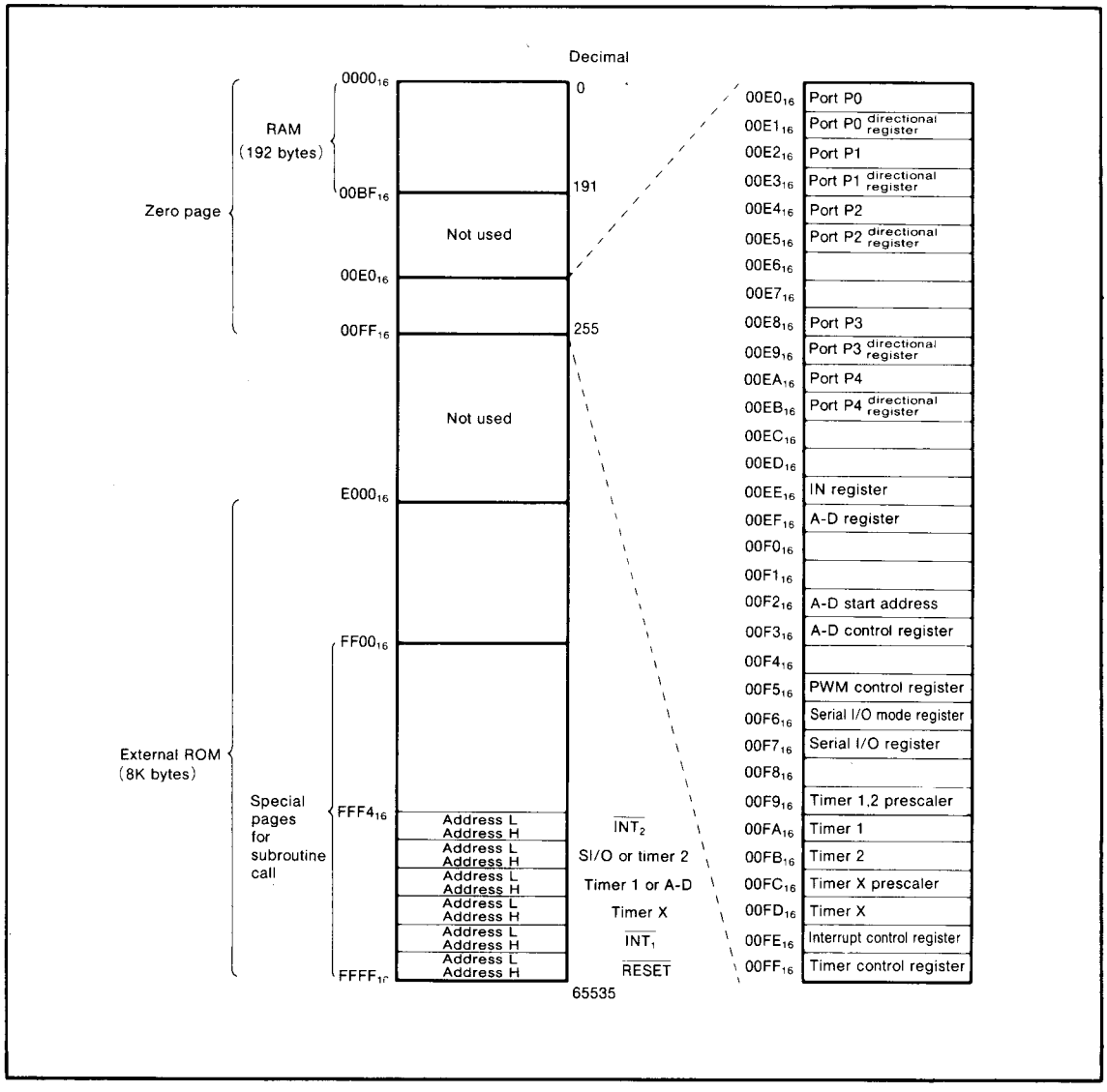


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50753-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50753-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50753-XXXSP.

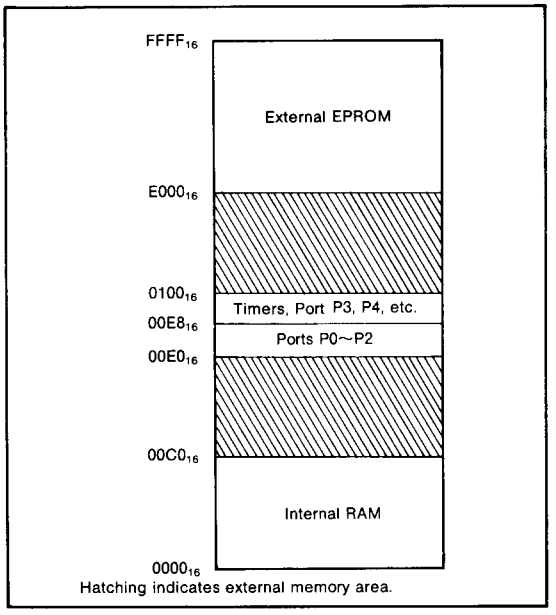


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) When developing programs with the M50753-PGYS, carefully consider the ROM capacity of the M50753-XXXSP.
In the case of the M50753-XXXSP, use the ROM area from $E800_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 0800_{16} to $1FFF_{16}$ and from 2800_{16} to $3FFF_{16}$, respectively.)

(2) The M50753-PGYS has no options as the M50753-XXXSP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Measured using V_{SS} as base. Output transistor is interrupted.	−0.3~7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, D_0~D_7		−0.3~7	V
V_I	Input voltage IN_0~IN_7		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_3$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3~13	V
V_O	Output voltage X_{OUT}, ϕ, 2ϕ, $\overline{RESET}_{OUT}$, A_0~A_{13}		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM		−0.3~13	V
P_d	Power consumption	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5% and T_a = −10~70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN_0~IN_7, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN_0~IN_7, CNTR $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" Input voltage D_0~D_7	0		0.15V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 1 : "H" input voltage for ports P_0, P_1, P_2, P_3, P_4 and CNTR, $\overline{INT_1}$ and $\overline{INT_2}$ is up to 12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a = 25℃ and $f_{(X_{IN})}$=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}, 2ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $P4_0$~$P4_3$, PWM	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}, 2ϕ	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V			−5	μA
I_{IL}	"L" input current IN_0~IN_7	V_I=0V			−5	μA
I_{IL}	"L" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=12V			12	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V (when not selected)			5	μA
I_{IH}	"H" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I=5V			5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V			5	mA
I_{CC}	Supply current	The output pin is left open, P0, P1, P2, P3 and P4 are connected to V_{CC} and all other input and I/O pins are connected to V_{SS}.		3	6	mA
I_{ACC}	A-D supply current	During A/D converter operation		2	4	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25°C and $f_{X_{IN}}$=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
						LSB
R_{LADDER}	Ladder resistance value		1			kΩ
t_{CONV}	Conversion time				72	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V