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VC0301L USB PC Camera Processor

Datasheet

Version 1.0

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Manual Part Number

0301L-1010
Vimicro Corporation

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1. General Description

The VC0301L chip provides a cost effective single chip solution for the PC camera application. It communicates with PC host via Universal Serial Bus (USB) port. All major image processing functions including image signal processing (ISP), image compression and data transfer units are built in the chip.

VC0301L is designed as a cost-effective single-chip device replacing the complex and costly chip sets used in current PC camera designs with embedded USB device controller and transceiver, 48-LQFP package, and no external DRAM requirement. Advanced on-chip image signal processor and JPEG encoder produce images with superior quality.

2. VC0301L System Block Diagram

Figure 2-1 shows the system block diagram of a typical PC camera phone. VC0301L is between the image sensor and the computer, enabling the computer to capture and display still images and video stream at real-time.

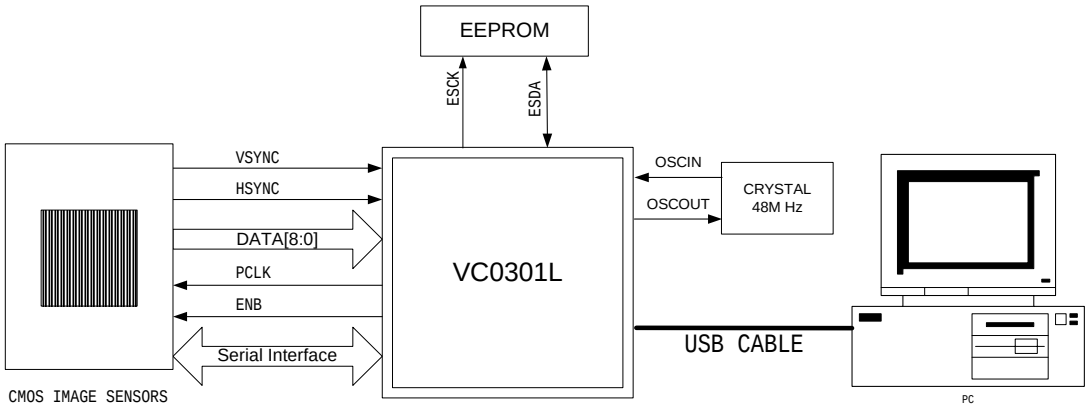

Figure 2.1 USB PC Camera System Block Diagram

3. VC0301L General Features

- Low cost, single chip solution for high resolution USB PC camera applications
- Support up to 15 fps VGA video streaming
- USB Device Controller compliant with USB protocol 1.1
- USB parameters configurable through EEPROM
- Support 10/9/8-bit RGB Bayer pattern raw data input from CMOS image sensors
- Support programmable color correction and gamma correction
- Support ISO/IEC 10918-1 (JPEG) standard image compression
- Support 4 quantization tables for programmable image quality
- Support raw data output for high quality still image
- 3.3V I/O, 1.8V core
- No external DRAM required
- Flexible system level solution support

4. VC0301L Chip Block Diagram

Figure 4-1 shows the block diagram of VC0301L. The ISP block receives RGB raw data from CMOS image sensor interface and performs various image processing tasks such as white balance, color correction, gamma correction, and edge enhancement. The Sub-sample & Raster block handles the input image data scaling and converts input image data to 8x8 block data format required by DCT module. The JPEG Encoder block compresses the image data from ISP block into JPEG format data. The compressed image data is then transferred to PC host via USB Device Controller (UDC) block for display.

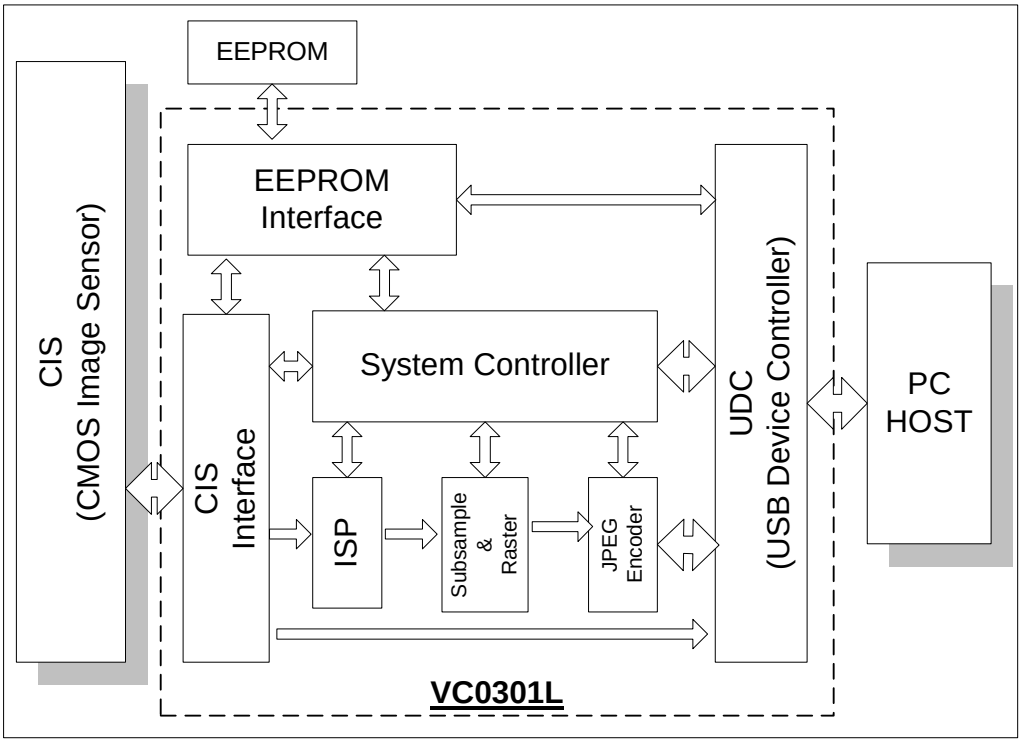

FIGURE 4.1 BLOCK DIAGRAM OF VC0301L

5. Pin Definition

5.1 Pin Assignment

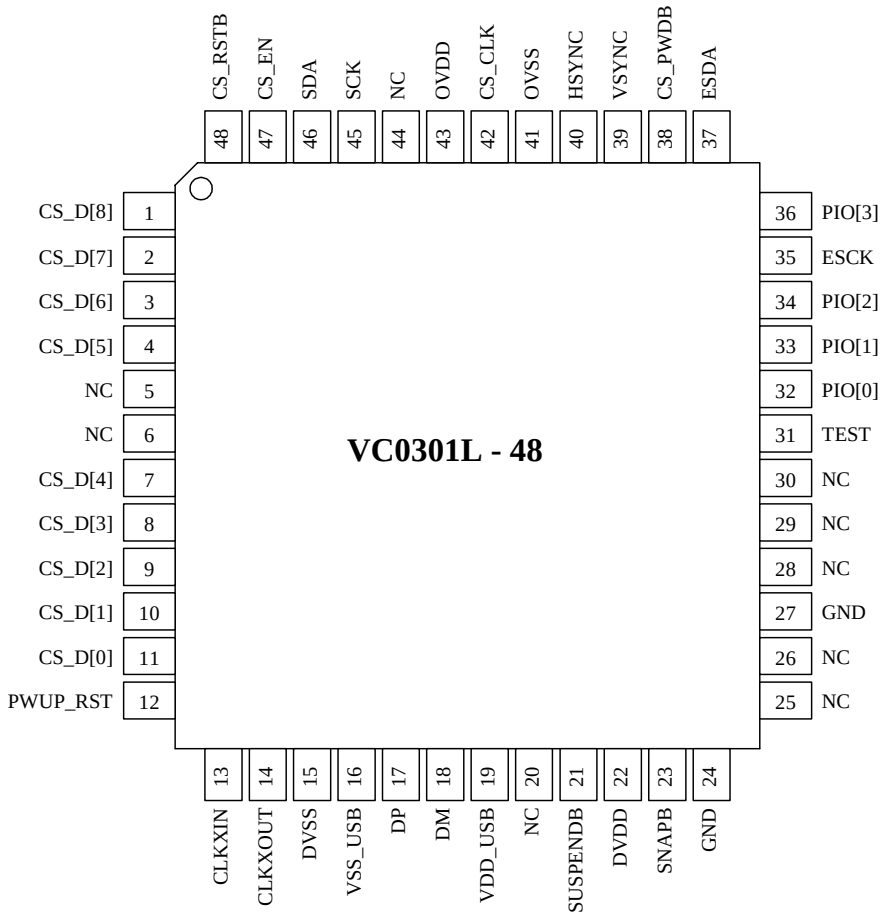

FIGURE 5.1 48-PIN LQFP PACKAGE

5.2 Pin Description

Pin	Type	Function	48 Pin LQFP
CS_D[8]	I, PD	Sensor data	1
CS_D[7]	I, PD	Sensor data	2
CS_D[6]	I, PD	Sensor data	3
CS_D[5]	I, PD	Sensor data	4
CS_D[4]	I, PD	Sensor data	7
CS_D[3]	I, PD	Sensor data	8
CS_D[2]	I, PD	Sensor data	9
CS_D[1]	I, PD	Sensor data	10
CS_D[0]	I, PD	Sensor data	11
PWUP_RST	I, Schmitt	Power on reset, active low	12
CLKXIN	I	Crystal input	13
CLKXOUT	O	Crystal output	14
DVSS	P	Core ground	15
VSS_USB	P	USB transceiver ground	16
DP	I/O	USB data	17
DM	I/O	USB data	18
VDD_USB	P	USB transceiver power	19
SUSPENDB	O	Active-low suspend	21
DVDD	P	Core power	22
SNAPB	I, PU	Snapshot and remote wake up, active low	23
GND	P	Ground	24
GND	P	Ground	27
TEST	I, PD	Manufacturing test mode	31
PIO[0]	I/O, PD	General purpose I/O	32
PIO[1]	I/O, PD	General purpose I/O	33
PIO[2]	I/O, PD	General purpose I/O	34
ESCK	O	SEEPROM clock	35
PIO[3]	I/O, PD	General purpose I/O	36
ESDA	I/O, Schmitt	EEPROM data	37
CS_PWDB	O	Power-down pin controlling DC/DC regulator	38
VSYNC	I/O, PD	Vertical synchronous signal	39
HSYNC	I/O, PD	Horizontal synchronous signal	40
OVSS	P	I/O ground	41
CS_CLK	O	Sensor clock	42
OVDD	P	I/O power	43
SCK / SICLK	O, PD	Serial interface clock	45
SDA / SIVAL	I/O, Schmitt	Serial interface data	46
CS_ENB / SI_EN	O, PD	Sensor power enable / Serial interface enable	47
CS_RSTB / AECNT	O, PD	Sensor reset / auto exposure for TASC VGA sensor	48

TABLE 5.1 VC0301L PIN DESCRIPTIONS

6. Electrical Characteristics

6.1 Absolute Maximum Ratings

Ambient temperature	0 °C to 70 °C
Storage temperature	-40 °C to 125 °C
I/O pin voltage with respect to VSS	-0.3V to VDD + 0.3V

TABLE 6.1 ABSOLUTE MAXIMUM RATINGS

6.2 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
VDD3V	3.3V Power Supply		3.0	3.6	V
VDD1V	1.8V Power Supply		1.65	1.95	V
V_{il}	Input Low voltage		-0.5	1.0	V
V_{ih}	Input High voltage		2.3	5.5	V
V_{ol}	Output Low Voltage		-	0.4	V
V_{oh}	Output High Voltage		2.4	-	V

TABLE 6.2 DC CHARACTERISTICS

6.3 Working Current

Current / Mode style	3.3V_IO (mA)	1.8V_Core (mA)
Normal Mode	15	20
Suspend Mode	0.25	0.02

TABLE 6.3 WORKING CURRENT

6.4 AC Timing

6.4.1 USB Transceiver AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FR}	Rise time	CL=50p	4	20		ns
T_{FF}	Fall time	CL=50p	4	20		ns
T_{FRFF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	90	111.11		%

TABLE 6.4 FULL-SPEED DRIVER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{LR}	Rise time	CL=50p CL=600p	75		300	ns
T_{LF}	Fall time	CL=50p CL=600p	75		300	ns
T_{LRLF}	Rise and fall time matching	$T_{LRLF}=T_{LR}/T_{LF}$	80		125	%

TABLE 6.5 LOW-SPEED DRIVER ELECTRICAL CHARACTERISTICS

6.4.2 RESET Timing AC Characteristics

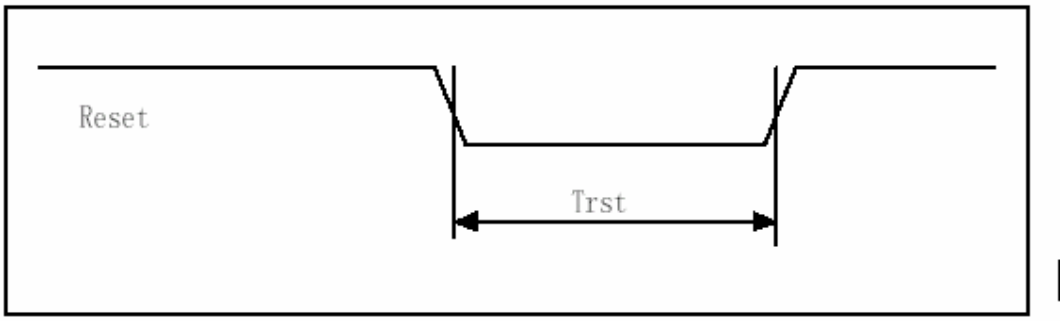

FIGURE 6.1 RESET TIMING AC CHARACTERISTICS DIAGRAM

Symbol	Parameter	Conditions	Min	Max	Unit
T_{rst}	Reset Pulse Width		--	20	ms

TABLE 6.6 RESET SIGNAL AC CHARACTERISTICS

6.4.3 Clock AC Characteristics

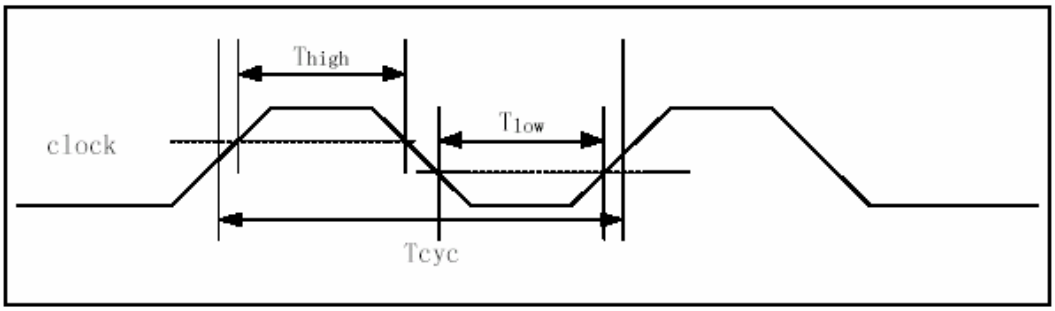

FIGURE 6.2 CLOCK TIMING AC CHARACTERISTICS DIAGRAM

Symbol	Parameter	Conditions	Min	Max	Unit
1/Tcyc	Oscillator Frequency	48@10PPM	-	-	MHz
T_{high}	Oscillator Clock High Time		8.3	-	ns
T_{low}	Oscillator Clock Low Time		8.3	-	ns

TABLE 6.7 CLOCK SIGNAL AC CHARACTERISTICS

6.4.4 Input Signal AC Characteristics

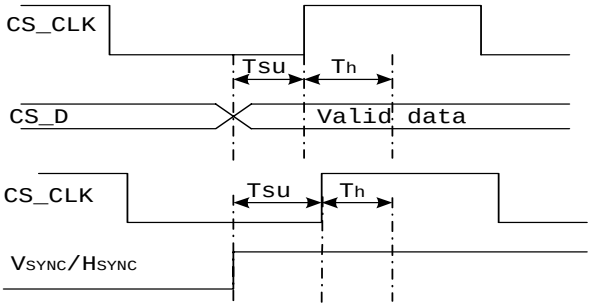

FIGURE 6.3 INPUT SIGNAL AC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
T_{su}	Input setup time		-	45	ns
T_h	Input hold time		0	-	ns

TABLE 6.8 CS_D INPUT SIGNAL AC CHARACTERISTICS

Symbol	parameter	conditions	Min	Max	Unit
T_{su}	Input setup time		-	20	ns
T_h	Input hold time		0	-	ns

TABLE 6.9 VSYNC / HSYNC INPUT AC CHARACTERISTICS

6.4.5 Output Signal AC Characteristic

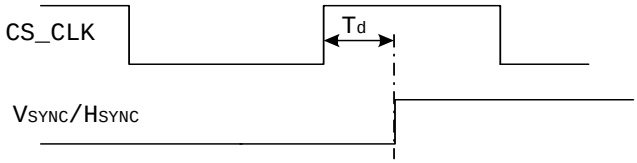

FIGURE 6.4 VSYNC/HSYNC OUTPUT AC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
T_d	Output delay		-	1.5	ns

TABLE 6.10 VSYNC/HSYNC OUTPUT AC CHARACTERISTICS

6.4.6 Serial Bus AC Timing

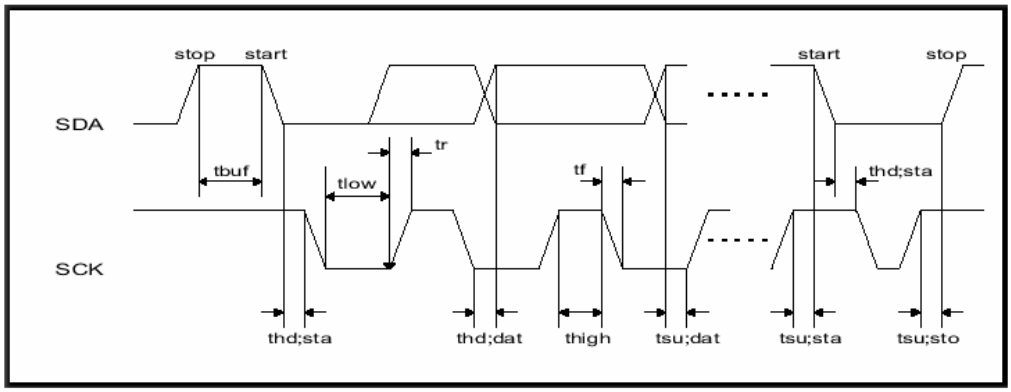

FIGURE 6.5 SERIAL BUS TIMING DIAGRAM

Parameter	Symbol	Min	Max.	Unit
SCK clock frequency	f_{sck}	0	100	KHz
Time that serial bus must be free before a new transmission can start	t_{buf}	4.7	-	us
Hold time for a START	$t_{hd};S_{ta}$	4.0	-	us
LOW period of SCK	t_{low}	4.7	-	us
HIGH period of SCK	t_{high}	4.0	-	us
Setup time for START	$t_{su};S_{ta}$	4.7	-	us
Data hold time	$t_{hd};d_{at}$	0	-	us
Data setup time	$t_{su};d_{at}$	200	-	ns
Rise time of both SDA and SCK	t_r	-	1	us
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};S_{tp}$	4.7	-	us
Capacitive load of each bus lines (SDA, SCK)	C_b	-	-	pf

TABLE 6.11 Serial Bus Timing Table

7. VC0301L Key Function Blocks

7.1 Image Sensor Interfaces

- Support off-the-shelf CMOS image sensors
- 10/9/8-bit RGB raw data input

7.2 USB Features

- Built-in USB transceiver
- Suspend and Remote wakeup
- When audio function is enabled, interface 0 is for video transfer, interface 1 and 2 are for audio control and audio transfer. When audio function is disabled, interface 0 is for video transfer.
- Programmable OEM USB parameters by EEPROM including: vendor ID, product ID, MaxPower, serial number, manufacturer descriptor, and product descriptor and chip revision.

7.3 Image Signal Processing

- Hardware Dead Pixel Compensation
- 2-wire/3-wire serial bus interface to CMOS image sensor
- Programmable white balance, color correction and gamma correction
- Automatic Exposure (AE), Automatic White Balance (AWB), Automatic Gain Control (AGC)
- Programmable AE/AWB windows
- Edge enhancement and noise removal
- 2x Sub-Sampling

7.4 Raster

- The output data format is 4:2:2 YCbCr
- Change the input image data to 8x8 block data format required by the DCT

7.5 Compression Engine

- Standard JPEG compression engine comply to ISO/IEC 10918-1 specifications
- 2 AC and 2 DC Huffman code table
- 4 quantization tables for flexible image quality control
- Bit Rate Control (BRC) engine
- Programmable simplified JPEG header for better performance
- VGA @ 15fps, CIF/SIF up to 30 fps
- Adjustable frame rate for efficient bandwidth usage

7.6 System Controller

- Control ISP, JPEG, and USB blocks, and configure related control registers
- Generate chip clock
- Error detection and handling through USB interface

8. Package Information

Lead Count		48
Body Size	D1	7
	E1	7
Stand-Off	A1	0.1
Body Thickness	A2	1.4
Lead Width	b	0.2
Lead Thickness	c	0.127
Lead Pitch	e	0.5

TABLE 8.1 VC0301L PACKAGE DIMENSION (UNIT: MM)

9. Contact Information

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