SONY

Audio Decoder LSI

CXD5091GG

Description

The CXD5091GG is an audio decoder LSI that achieves super-low power consumption and supports many codecs. Useful interface such as NAND/NOR flash memory and Memory Stick is supported, and it comprises analog circuits such as audio D/A converter and SAR A/D converter. The CXD5091GG is suitable for portable audio players and cellular phone audio backend.

Features

- ◆ CPU : ARM7TDMI
- ◆ RAM : 320K bytes
- ◆ ROM : 448K bytes
- ◆ Frequency : 45.1584MHz
- ◆ Peripherals
  - ◆ Host interface : SRAM, NOR flash slave compatible
    Host processor can be connected.
    16/8-bit data bus, 4-chip select
  - ◆ Bus interface : 16/8-bit data bus, 5-chip select
    An external acknowledge device is also supported.
  - ◆ NAND flash interface : 4-symbol ECC, Reed-Solomon error correction
    4-chip select
  - ◆ DMA controller : × 4ch
  - ◆ Serial interface : × 2ch (1ch supports up to 3Mbps baud rate.)
  - ◆ Clocked serial interface : × 2ch
  - ◆ Memory Stick interface : MS-Pro × 1ch
  - ◆ I^2C bus interface : × 1ch
  - ◆ Audio interface : × 1ch
    Either analog audio interface or I^2S bus interface can be selected as transfer protocol.
  - ◆ USB2.0 : PHY included, Low/Full/High-speed device, 5 end points, Control/Interrupt/Bulk/Isochronous transfer
  - ◆ 8-bit timer : × 8ch, internal clock/external event trigger
  - ◆ Watchdog timer : 16-bit × 1ch
  - ◆ PWM pulse generator : 8-bit × 1ch
  - ◆ A/D converter : 10-bit × 8 analog inputs, SAR, 1Msps
  - ◆ Audio D/A converter : 24-bit × 2

- ◆ Sampling rate converter : 8 to 96kHz sampling frequency is converted to 44.1kHz. Peak detection
- ◆ Magic Gate : × 1ch
- ◆ Interrupt controller : External event × 12

◆ General-purpose I/O : 116 (When all multiplexed pins are set as GPIO), Direction individually selected

◆ Signal processing accelerator : Virtual Mobile Engine

◆ Oscillator

- ◆ Main : 45.1584MHz input, Crystal/Ceramic selectable
- ◆ Sub : 12MHz input, Crystal/Ceramic selectable

◆ Process : CMOS 0.13μm

Conventions

In this data sheet abbreviations shown below are used to simplify descriptions.

Abbreviation	Description
fSYS	Frequency of system clock which can be selected either in 45MHz, 22MHz, 11MHz, 5.6MHz, 2.8MHz or 1.4MHz
tSYS	Cycle time of system clock which can be selected either in 22ns, 44ns, 89ns, 177ns, 354ns or 708ns

Pin Configuration

Fig. 1 and Fig. 2 show the package of the CXD5091GG.

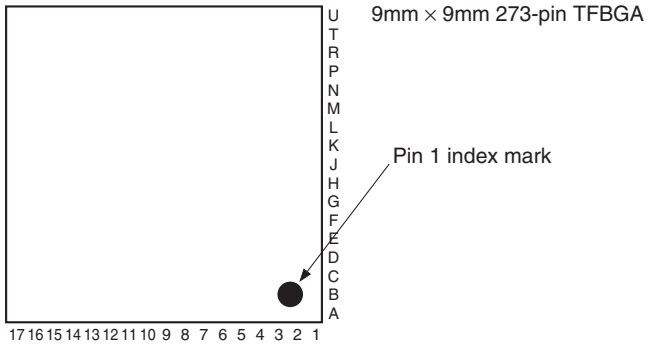


Fig. 1. 273-pin Package (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
U	NC	77	54	92	93	80	82	95	96	120	117	103	102	122	130	135	NC	U
T	52	49	46	72	81	89	94	99	107	105	111	114	116	126	131	133	154	T
R	40	68	71	70	74	78	84	90	101	106	109	118	128	129	134	140	159	R
P	69	67	60	73	61	75	86	88	98	108	115	119	127	132	139	145	125	P
N	64	66	55	47	76	83	87	100	113	121	137	142	141	136	144	150	124	N
M	59	65	53	51	44	42	79	91	97	110	112	147	152	151	146	155	123	M
L	58	63	50	48	43	39						138	161	158	157	160	156	L
K	57	62	45	37	38	29		85	104	153		143	148	162	166	165	149	K
J	56	41	34	33	32	22		242	232	168		173	163	167	171	170	164	J
H	30	36	35	28	24	12		243	233	183		198	178	172	176	175	169	H
G	23	31	19	18	21	9						200	193	181	177	180	174	G
F	20	26	17	14	13	4	261	244	221	215	191	187	188	182	184	185	179	F
E	15	16	7	8	266	262	260	250	234	226	216	210	209	196	192	190	186	E
D	5	11	2	3	263	257	252	247	230	224	217	214	211	197	199	195	189	D
C	27	6	1	269	255	251	246	239	237	231	225	219	207	205	204	194	203	C
B	25	253	10	267	265	259	249	245	241	235	229	227	213	212	201	206	202	B
A	NC	258	256	268	264	254	248	240	238	236	228	222	220	208	223	218	NC	A
	1	2	3	4	5	6	7	8	9	10	1	12	13	14	15	16	17	

Fig. 2. 273-pin Package (Bottom View)

Table 1. Pin Coordinates

Pin No.	Coordinate	Pin name	Pin No.	Coordinate	Pin name
1	C3	NAD0/GPIOC0	38	K5	EVA
2	D3	NAD1/GPIOC1	39	L6	TREQA
3	D4	NAD2/GPIOC2	40	R1	TACK
4	F6	NAD3/GPIOC3	41	J2	SCL/GPIOK0
5	D1	NAD4/GPIOC4	42	M6	SDA/GPIOK1
6	C2	NAD5/GPIOC5	43	L5	EC0/INT6/GPIOL0
7	E3	NAD6/GPIOC6	44	M5	T1/GPIOL1
8	E4	NAD7/GPIOC7	45	K3	EC2/INT7/GPIOL2
9	G6	NCLE/GPIOC8	46	T3	T3/GPIOL3
10	B3	NALE/GPIOC9	47	N4	BEEP/GPIOL4
11	D2	$\overline{\text{NCE0}}$/GPIOC10	48	L4	PWM/SUSPEND/GPIOL5
12	H6	$\overline{\text{NCE1}}$/GPIOC11	49	T2	DVS
13	F5	$\overline{\text{NCE2}}$/GPIOC12	50	L3	DVDIO2
14	F4	$\overline{\text{NCE3}}$/GPIOC13	51	M4	DVDIO2
15	E1	$\overline{\text{NRE}}$/GPIOC14	52	T1	DVS
16	E2	$\overline{\text{NWE}}$/GPIOC15	53	M3	DVDK2
17	F3	$\overline{\text{NWP}}$/GPIOC16	54	U3	DVS
18	G4	$\overline{\text{NRB0}}$/GPIOC17	55	N3	AVDLPF
19	G3	$\overline{\text{NRB1}}$/GPIOC18	56	J1	VREFL
20	F1	$\overline{\text{NRB2}}$/GPIOC19	57	K1	AOUTL
21	G5	$\overline{\text{NRB3}}$/GPIOC20	58	L1	AOUTR
22	J6	DVS	59	M1	VREFR
23	G1	DVDIO2	60	P3	AVSLPF
24	H5	DVDIO2	61	P5	AVDADC
25	B1	DVS	62	K2	AN0
26	F2	DVDK2	63	L2	AN1
27	C1	DVS	64	N1	AN2
28	H4	GPION0/INT8	65	M2	AN3
29	K6	GPION1/INT9	66	N2	AN4
30	H1	GPION2/INT10	67	P2	AN5
31	G2	GPION3/INT11	68	R2	AN6
32	J5	TDI	69	P1	AN7
33	J4	TMS	70	R4	AVSADC
34	J3	TCK	71	R3	NC
35	H3	TDO	72	T4	INT1/GPIOF0
36	H2	$\overline{\text{TRST}}$	73	P4	DREQ/INT2/GPIOF1
37	K4	TEST	74	R5	DACK/INT3/GPIOF2

Pin No.	Coordinate	Pin name	Pin No.	Coordinate	Pin name
75	P6	INT4/GPIOF3	112	M11	$\overline{\text{SCS0}}$/GPIOG2
76	N5	INT5/GPIOF4	113	N9	SI1/GPIOH1
77	U2	DVS	114	T12	SO1/GPIOH0
78	R6	DVDIO2	115	P11	$\overline{\text{SCK1}}$
79	M7	DVDK2	116	T13	$\overline{\text{SCS1}}$/GPIOH2
80	U6	DVS	117	U11	DVS
81	T5	DVDIO2	118	R12	DVDIO1
82	U7	DVS	119	P12	DVDIO1
83	N6	MSBS/INT0/GPIOE0	120	U10	DVS
84	R7	MSSCLK	121	N10	DVDK1
85	K8	MSDIO0/GPIOE1	122	U14	DVS
86	P7	MSDIO1/GPIOE2	123	M17	FS256
87	N7	MSDIO2/GPIOE3	124	N17	LRCK/WS
88	P8	MSDIO3/GPIOE4	125	P17	BCK/SCK
89	T6	$\overline{\text{MSINS}}$/GPIOE5	126	T14	ADDT/SDI/GPIOM0
90	R8	MCSEL	127	P13	DADT/SDO/GPIOM1
91	M8	AVDOSC1	128	R13	MUTFGL/GPIOM2
92	U4	EXTAL	129	R14	MUTFGR/GPIOM3
93	U5	XTAL	130	U15	DVS
94	T7	AVSOSC	131	T15	DVDIO2
95	U8	TEX	132	P14	DVDIO2
96	U9	TX	133	T16	DVS
97	M9	AVDOSC2	134	R15	DVDK2
98	P9	AVSPLL	135	U16	DVS
99	T8	AVDPLL	136	N14	NBOOT
100	N8	AVDUSB	137	N11	A0/GPIOA0
101	R9	AVSUSB	138	L12	A1
102	U13	DP	139	P15	A2
103	U12	DM	140	R16	A3
104	K9	VBUS/GPIOD0	141	N13	A4
105	T10	TxD0/GPIOI0	142	N12	A5
106	R10	RxD0/GPIOI1	143	K12	A6
107	T9	TxD1/GPIOJ0	144	N15	A7
108	P10	RxD1/GPIOJ1	145	P16	A8
109	R11	SI0/GPIOG1	146	M15	A9
110	M10	SO0/GPIOG0	147	M12	A10
111	T11	$\overline{\text{SCK0}}$	148	K13	A11

Pin No.	Coordinate	Pin name	Pin No.	Coordinate	Pin name
149	K17	A12	185	F16	D10/GPIOA14
150	N16	A13	186	E17	D11/GPIOA15
151	M14	A14	187	F12	D12/GPIOA16
152	M13	A15	188	F13	D13/GPIOA17
153	K10	A16	189	D17	D14/GPIOA18
154	T17	DVS	190	E16	D15/GPIOA19
155	M16	DVDIO2	191	F11	$\overline{\text{WAIT}}$/GPIOA20
156	L17	DVDIO2	192	E15	$\overline{\text{CS0}}$/GPIOA21
157	L15	DVS	193	G13	$\overline{\text{CS1}}$/GPIOA22
158	L14	DVDK2	194	C16	$\overline{\text{CS2}}$/GPIOA23
159	R17	DVS	195	D16	$\overline{\text{CS3}}$/GPIOA24
160	L16	A17	196	E14	$\overline{\text{CS4}}$/GPIOA25
161	L13	A18	197	D14	$\overline{\text{RE}}$/GPIOA26
162	K14	A19	198	H12	$\overline{\text{WE}}$/GPIOA27
163	J13	A20	199	D15	$\overline{\text{LB}}$/GPIOA28
164	J17	A21	200	G12	$\overline{\text{UB}}$/GPIOA29
165	K16	A22	201	B15	DVDK2
166	K15	A23/GPIOA1	202	B17	DVS
167	J14	A24/GPIOA2	203	C17	DVS
168	J10	A25/GPIOA3	204	C15	DVDIO2
169	H17	D0/GPIOA4	205	C14	DVDIO2
170	J16	D1/GPIOA5	206	B16	DVS
171	J15	D2/GPIOA6	207	C13	HA0
172	H14	D3/GPIOA7	208	A14	HA1
173	J12	D4/GPIOA8	209	E13	HA2
174	G17	D5/GPIOA9	210	E12	HA3
175	H16	D6/GPIOA10	211	D13	HA4
176	H15	D7/GPIOA11	212	B14	HA5
177	G15	DVS	213	B13	HA6
178	H13	DVDIO2	214	D12	HA7
179	F17	DVDIO2	215	F10	HA8
180	G16	DVS	216	E11	HA9
181	G14	DVDK2	217	D11	HA10
182	F14	DVS	218	A16	DVS
183	H10	D8/GPIOA12	219	C12	DVDIO0
184	F15	D9/GPIOA13	220	A13	DVDIO0

Pin No.	Coordinate	Pin name
221	F9	DVS
222	A12	DVDK0
223	A15	DVS
224	D10	HA11
225	C11	HA12
226	E10	HA13
227	B12	HA14
228	A11	HA15
229	B11	HA16/GPIOB0
230	D9	HA17/GPIOB1
231	C10	HD0/GPIOB2
232	J9	HD1/GPIOB3
233	H9	HD2/GPIOB4
234	E9	HD3/GPIOB5
235	B10	DVS
236	A10	DVDIO0
237	C9	DVDK0
238	A9	DVS
239	C8	DVDIO0
240	A8	DVS
241	B9	HD4/GPIOB6
242	J8	HD5/GPIOB7
243	H8	HD6/GPIOB8
244	F8	HD7/GPIOB9
245	B8	HD8/GPIOB10
246	C7	HD9/GPIOB11
247	D8	HD10/GPIOB12
248	A7	HD11/GPIOB13
249	B7	HD12/GPIOB14
250	E8	HD13 / GPIOB15
251	C6	HD14 / GPIOB16
252	D7	HD15/GPIOB17
253	B2	DVS
254	A6	DVDIO0
255	C5	DVDK0
256	A3	DVS
257	D6	DVDIO0
258	A2	DVS
259	B6	$\overline{\text{RST}}$
260	E7	$\overline{\text{HWAIT}}$/GPIOB18
261	F7	$\overline{\text{HCS}}$/GPIOB19
262	E6	$\overline{\text{HBUS8}}$/GPIOB20
263	D5	HBIG/GPIOB21
264	A5	HADMUX/GPIOB22
265	B5	HALE/GPIOB23
266	E5	$\overline{\text{HRE}}$/GPIOB24
267	B4	$\overline{\text{HWE}}$/GPIOB25
268	A4	$\overline{\text{HLB}}$/GPIOB26
269	C4	$\overline{\text{HUB}}$/GPIOB27

Pin Description

Table 2 shows the pin description.

Table 2. Pin Description

Pin name	Direction	Description	
NAD0/GPIOC0	I/O / I/O	NAND flash address/data bus	GPIO group C 0 to 20
NAD1/GPIOC1	I/O / I/O		
NAD2/GPIOC2	I/O / I/O		
NAD3/GPIOC3	I/O / I/O		
NAD4/GPIOC4	I/O / I/O		
NAD5/GPIOC5	I/O / I/O		
NAD6/GPIOC6	I/O / I/O		
NAD7/GPIOC7	I/O / I/O		
NCLE/GPIOC8	Output / I/O	Command latch enable	
NALE/GPIOC9	Output / I/O	Address latch enable	
$\overline{\text{NCE0}}$/GPIOC10	Output / I/O	NAND chip enable bank 0	
$\overline{\text{NCE1}}$/GPIOC11	Output / I/O	NAND chip enable bank 1	
$\overline{\text{NCE2}}$/GPIOC12	Output / I/O	NAND chip enable bank 2	
$\overline{\text{NCE3}}$/GPIOC13	Output / I/O	NAND chip enable bank 3	
$\overline{\text{NRE}}$/GPIOC14	Output / I/O	NAND read enable	
$\overline{\text{NWE}}$/GPIOC15	Output / I/O	NAND write enable	
$\overline{\text{NWP}}$/GPIOC16	Output / I/O	NAND write protect	
$\overline{\text{NRB0}}$/GPIOC17	Input / I/O	NAND ready/busy bank 0	
$\overline{\text{NRB1}}$/GPIOC18	Input / I/O	NAND ready/busy bank 1	
$\overline{\text{NRB2}}$/GPIOC19	Input / I/O	NAND ready/busy bank 2	
$\overline{\text{NRB3}}$/GPIOC20	Input / I/O	NAND ready/busy bank 3	
GPION0/INT8	I/O / Input	GPIO group N 0 to 3	Interrupt 8 to 11
GPION1/INT9	I/O / Input		
GPION2/INT10	I/O / Input		
GPION3/INT11	I/O / Input		
TDI	Input	Debug data input	
TMS	Input	Debug mode select input	
TCK	Input	Debug clock input	
TDO	Output	Debug data output	
$\overline{\text{TRST}}$	Input	Debug reset input	
SCL/GPIOK0	I/O / I/O	I^2C clock	GPIO group K 0 to 1
SDA/GPIOK1	I/O / I/O	I^2C data	

Pin name	Direction	Description			
EC0/INT6/GPIOL0	Input / Input / I/O	Event clock input 0		Interrupt 6	GPIO group L 0 to 5
T1/GPIOL1	Output / I/O	Event trigger output 1			
EC2/INT7/GPIOL2	Input / Input / I/O	Event clock input 2		Interrupt 7	
T3/GPIOL3	Output / I/O	Event trigger output 3			
BEEP/GPIOL4	Output / I/O	Beep output			
PWM/SUSPEND/ GPIOL5	Output / Output / I/O	PWM output	USB2.0 suspend status		
VREFL	Output	LPF reference voltage output (Lch)			
AOUTL	Output	LPF output (Lch)			
AOUTR	Output	LPF output (Rch)			
VREFR	Output	LPF reference voltage output (Rch)			
AN0	Input	SAR A/D converter analog input (ch0)			
AN1	Input	SAR A/D converter analog input (ch1)			
AN2	Input	SAR A/D converter analog input (ch2)			
AN3	Input	SAR A/D converter analog input (ch3)			
AN4	Input	SAR A/D converter analog input (ch4)			
AN5	Input	SAR A/D converter analog input (ch5)			
AN6	Input	SAR A/D converter analog input (ch6)			
AN7	Input	SAR A/D converter analog input (ch7)			
INT1/GPIOF0	Input / I/O	—		Interrupt 1 to 5	GPIO group F 0 to 4
DREQ/INT2/GPIOF1	Input / Input / I/O	BIU external acknowledge device DMA request input			
DACK/INT3/GPIOF2	Output / Input / I/O	BIU external acknowledge device DMA request output			
INT4/GPIOF3	Input / I/O	—			
INT5/GPIOF4	Input / I/O	—			
MSSCLK	Output	MS Pro I/F clock output			
MSBS/INT0/GPIOE0	Output / Input / I/O	MS Pro I/F bus state output	Interrupt 0	GPIO group E 0 to 5	
MSDIO0/GPIOE1	I/O / I/O	MS Pro I/F data 0 to 3 I/O			
MSDIO1/GPIOE2	I/O / I/O				
MSDIO2/GPIOE3	I/O / I/O				
MSDIO3/GPIOE4	I/O / I/O				
MSINSN/GPIOE5	Input / I/O	MS Pro I/F attach detection			
MCSEL	Input	Main oscillator ceramic select. H: ceramic, L: crystal			
EXTAL	Input	Main oscillator 45.1584MHz input			
XTAL	Output	Main oscillator output			
TEX	Input	Sub oscillator 12MHz input			
TX	Output	Sub oscillator output			

Pin name	Direction	Description		
DP	I/O	USB2.0 D+		
DM	I/O	USB2.0 D–		
VBUS/GPIOD0	Input / I/O	USB2.0 VBUS interrupt	GPIO group D 0	
TxD0/GPIOI0	Output / I/O	UART0 transmit data	GPIO group I 0 to 1	
RxD0/GPIOI1	Input / I/O	UART0 receive data		
TxD1/GPIOJ0	Output / I/O	UART1 transmit data	GPIO group J 0 to 1	
RxD1/GPIOJ1	Input / I/O	UART1 receive data		
SO0/GPIOG0	Output / I/O	Clocked serial 0 transmit data	GPIO group G 0 to 2	
SI0/GPIOG1	Input / I/O	Clocked serial 0 receive data		
$\overline{\text{SCS0}}$/GPIOG2	Input / I/O	Clocked serial 0 external start trigger		
$\overline{\text{SCK0}}$	I/O	Clocked serial 0 clock		
SO1/GPIOH0	Output / I/O	Clocked serial 1 transmit data	GPIO group H 0	
SI1/GPIOH1	Input / Input	Clocked serial 1 receive data	GPIO group H 1	
$\overline{\text{SCS1}}$/GPIOH2	Input / I/O	Clocked serial 1 external start trigger	GPIO group H 2	
$\overline{\text{SCK1}}$	I/O	Clocked serial 1 clock		
FS256	Output	256fs (11.2896MHz) clock output		
LRCK/WS	I/O / I/O	Audio serial LR clock	I^2S word select	
BCK/SCK	I/O / I/O	Audio serial bit clock	I^2S clock	
ADDT/SDI/GPIOM0	Input / Input / I/O	Audio serial data input	I^2S data input	GPIO group M 0 to 3
DADT/SDO/GPIOM1	Output / Output / I/O	Audio serial data output	I^2S data output	
MUTFGL/GPIOM2	Output / I/O	Mute (Lch) output		
MUTFGR/GPIOM3	Output / I/O	Mute (Rch) output		
NBOOT	Input	NAND flash ROM boot select. H: NAND boot, L: NOR boot		

Pin name	Direction	Description	
A0/GPIOA0	Output / I/O	BIU address 0	GPIO group A 0
A1	Output	BIU address 1 to 22	
A2	Output		
A3	Output		
A4	Output		
A5	Output		
A6	Output		
A7	Output		
A8	Output		
A9	Output		
A10	Output		
A11	Output		
A12	Output		
A13	Output		
A14	Output		
A15	Output		
A16	Output		
A17	Output		
A18	Output		
A19	Output		
A20	Output		
A21	Output		
A22	Output		
A23/GPIOA1	Output / I/O	BIU address 23 to 25	GPIO group A 1 to 3
A24/GPIOA2	Output / I/O		
A25/GPIOA3	Output / I/O		

Pin name	Direction	Description	
D0/GPIOA4	I/O / I/O	BIU data 0 to 15	GPIO group A 4 to 29
D1/GPIOA5	I/O / I/O		
D2/GPIOA6	I/O / I/O		
D3/GPIOA7	I/O / I/O		
D4/GPIOA8	I/O / I/O		
D5/GPIOA9	I/O / I/O		
D6/GPIOA10	I/O / I/O		
D7/GPIOA11	I/O / I/O		
D8/GPIOA12	I/O / I/O		
D9/GPIOA13	I/O / I/O		
D10/GPIOA14	I/O / I/O		
D11/GPIOA15	I/O / I/O		
D12/GPIOA16	I/O / I/O		
D13/GPIOA17	I/O / I/O		
D14/GPIOA18	I/O / I/O		
D15/GPIOA19	I/O / I/O		
$\overline{\text{WAIT}}$/GPIOA20	Input / I/O	BIU wait input	
$\overline{\text{CS0}}$/GPIOA21	Output / I/O	BIU chip select bank 0	
$\overline{\text{CS1}}$/GPIOA22	Output / I/O	BIU chip select bank 1	
$\overline{\text{CS2}}$/GPIOA23	Output / I/O	BIU chip select bank 2	
$\overline{\text{CS3}}$/GPIOA24	Output / I/O	BIU chip select bank 3	
$\overline{\text{CS4}}$/GPIOA25	Output / I/O	BIU chip select bank 4	
$\overline{\text{RE}}$/GPIOA26	Output / I/O	BIU read enable	
$\overline{\text{WE}}$/GPIOA27	Output / I/O	BIU write enable	
$\overline{\text{LB}}$/GPIOA28	Output / I/O	BIU lower byte enable	
$\overline{\text{UB}}$/GPIOA29	Output / I/O	BIU upper byte enable	
$\overline{\text{RST}}$	Input	System reset	

Pin name	Direction	Description
HA0	I/O	HOST I/F address input, data I/O (address/data multiplex mode)
HA1	I/O	
HA2	I/O	
HA3	I/O	
HA4	I/O	
HA5	I/O	
HA6	I/O	
HA7	I/O	
HA8	I/O	
HA9	I/O	
HA10	I/O	
HA11	I/O	
HA12	I/O	
HA13	I/O	
HA14	I/O	
HA15	I/O	

Pin name	Direction	Description	
HA16/GPIOB0	Input / I/O	HOST I/F address input	GPIO group B 0 to 27
HA17/GPIOB1	Input / I/O		
HD0/GPIOB2	I/O / I/O	Host I/F data I/O (Address/data separate mode)	
HD1/GPIOB3	I/O / I/O		
HD2/GPIOB4	I/O / I/O		
HD3/GPIOB5	I/O / I/O		
HD4/GPIOB6	I/O / I/O		
HD5/GPIOB7	I/O / I/O		
HD6/GPIOB8	I/O / I/O		
HD7/GPIOB9	I/O / I/O		
HD8/GPIOB10	I/O / I/O		
HD9/GPIOB11	I/O / I/O		
HD10/GPIOB12	I/O / I/O		
HD11/GPIOB13	I/O / I/O		
HD12/GPIOB14	I/O / I/O		
HD13/GPIOB15	I/O / I/O		
HD14/GPIOB16	I/O / I/O		
HD15/GPIOB17	I/O / I/O		
$\overline{\text{HWAIT}}$/GPIOB18	Output / I/O	Host I/F wait output	
$\overline{\text{HCS}}$/GPIOB19	Input / I/O	Host I/F chip select	
$\overline{\text{HBUS8}}$/GPIOB20	Input / I/O	Host I/F 8/16-bit data select	
HBIG/GPIOB21	Input / I/O	Host I/F endianness select	
HADMUX/GPIOB22	Input / I/O	Address/data separate, multiplex select	
HALE/GPIOB23	Input / I/O	Address latch enable (address data mux)	
$\overline{\text{HRE}}$/GPIOB24	Input / I/O	Host I/F read enable	
$\overline{\text{HWE}}$/GPIOB25	Input / I/O	Host I/F write enable	
$\overline{\text{HLB}}$/GPIOB26	Input / I/O	Host I/F lower byte enable	
$\overline{\text{HUB}}$/GPIOB27	Input / I/O	Host I/F upper byte enable	

Power Supply/GND Pins

Table 3 shows the correspondence of power supply/GND pins to general pins.

Table 3. Power Supply/GND Correspondence to General Pins

Power supply pin	GND pin	Digital/ Analog	Pins
DVDIO0	DVS	Digital I/O 0	HA0, HA1, HA2, HA3, HA4, HA5, HA6, HA7, HA8, HA9, HA10, HA11, HA12, HA13, HA14, HA15, HA16/GPIOB0, HA17/GPIOB1, HD0/GPIOB2, HD1/GPIOB3, HD2/GPIOB4, HD3/GPIOB5, HD4/GPIOB6, HD5/GPIOB7, HD6/GPIOB8, HD7/GPIOB9, HD8/GPIOB10, HD9/GPIOB11, HD10/GPIOB12, HD11/GPIOB13, HD12/GPIOB14, HD13/GPIOB15, HD14/GPIOB16, HD15/GPIOB17, HWAIT/GPIOB18, HCS/GPIOB19, HBUS8/GPIOB20, HBIG/GPIOB21, HADMUX/GPIOB22, HALE/GPIOB23, HRE/GPIOB24, HWE/GPIOB25, HLB/GPIOB26, HUB/GPIOB27, RST
DVDK0		Digital core 0	
DVDIO1		Digital I/O 1	VBUS/GPIOD0, TxD0/GPIOI0, RxD0/GPIOI1, TxD1/GPIOJ0, RxD1/GPIOJ1, SI0/GPIOG1, SO0/GPIOG0, SCK0, SCS0/GPIOG2, SI1/GPIOH1, SO1/GPIOH0, SCK1, SCS1/GPIOH2, FS256, LRCK/WS, BCK/SCK, ADDT/SDI/GPIOM0, DADT/SDO/GPIOM1, MUTFGL/GPIOM2, MUTFGR/GPIOM3
DVDK1		Digital core 1	
DVDIO2		Digital I/O 2	NAD0/GPIOC0, NAD1/GPIOC1, NAD2/GPIOC2, NAD3/GPIOC3, NAD4/GPIOC4, NAD5/GPIOC5, NAD6/GPIOC6, NAD7/GPIOC7, NCLE/GPIOC8, NALE/GPIOC9, NCE0/GPIOC10, NCE1/GPIOC11, NCE2/GPIOC12, NCE3/GPIOC13, NRE/GPIOC14, NWE/GPIOC15, NWP/GPIOC16, NRB0/GPIOC17, NRB1/GPIOC18, NRB2/GPIOC19, NRB3/GPIOC20, GPION0/INT8, GPION1/INT9, GPION2/INT10, GPION3/INT11, TDI, TMS, TCK, TDO, TRST, TEST, EVA, TREQA, TACK, SCL/GPIOK0, SDA/GPIOK1, EC0/INT6/GPIOL0, T1/GPIOL1, EC2/INT7/GPIOL2, T3/GPIOL3, BEEP/GPIOL4, PWM/SUSPEND/GPIOL5, INT1/GPIOF0, DREQ/INT2/GPIOF1, DACK/INT3/GPIOF2, INT4/GPIOF3, INT5/GPIOF4, MSBS/INT0/GPIOE0, MSSCLK, MSDIO0/GPIOE1, MSDIO1/GPIOE2, MSDIO2/GPIOE3, MSDIO3/GPIOE4, MSINS/GPIOE5, MCSEL, NBOOT, A0/GPIOA0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23/GPIOA1, A24/GPIOA2, A25/GPIOA3, D0/GPIOA4, D1/GPIOA5, D2/GPIOA6, D3/GPIOA7, D4/GPIOA8, D5/GPIOA9, D6/GPIOA10, D7/GPIOA11, D8/GPIOA12, D9/GPIOA13, D10/GPIOA14, D11/GPIOA15, D12/GPIOA16, D13/GPIOA17, D14/GPIOA18, D15/GPIOA19, WAIT/GPIOA20, CS0/GPIOA21, CS1/GPIOA22, CS2/GPIOA23, CS3/GPIOA24, CS4/GPIOA25, RE/GPIOA26, WE/GPIOA27, LB/GPIOA28, UB/GPIOA29
DVDK2		Digital core 2	
AVDLPF	AVSLPF	Analog	VREFL, AOUTL, AOUTR, VREFR
AVDADC	AVSADC	Analog	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7
AVDOSC1	AVSOSC	Analog	EXTAL, XTAL
AVDOSC2		Analog	TEX, TX
AVDPLL	AVSPLL	Analog	
AVDUSB	AVSUSB	Analog	DP, DM

State of Pins

Table 4 shows the state of pins at certain conditions.

Table 4. State of Pins

Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
NAD0/GPIOC0	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD1/GPIOC1	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD2/GPIOC2	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD3/GPIOC3	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD4/GPIOC4	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD5/GPIOC5	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD6/GPIOC6	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NAD7/GPIOC7	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NCLE/GPIOC8	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
NALE/GPIOC9	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{NCE0}}$/GPIOC10	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{NCE1}}$/GPIOC11	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{NCE2}}$/GPIOC12	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{NCE3}}$/GPIOC13	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{NRE}}$/GPIOC14	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{NWE}}$/GPIOC15	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{NWP}}$/GPIOC16	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{NRB0}}$/GPIOC17	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 1
$\overline{\text{NRB1}}$/GPIOC18	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 1
$\overline{\text{NRB2}}$/GPIOC19	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 1
$\overline{\text{NRB3}}$/GPIOC20	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 1
GPION0/INT8	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 2
GPION1/INT9	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 2
GPION2/INT10	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 2
GPION3/INT11	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 2
TDI	Input	Test pin	Pull-up		Open	Input Note 3
TMS	Input	Test pin	Pull-up		Open	Input Note 3
TCK	Input	Test pin	Pull-up		Open	Input Note 3
TDO	Low output	Test pin		DI_{OH1}, DI_{OL1}	Open	Output Note 5
$\overline{\text{TRST}}$	Input	Test pin	None		DVDIO2	Input Note 3
TEST	Input	Test pin	Pull-down		Open	Input Note 3
EVA	Input	Test pin	Pull-down		Open	Input Note 3
TREQA	Input	Test pin	Pull-down		Open	Input Note 3

Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
TACK	Low output	Test pin		DI_{OH1}, DI_{OL1}	Open	Output Note 5
SCL/GPIOK0	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 7
SDA/GPIOK1	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 6
EC0/INT6/GPIOL0	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 2
T1/GPIOL1	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
EC2/INT7/GPIOL2	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 2
T3/GPIOL3	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
BEEP/GPIOL4	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
PWM/SUSPEND/ GPIOL5	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
VREFL	Unknown output	Functional			Open	Analog
AOUTL	Unknown output	Functional			Open	Analog
AOUTR	Unknown output	Functional			Open	Analog
VREFR	Unknown output	Functional			Open	Analog
AN0	Input	Functional			Open	Analog
AN1	Input	Functional			Open	Analog
AN2	Input	Functional			Open	Analog
AN3	Input	Functional			Open	Analog
AN4	Input	Functional			Open	Analog
AN5	Input	Functional			Open	Analog
AN6	Input	Functional			Open	Analog
AN7	Input	Functional			Open	Analog
INT1/GPIOF0	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
DREQ/INT2/GPIOF1	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
DACK/INT3/GPIOF2	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
INT4/GPIOF3	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
INT5/GPIOF4	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
MSSCLK	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
MSBS/INT0/GPIOE0	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 2
MSDIO0/GPIOE1	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
MSDIO1/GPIOE2	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
MSDIO2/GPIOE3	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
MSDIO3/GPIOE4	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{MSINS}}$/GPIOE5	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 2
MCSEL	Input	Functional	None		DVS	Input Note 3

Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
EXTAL	Input	Functional			Open	Analog
XTAL	Unknown output	Functional			Open	Analog
TEX	Input	Functional			Open	Analog
TX	Unknown output	Functional			Open	Analog
DP	Input	Functional			Open	Analog
DM	Input	Functional			Open	Analog
VBUS/GPIOD0	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
TxD0/GPIOI0	High output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
RxD0/GPIOI1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
TxD1/GPIOJ0	High output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
RxD1/GPIOJ1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
SO0/GPIOG0	Low output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
SI0/GPIOG1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
$\overline{SCS0}$/GPIOG2	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
$\overline{SCK0}$	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 2
SO1/GPIOH0	Low output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
SI1/GPIOH1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
$\overline{SCS1}$/GPIOH2	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 1
$\overline{SCK1}$	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO1	I/O Note 2
FS256	Low output	Functional		DI_{OH1}, DI_{OL1}	Open	Output Note 5
LRCK/WS	Low output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
BCK/SCK	Low output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
ADDT/SDI/GPIOM0	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
DADT/SDO/GPIOM1	Low output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
MUTFGL/GPIOM2	High output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
MUTFGR/GPIOM3	High output	Functional	None	DI_{OH1}, DI_{OL1}	Open	I/O Note 1
NBOOT	Input	Functional	Pull-down		Open	Input Note 3
A0/GPIOA0	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
A1	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A2	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A3	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A4	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A5	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A6	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A7	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A8	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5

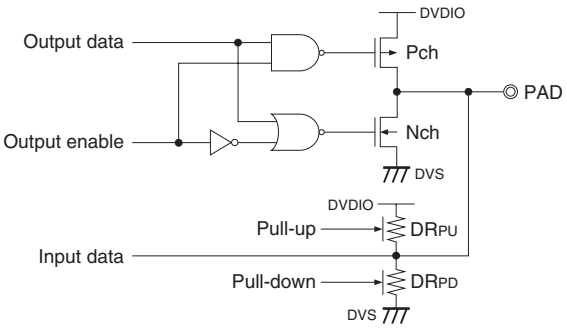
Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
A9	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A10	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A11	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A12	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A13	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A14	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A15	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A16	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A17	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A18	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A19	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A20	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A21	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A22	Low output	Functional		DI_{OH2}, DI_{OL2}	Open	Output Note 5
A23/GPIOA1	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
A24/GPIOA2	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
A25/GPIOA3	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D0/GPIOA4	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D1/GPIOA5	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D2/GPIOA6	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D3/GPIOA7	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D4/GPIOA8	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D5/GPIOA9	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D6/GPIOA10	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D7/GPIOA11	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D8/GPIOA12	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D9/GPIOA13	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D10/GPIOA14	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D11/GPIOA15	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D12/GPIOA16	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D13/GPIOA17	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D14/GPIOA18	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
D15/GPIOA19	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{WAIT}}$/GPIOA20	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVDIO2	I/O Note 1
$\overline{\text{CS0}}$/GPIOA21	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{CS1}}$/GPIOA22	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{CS2}}$/GPIOA23	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{\text{CS3}}$/GPIOA24	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1

Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
$\overline{CS4}$/GPIOA25	Input	GPIO	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
$\overline{RE}$/GPIOA26	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{WE}$/GPIOA27	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{LB}$/GPIOA28	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{UB}$/GPIOA29	Input	GPIO	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HA0	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA2	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA3	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA4	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA5	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA6	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA7	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA8	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA9	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA10	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA11	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA12	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA13	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA14	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA15	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA16/GPIOB0	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HA17/GPIOB1	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HD0/GPIOB2	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD1/GPIOB3	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD2/GPIOB4	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD3/GPIOB5	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD4/GPIOB6	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD5/GPIOB7	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD6/GPIOB8	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD7/GPIOB9	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD8/GPIOB10	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD9/GPIOB11	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD10/GPIOB12	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD11/GPIOB13	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD12/GPIOB14	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD13/GPIOB15	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
HD14/GPIOB16	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1

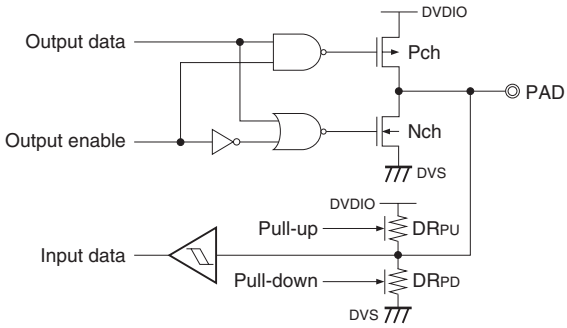
Pin name	On reset/ after reset, state of pins	On reset/ after reset, description	On reset/ after reset, pull-up or pull-down	Output drivability*1	Termination when not used	I/O type
HD15/GPIOB17	Input	Functional	None	DI_{OH2}, DI_{OL2}	DVS	I/O Note 1
$\overline{\text{HWAIT}}$/GPIOB18	High output	Functional	None	DI_{OH2}, DI_{OL2}	Open	I/O Note 1
$\overline{\text{HCS}}$/GPIOB19	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{HBUS8}}$/GPIOB20	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
HBIG/GPIOB21	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
HADMUX/GPIOB22	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVS	I/O Note 1
HALE/GPIOB23	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{HRE}}$/GPIOB24	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{HWE}}$/GPIOB25	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{HLB}}$/GPIOB26	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{HUB}}$/GPIOB27	Input	Functional	None	DI_{OH1}, DI_{OL1}	DVDIO0	I/O Note 1
$\overline{\text{RST}}$	Input	Functional	None		DVS	Input Note 4

*1 For DI_{OH1}, DI_{OL1}, DI_{OH2} and DI_{OL2}, refer to Table 7 Electrical Characteristics.

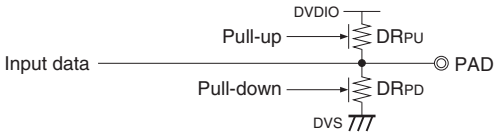
The I/O types in Table 4 are illustrated below.



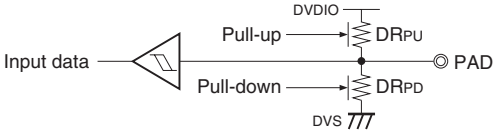
Note 1. I/O



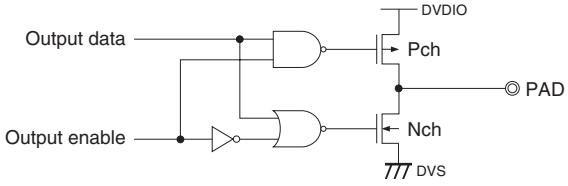
Note 2. I/O (Schmitt Input)



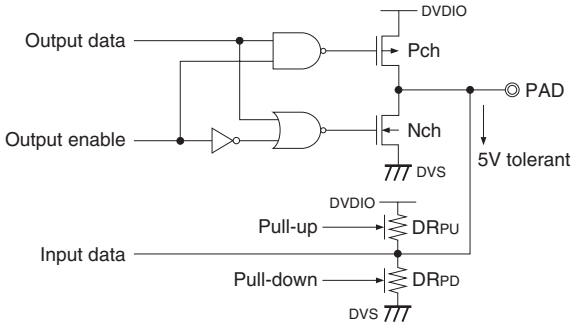
Note 3. Input



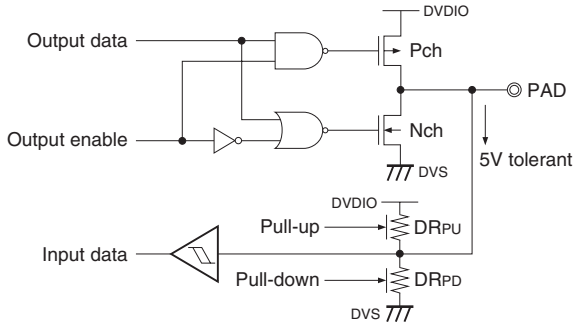
Note 4. Input (Schmitt Input)



Note 5. Output



Note 6. I/O (5V Tolerant)



Note 7. I/O (5V Tolerant, Schmitt Input)

Electrical Characteristics and Operating Conditions

1. Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Item		Symbol	Min.	Max.	Unit
Digital I/O power supply 0 to 2		DVDIO0-2	–0.3	4.0	V
Digital core power supply 0 to 2		DVDK0-2	–0.3	1.68	V
Digital input voltage	SCL/GPIOK0, SDA/GPIOK1	DIV	–0.3	7.0	V
	All other digital inputs		–0.3	4.0	V
Digital output voltage	High output	DOV	—	DVDIO0-2 + 0.3	V
	Low output		–0.3	—	V
Audio LPF power supply		AVDLPF	–0.3	3.6	V
SAR A/D converter power supply		AVDADC	–0.3	1.68	V
Main oscillator power supply		AVDOSC1	–0.3	1.68	V
Sub oscillator power supply		AVDOSC2	–0.3	1.68	V
PLL power supply		AVDPLL	–0.3	1.68	V
USB PHY power supply		AVDUSB	–0.3	3.6	V
Storage temperature		Tstg	–40	+150	℃

2. Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit
Digital I/O power supply 0 to 2	SCL/GPIOK0, SDA/GPIOK1	DVDIO0-2	1.8	2.8	3.6	V
	All other digital pins		1.71*3	2.8	3.6	
Digital core power supply 0 to 2	USB is disabled.	DVDK0-2	1.08	1.20	1.32	V
	USB is established.		1.35	1.40	1.50	
Digital High input voltage	Normal input*1	DV_{IH}	0.7 × DVDIO0-2	—	—	V
	Schmitt trigger input*1		0.8 × DVDIO0-2	—	—	
Digital Low input voltage	Normal input*1	DV_{IL}	—	—	0.3 × DVDIO0-2	V
	Schmitt trigger input*1		—	—	0.2 × DVDIO0-2	
Digital ground		DVS		0		V
Audio LPF power supply		AVDLPF	1.9	2.0	2.2	V
Audio LPF ground		AVSLPF		0		V
SAR A/D converter power supply*2		AVDADC	1.08	1.2	1.50	V
SAR A/D converter ground		AVSADC		0		V
Main oscillator power supply*2		AVDOSC1	1.08	1.2	1.50	V
Sub oscillator power supply*2		AVDOSC2	1.08	1.2	1.50	V
Oscillator ground		AVSOSC		0		V
PLL power supply*2		AVDPLL	1.08	1.2	1.50	V
PLL ground		AVSPLL		0		V
USB PHY power supply		AVDUSB	2.97	3.3	3.63	V
USB PHY ground		AVSUSB		0		V
Operating temperature		T_C	–20	+25	+75	˚C

*1 Refer to I/O Type column in Table 4 State of Pins.

*2 Offset for DVDK0-2 shall be less than 0.3V.

*3 When SCL/GPIOK0 and SDA/GPIOK1 are in use, the minimum voltage must be as low as 1.8V.

3. Electrical Characteristics Under Recommended Operating Temperature Range

Table 7. Electrical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Digital High input current	DI_{IH}	Neither pull-up nor pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	µA
		Pull-up enabled*1, DVDIOx = 3.63V	–5	—	5	
		Pull-down enabled*1, DVDIOx = 3.63V	18	—	80	
Digital Low input current	DI_{IL}	Neither pull-up nor pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	µA
		Pull-up enabled*1, DVDIOx = 3.63V	–80	—	–18	
		Pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	
Digital High output current 1*2	DI_{OH1}	DV_{OL} = 0.4V, DVDIOx = 1.8V	–0.9	—	—	mA
Digital Low output current 1*2	DI_{OL1}	DV_{OH} = 1.35V, DVDIOx = 1.8V	1.0	—	—	mA
Digital High output current 2*3	DI_{OH2}	DV_{OL} = 0.4V, DVDIOx = 1.8V	–1.9	—	—	mA
Digital Low output current 2*3	DI_{OL2}	DV_{OH} = 1.35V, DVDIOx = 1.8V	2.0	—	—	mA
Digital High input current in high impedance	DI_{ZH}	Neither pull-up nor pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	µA
		Pull-up enabled*1, DVDIOx = 3.63V	–5	—	5	
		Pull-down enabled*1, DVDIOx = 3.63V	18	—	80	
Digital Low input current in high impedance	DI_{ZL}	Neither pull-up nor pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	µA
		Pull-up enabled*1, DVDIOx = 3.63V	–80	—	–18	
		Pull-down enabled*1, DVDIOx = 3.63V	–5	—	5	
Digital I/O pull-up resistance	DR_{PU}		45	75	205	kΩ
Digital I/O pull-down resistance	DR_{PD}		45	75	205	kΩ
3.3V USB current	I_{USB}	HS OUT transfer, T_C = 25°C, DVDKx = 1.50V	—	35	—	mA
		Suspend mode, T_C = 25°C, DVDKx = 1.50V	—	55	—	µA
LPF current	I_{LPF}	AVDLPF = 2.2V	—	880	1500	µA
		Power down mode	—	—	100	
Oscillator, PLL current	I_{OSC}	AVDOSC1 = AVDOSC2 = AVDPLL = 1.32V Both OSC45 and OSC12 are in ceramic mode*4, PLL is running at 40MHz*6	—	—	3.0	mA
		AVDOSC1 = AVDOSC2 = AVDPLL = 1.32V Both OSC45 and OSC12 are in crystal mode*5, PLL is running at 40MHz*6	—	—	2.5	mA
		AVDOSC1 = AVDOSC2 = AVDPLL = 1.32V OSC45, OSC12 and PLL are in power down mode*7	—	—	90	µA
ADC current	I_{ADC}	AVDADC = 1.32V, active*8	—	—	1.25	mA
		AVDADC = 1.32V, power down mode*9	—	—	80	µA

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
DVDK current	Full speed	I_{CORE}	DVDKx = 1.20V, CPU is running at 45.1584MHz, T_C = 25℃	—	12	13	mA
			DVDKx = 1.20V, DMAC is running at 45.1584MHz, T_C = 25℃	—	16	—	mA
	VME mode		DVDKx = 1.20V, VME is running at 45.1584MHz, T_C = 25℃	—	40	—	mA
	Idle mode		DVDKx = 1.20V, audio effect H/W is running at 45.1584MHz, T_C = 25℃	—	10	—	mA
DVDK current on power down	Stop mode	I_{PD}	DVDKx = 1.2V, T_C = 25℃	—	250	400	μA
			DVDKx = 1.5V, T_C = 25℃	—	800	1100	μA

*1 Refer to GPIO setting in user's manual.

*2 Refer to Output Drivability column in Table 4 State of Pins.

*3 Refer to Output Drivability column in Table 4 State of Pins.

*4 Ceramic mode: For OSC45, keep MCSEL pin "H". For OSC12, set SCSEL bit to "1" in SCLE register (30000010h). Set SOSC bit to "0" in CLC register (30000000h).

*5 Crystal mode: For OSC45, keep MCSEL pin "L". For OSC12, set SCSEL bit to "0" in SCLE register (30000010h). Set SOSC bit to "0" in CLC register (30000000h).

*6 Set SPLLEN bit to "1", set SFDEV1 bit to "0", and set SFDEV0 bit to "1" in SCLE register (30000010h).

*7 Set SOSC bit to "1" in CLC register (30000000h) and set SPLLEN bit to "0" in SCLE register (30000010h), then set to stop mode.

*8 Set ADEN bit to "1" in ADCC register (30002004h).

*9 Set ADEN bit to "0" in ADCC register (30002004h).

Analog Block

1. OSC45

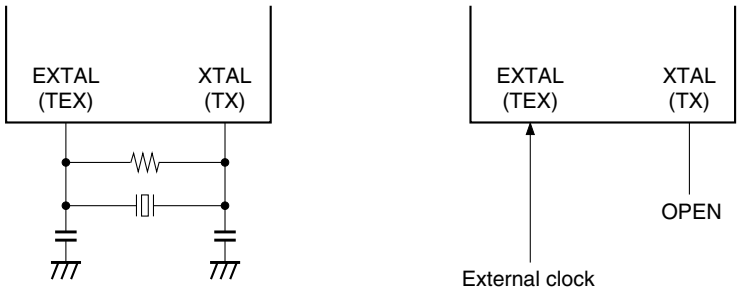
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Equivalent series resistance	ESR		—	30	—	Ω
Input frequency	FP		40	45	60	MHz
Frequency fluctuation	FOUT	Crystal mode	–30	—	30	ppm
		Ceramic mode	–500	—	500	ppm
Period jitter	TCYC	Crystal mode	80	100	120	ps
Supply current in suspend mode	ICCS		—	2	—	μA
Operating supply current	IOS	Crystal mode	—	500	—	μA
		Ceramic mode	—	700	—	μA
Lock-in time	TL		—	—	5	ms

2. OSC12

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Equivalent series resistance	ESR		—	30	—	Ω
Input frequency	FP		10	12	20	MHz
Frequency fluctuation	FOUT	Crystal mode	–30	—	30	ppm
		Ceramic mode	–500	—	500	ppm
Period jitter	TCYC		80	100	120	ps
Supply current in suspend mode	ICCS		—	2	—	μA
Operating supply current	IOS	Crystal mode	—	200	—	μA
		Ceramic mode	—	300	—	μA
Lock-in time	TL		—	—	5	ms

3. Crystal/Ceramic and Oscillator Connection

Exact matching parameters for feedback resistance and capacitance depend on the system.



(a) Crystal/Ceramic **(b) External clock**

Fig. 3. Crystal/Ceramic Connection

4. PLL

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input frequency	F_{IN}		—	12	—	MHz
Output frequency	F_{OUT}		40/32/20/16 (switchable)			MHz
Output duty cycle	D		47	50	53	%
Period jitter	T_P	Peak to peak	–80	—	80	ps
		RMS	—	—	20	ps
Cycle-to-cycle jitter	T_C	Peak to peak	–150	—	150	ps
		RMS	—	—	40	ps
Lock-in time	T_L		—	—	10	μs

5. LPF

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dynamic range		A-weight = ON, Vp-p 1.6V	—	93	—	dB
Signal to noise ratio	SNR	10 to 20kHz, Vp-p 1.6V, AVDLPF = 2.0V, 0dB, A-weight = OFF	—	90	—	dB
		10 to 20kHz, Vp-p 1.6V, AVDLPF = 2.0V, 0dB, A-weight = ON	—	93	—	dB
Total harmonic distortion	THD+N	10 to 20kHz at 100kΩ load	—	0.01	0.03	%
Interchannel isolation		L → R, R → L	—	90	—	dB
Gain		1kHz	—	–1.9	—	dB
		20kHz	—	–1.9	—	
		1kHz, A-weight = ON	—	–36.8	—	
Cutoff frequency	f_{CUT}		—	90	—	kHz
Power supply rejection ratio	PSRR	AVDLPF pin voltage deviation: 100Hz, –10dBV External capacitor at VREFL and VREFR pins: 10μF Signal input: DC	—	–60	—	dB
Charge time of capacitor at reference voltage	t_{VREF}	C_{VREF} = 1μF	—	24	—	ms
Output resistance load	R_{OUT}		15	—	100	kΩ

6. SAR-ADC

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input frequency	F_{IN}		—	—	11	MHz
Conversion cycle time	T_{CYC}		11			cyc
Accuracy	N_{ACC}	–10 to +75°C	7	—	—	bit
Differential nonlinearity	D_{NL}		—	—	3	LSB
Integral nonlinearity	I_{NL}		—	—	8	LSB

7. USB PHY

7-1. FS Specific

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Bus pull-up resistance on D+	R_{PU}		0.9	—	1.575	kΩ
FS differential input sensitivity	V_{DI}		0.2	—	—	V
FS differential common mode range	V_{CM}		0.8	—	2.5	V
FS source Low output signal level	V_{FSOL}		0.0	—	0.3	V
FS source High output signal level	V_{FSOH}		2.8	—	3.6	V
FS output signal crossover voltage	V_{CRS}		1.3	—	2.0	V
FS driver rise time	T_{FSR}	10% to 90%	4	—	20	ns
FS driver fall time	T_{FSF}	10% to 90%	4	—	20	ns
FS source jitter	T_{DJ1}	Next transition	–3.5	—	3.5	ns
FS source jitter	T_{DJ2}	Paired transitions	–4	—	4	ns
FS source SE0 interval of EOP	T_{FEOPT}		160	—	175	ns
FS width of SE0 during transition	T_{FST}		—	—	14	ns

7-2. HS Specific

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
HS squelch detection threshold (differential signal amplitude)	V_{HSSQ}		100	—	150	mV
HS data signaling common mode voltage range	V_{HSCM}		–50	—	500	mV
HS idle signal level	V_{HSOI}		–10	—	10	mV
HS data signaling High	V_{HSOH}		360	—	500	mV
HS data signaling Low	V_{HSOL}		–10	—	10	mV
Chirp J level	V_{CHIRPJ}	Differential voltage	700	—	1100	mV
Chirp K level	V_{CHIRPK}	Differential voltage	–900	—	–500	mV
HS driver rise time	T_{HSR}	10% to 90%	500	—	—	ps
HS driver fall time	T_{HSF}	10% to 90%	500	—	—	ps

Recommended Power-on/Power-off Sequence

DVDK0-2 and analog power supply should be powered on prior to DVDIO0-2 power supply. The system must wait until its stabilization by asserting $\overline{RST}$ for over 1ms. There is not any requirement for supply order between DVDK0-2 and analog power supply. The power-off sequence does not care the state of $\overline{RST}$.

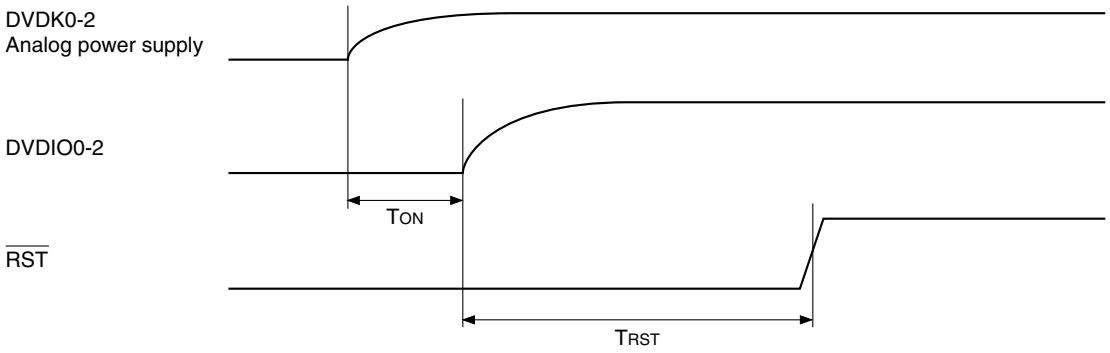


Fig. 4. Power-on Sequence

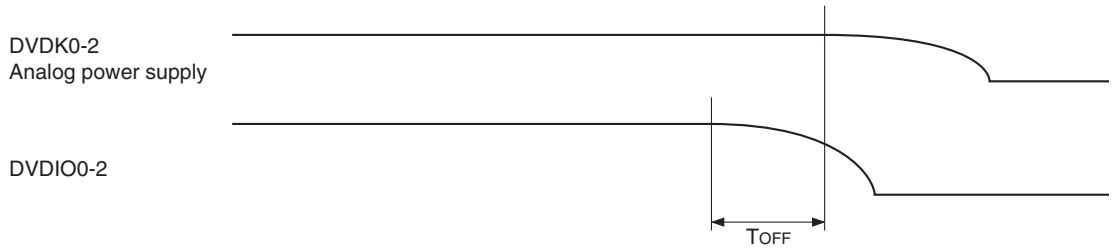


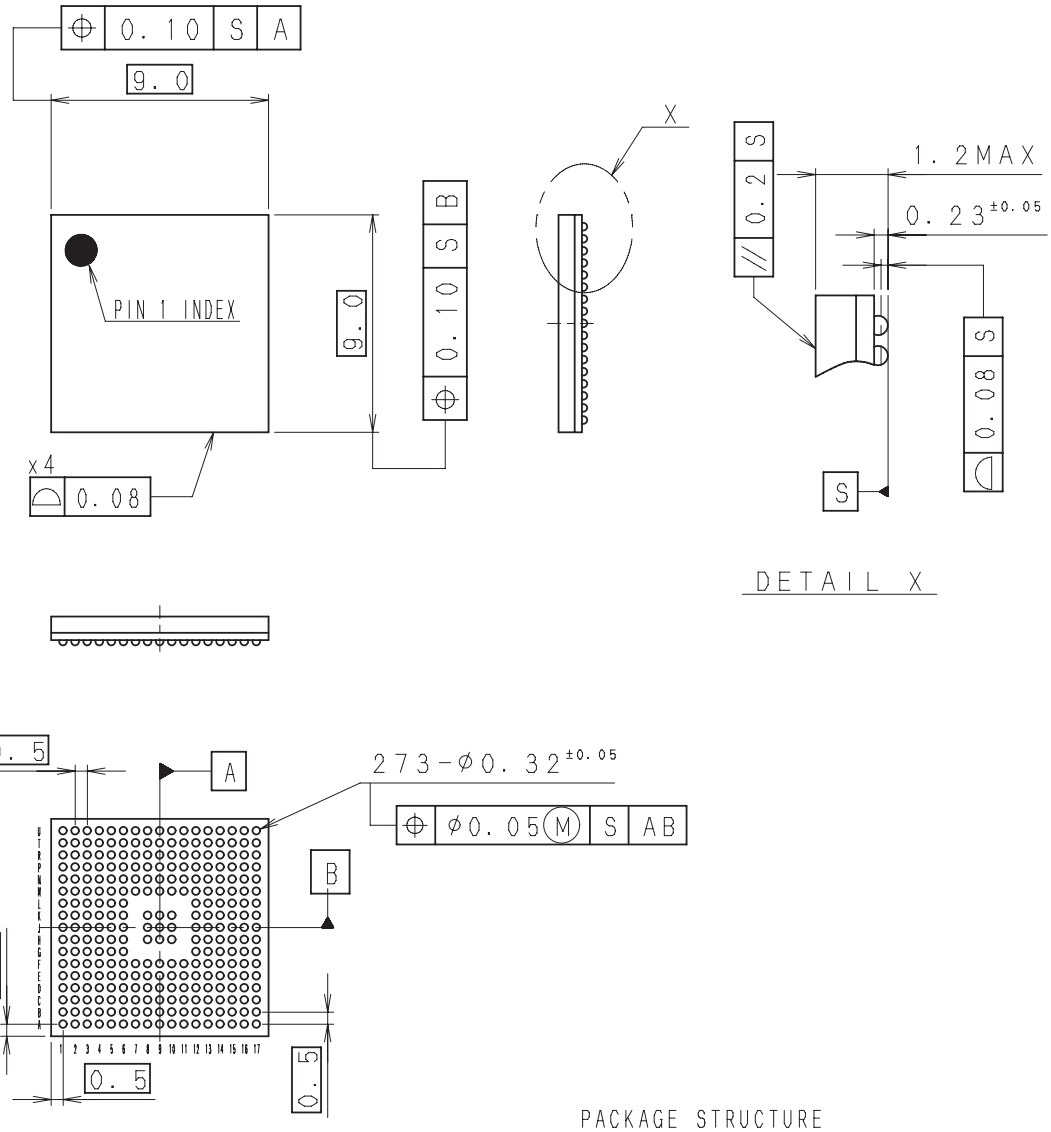
Fig. 5. Power-off Sequence

Item	Symbol	Min.	Typ.	Unit
DVDIO0-2 power-on wait for DVDK0-2 and analog power supply	TON	5	10	ms
$\overline{RST}$ power-on wait for DVDIO0-2	TRST	1	10	ms
DVDK0-2 and analog power supply power-off wait for DVDIO0-2	TOFF	1	2	ms

Package Outline

(Unit: mm)

273PIN TFBGA



SONY CODE	TFBGA-273P-02
JEITA CODE	P-TFBGA273-9X9-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	0.2g

AP-4000-273002S Rev. 0