

ASSP For Power Management Applications (DC/DC Converter for DSC/Camcorder)

4-ch DC/DC Converter IC

MB39A102

■ DESCRIPTION

The MB39A102 is a 4-channel DC/DC converter IC using pulse width modulation (PWM). This IC is ideal for up conversion, down conversion, and up/down conversion.

4ch is built in TSSOP-30P/BCC-32P package. Each channel can be controlled, and soft-start.

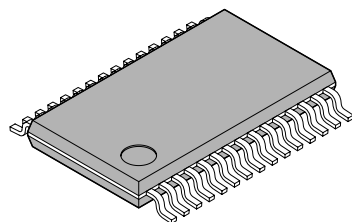
This is an ideal power supply for high-performance portable devices such as digital still cameras.

■ FEATURES

- Supports for down-conversion and up/down Zeta conversion (CH1 to CH3)
- Supports for up-conversion and up/down Sepic conversion (CH4)
- Power supply voltage range : 2.5 V to 11 V
- Reference voltage : 2.0 V \pm 1 %
- Error amplifier threshold voltage : 1.24 V \pm 1.5 %
- Built-in totem-pole type output for MOS FET
- Built-in soft-start circuit without load dependence
- High-frequency operation capability : 1.5 MHz (Max)
- External short-circuit detection capability by -INS terminal

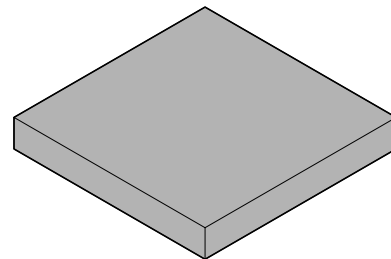
■ PACKAGES

30-pin plastic TSSOP



(FPT-30P-M04)

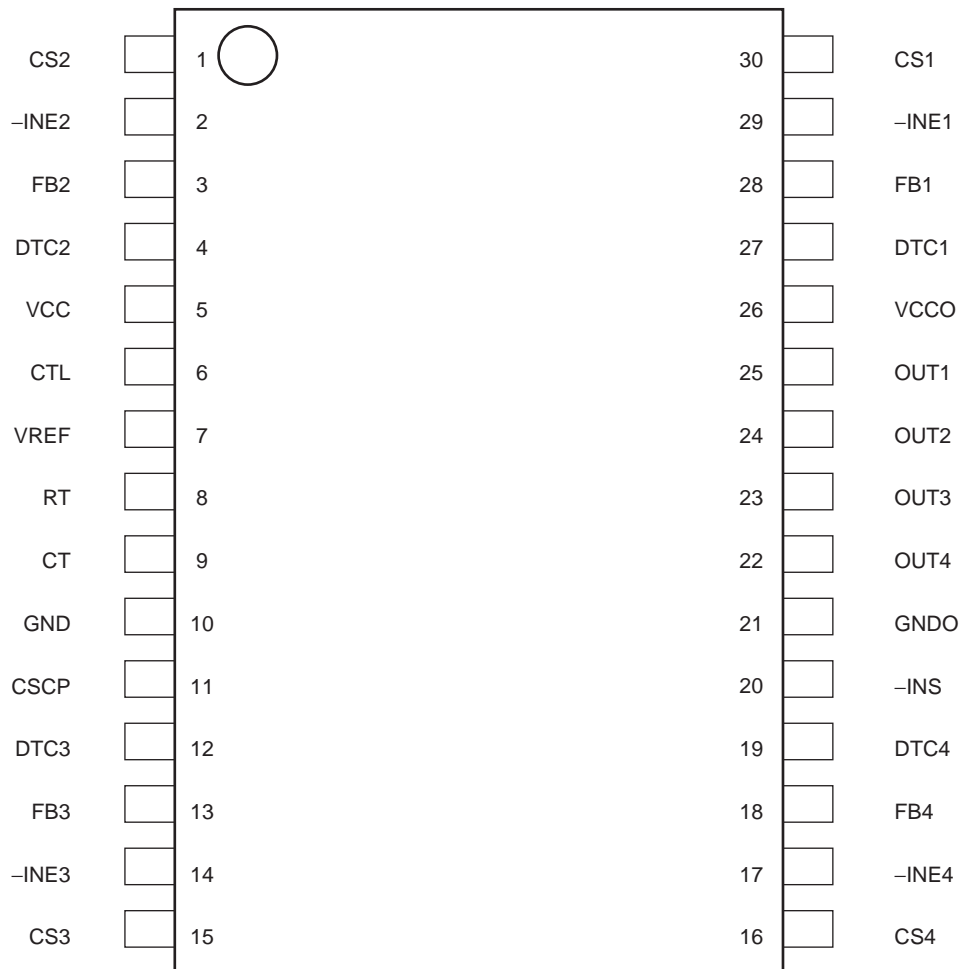
32-pad plastic BCC



(LCC-32P-M15)

■ PIN ASSIGNMENTS

(TOP VIEW)

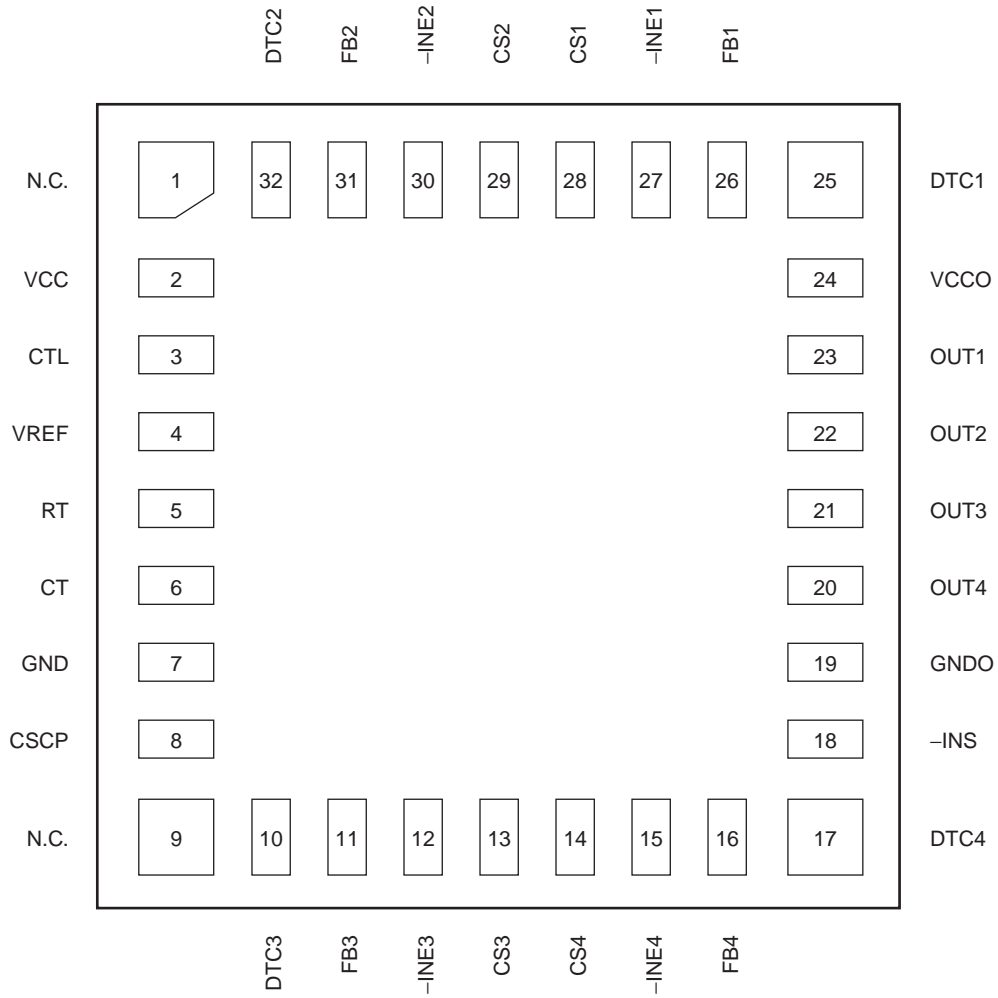


(FPT-30P-M04)

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(TOP VIEW)
(Penetration diagram from surface)



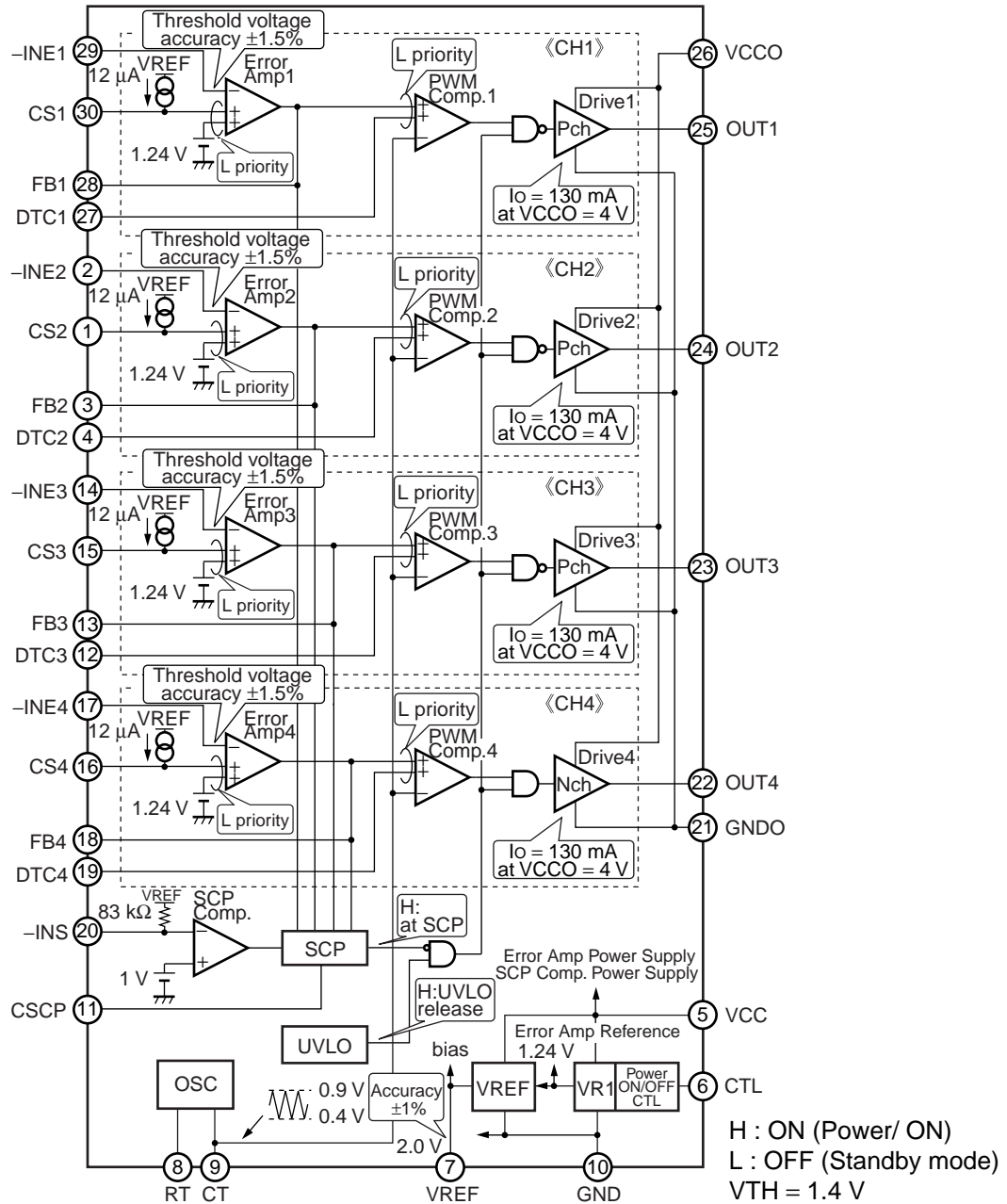
(LCC-32P-M15)

MB39A102

■ PIN DESCRIPTION

| Block | Pin No. | | Symbol | I/O | Descriptions |
|---------|---------|-----|--------|-----|---|
| | TSSOP | BCC | | | |
| CH1 | 27 | 25 | DTC1 | I | Dead time control terminal |
| | 28 | 26 | FB1 | O | Error amplifier output terminal |
| | 29 | 27 | -INE1 | I | Error amplifier inverted input terminal |
| | 30 | 28 | CS1 | — | Soft-start capacitor connection terminal |
| | 25 | 23 | OUT1 | O | Output terminal |
| CH2 | 4 | 32 | DTC2 | I | Dead time control terminal |
| | 3 | 31 | FB2 | O | Error amplifier output terminal |
| | 2 | 30 | -INE2 | I | Error amplifier inverted input terminal |
| | 1 | 29 | CS2 | — | Soft-start capacitor connection terminal |
| | 24 | 22 | OUT2 | O | Output terminal |
| CH3 | 12 | 10 | DTC3 | I | Dead time control terminal |
| | 13 | 11 | FB3 | O | Error amplifier output terminal |
| | 14 | 12 | -INE3 | I | Error amplifier inverted input terminal |
| | 15 | 13 | CS3 | — | Soft-start capacitor connection terminal |
| | 23 | 21 | OUT3 | O | Output terminal |
| CH4 | 19 | 17 | DTC4 | I | Dead time control terminal |
| | 18 | 16 | FB4 | O | Error amplifier output terminal |
| | 17 | 15 | -INE4 | I | Error amplifier inverted input terminal |
| | 16 | 14 | CS4 | — | Soft-start capacitor connection terminal |
| | 22 | 20 | OUT4 | O | Output terminal |
| OSC | 9 | 6 | CT | — | Triangular wave frequency setting capacitor connection terminal |
| | 8 | 5 | RT | — | Triangular wave frequency setting resistor connection terminal |
| Control | 6 | 3 | CTL | I | Power supply and control terminal |
| | 11 | 8 | CSCP | — | Short-circuit detection circuit capacitor connection terminal |
| | 20 | 18 | -INS | I | Short-circuit detection comparator inverted input terminal |
| Power | 26 | 24 | VCCO | — | Output block power supply terminal |
| | 5 | 2 | VCC | — | Power supply terminal |
| | 7 | 4 | VREF | O | Reference voltage output terminal |
| | 21 | 19 | GNDO | — | Output block ground terminal |
| | 10 | 7 | GND | — | Ground terminal |

■ BLOCK DIAGRAM



MB39A102

■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Condition | Rating | | Unit |
|----------------------|------------------|---|--------|-------|------|
| | | | Min | Max | |
| Power supply voltage | V _{CC} | VCC, VCCO terminals | — | 12 | V |
| Output current | I _o | OUT1 to OUT4 terminals | — | 20 | mA |
| Output peak current | I _{oP} | OUT1 to OUT4 terminals Duty ≤ 5% (t = 1/f _{osc} × Duty) | — | 400 | mA |
| Power dissipation | P _D | T _a ≤ +25 °C (TSSOP-30P) | — | 1390* | mW |
| | | T _a ≤ +25 °C (BCC-32P) | — | 980* | mW |
| Storage temperature | T _{STG} | — | -55 | +125 | °C |

* : The packages are mounted on the epoxy board (10 cm × 10 cm).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Condition | Value | | | Unit |
|------------------------------------|------------------|--------------------------|-------|-----|-----------------------|------|
| | | | Min | Typ | Max | |
| Power supply voltage | V _{CC} | VCC, VCCO terminals | 2.5 | 4 | 11 | V |
| Reference voltage output current | I _{REF} | VREF terminal | -1 | — | 0 | mA |
| Input voltage | V _{INE} | -INE1 to -INE4 terminals | 0 | — | V _{CC} - 0.9 | V |
| | | -INS terminal | 0 | — | V _{REF} | V |
| | V _{DTC} | DTC1 to DTC4 terminals | 0 | — | V _{REF} | V |
| Control input voltage | V _{CTL} | CTL terminal | 0 | — | 11 | V |
| Output current | I _o | OUT1 to OUT4 terminals | -15 | — | +15 | mA |
| Oscillation frequency | f _{osc} | * | 100 | 500 | 1500 | kHz |
| Timing capacitor | C _T | — | 39 | 100 | 560 | pF |
| Timing resistor | R _T | — | 11 | 24 | 130 | kΩ |
| Soft-start capacitor | C _S | CS1 to CS4 terminals | — | 0.1 | 1.0 | μF |
| Short detection capacitor | C _{SCP} | — | — | 0.1 | 1.0 | μF |
| Reference voltage output capacitor | C _{REF} | — | — | 0.1 | 1.0 | μF |
| Operating ambient temperature | T _a | — | -30 | +25 | +85 | °C |

* : See “■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY”.

Note : Pin numbers referred after this part are present on TSSOP-30P PKG.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = VCCO = 4 V, Ta = +25 °C)

| Parameter | Symbol | Pin No | Conditions | Value | | | Unit | |
|---|--------------------------------------|--------------------------|---------------------|-------------------------------|-------|-------|-------|-----|
| | | | | Min | Typ | Max | | |
| Reference voltage block [Ref] | Output voltage | V _{REF} | 7 | — | 1.98 | 2.00 | 2.02 | V |
| | Output voltage temperature variation | $\Delta V_{REF}/V_{REF}$ | 7 | Ta = -30 °C to +85 °C | — | 0.5* | — | % |
| | Input stability | Line | 7 | VCC = 2.5 V to 11 V | -10 | — | +10 | mV |
| | Load stability | Load | 7 | VREF = 0 mA to -1 mA | -10 | — | +10 | mV |
| Under voltage lockout protection circuit block [UVLO] | Threshold voltage | V _{TH} | 25 | VCC = $\underline{\text{L}}$ | 1.7 | 1.8 | 1.95 | V |
| | Hysteresis width | V _H | 25 | — | 0.05 | 0.1 | 0.2 | V |
| Short comparator detection block [SCP] | Threshold voltage | V _{TH} | 11 | — | 0.65 | 0.70 | 0.75 | V |
| | Input source current | I _{CSCP} | 11 | — | -1.4 | -1.0 | -0.6 | μA |
| | Reset voltage | V _{RST} | 25 | VREF = $\underline{\text{L}}$ | 1.5 | 1.7 | 1.9 | V |
| Triangular wave oscillator block [OSC] | Oscillation frequency | f _{osc} | 22, 23, 24, 25 | CT = 100 pF, RT = 24 kΩ | 450 | 500 | 550 | kHz |
| | Frequency temperature variation | $\Delta f_{osc}/f_{osc}$ | 22, 23, 24, 25 | Ta = -30 °C to +85 °C | — | 1* | — | % |
| Soft-start block [CS] | Charge current | I _{CS} | 1, 15, 16, 30 | CS1 to CS4 = 0 V | -16 | -12 | -8 | μA |
| Error amplifier block [Error Amp1 to Error Amp4] | Threshold voltage | V _{TH} | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | 1.222 | 1.240 | 1.258 | V |
| | Input bias current | I _B | 2, 14, 17, 29 | -INE1 to -INE4 = 0 V | -120 | -30 | — | nA |
| | Voltage gain | A _v | 3, 13, 18, 28 | DC | — | 100* | — | dB |
| | Frequency bandwidth | BW | 3, 13, 18, 28 | A _v = 0 dB | — | 1.6* | — | MHz |
| | Output voltage | V _{OH} | 3, 13, 18, 28 | — | 1.7 | 1.9 | — | V |
| | | V _{OL} | 3, 13, 18, 28 | — | — | 40 | 200 | mV |
| | Output source current | I _{SOURCE} | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | — | -2 | -1 | mA |
| Output sink current | I _{SINK} | 3, 13, 18, 28 | FB1 to FB4 = 0.65 V | 150 | 200 | — | μA | |

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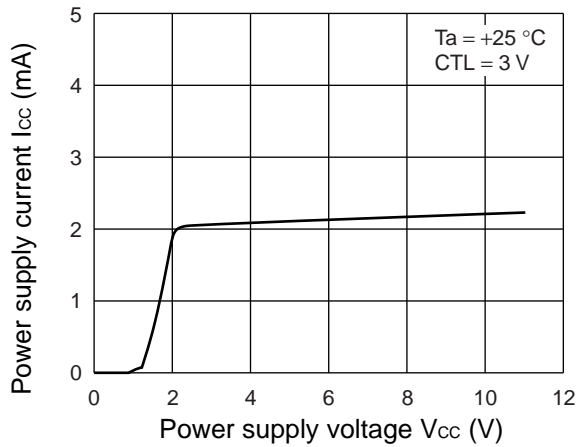
(VCC = VCCO = 4 V, Ta = +25 °C)

| Parameter | | Symbol | Pin No. | Conditions | Value | | | Unit |
|--|-----------------------|---------------------|----------------|---|-------|------|------|------|
| | | | | | Min | Typ | Max | |
| PWM comparator block [PWM Comp.1 to PWM Comp.4] | Threshold voltage | V _{T0} | 22, 23, 24, 25 | Duty cycle = 0 % | 0.3 | 0.4 | — | V |
| | | V _{T100} | 22, 23, 24, 25 | Duty cycle = 100 % | — | 0.9 | 1.0 | V |
| | Input current | I _{DTC} | 4, 12, 19, 27 | DTC1 to DTC4 = 0.4 V | -2.0 | -0.6 | — | μA |
| Output block [Drive1 to Drive4] | Output source current | I _{SOURCE} | 22, 23, 24, 25 | Duty ≤ 5 % (t = 1/f _{osc} × Duty) OUT1 to OUT4 = 0 V | — | -130 | -75 | mA |
| | Output sink current | I _{SINK} | 22, 23, 24, 25 | Duty ≤ 5 % (t = 1/f _{osc} × Duty) OUT1 to OUT4 = 4 V | 75 | 120 | — | mA |
| | Output ON resistance | R _{OH} | 22, 23, 24, 25 | OUT1 to OUT4 = -15 mA | — | 18 | 27 | Ω |
| | | R _{OL} | 22, 23, 24, 25 | OUT1 to OUT4 = 15 mA | — | 18 | 27 | Ω |
| Short detection comparator block [SCP Comp.] | Threshold voltage | V _{TH} | 25 | — | 0.97 | 1.00 | 1.03 | V |
| | Input bias current | I _B | 20 | -INS = 0 V | -29 | -24 | -21 | μA |
| Control block [CTL] | CTL input voltage | V _{IH} | 6 | IC Active mode | 1.7 | — | 11 | V |
| | | V _{IL} | 6 | IC Standby mode | 0 | — | 0.8 | V |
| | Input current | I _{CTLH} | 6 | CTL = 3 V | 5 | 30 | 60 | μA |
| | | I _{CTLL} | 6 | CTL = 0 V | — | — | 1 | μA |
| General | Standby current | I _{CCS} | 5 | CTL = 0 V | — | 0 | 2 | μA |
| | | I _{CCSO} | 26 | CTL = 0 V | — | 0 | 2 | μA |
| | Power supply current | I _{CC} | 5 | CTL = 3 V | — | 2.1 | 4.5 | mA |

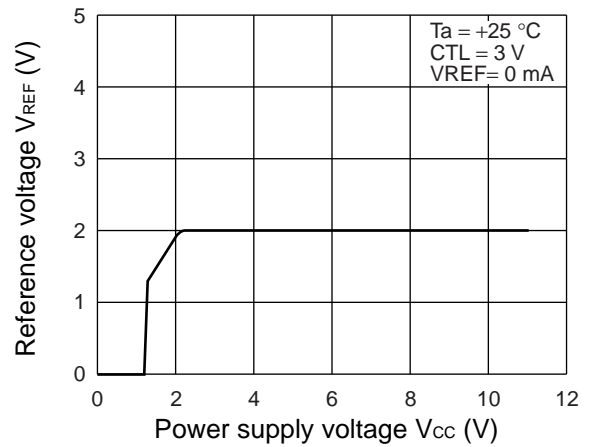
*: Standard design value.

TYPICAL CHARACTERISTICS

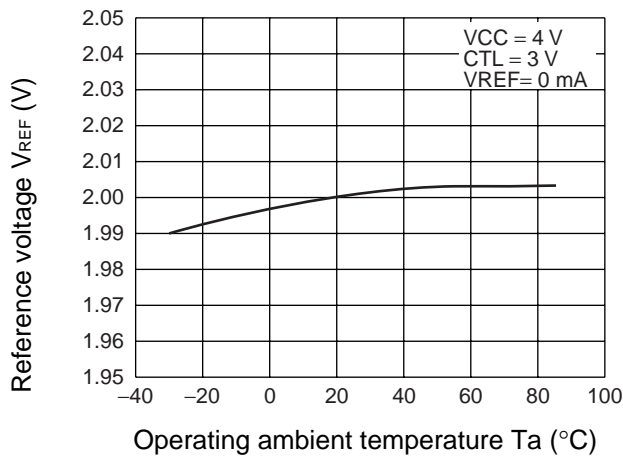
Power Supply Current vs. Power Supply Voltage



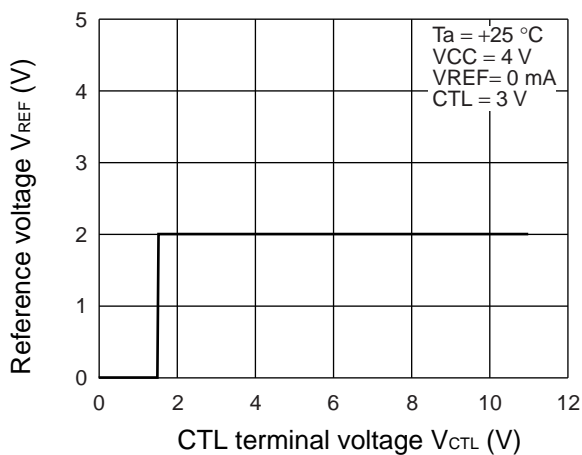
Reference Voltage vs. Power Supply Voltage



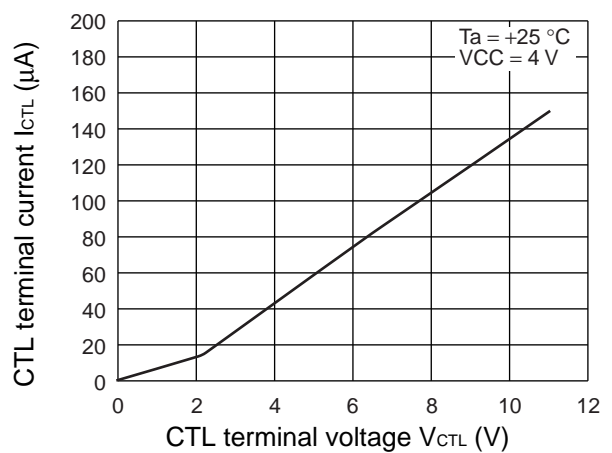
Reference Voltage vs. Operating Ambient Temperature



Reference Voltage vs. CTL terminal Voltage

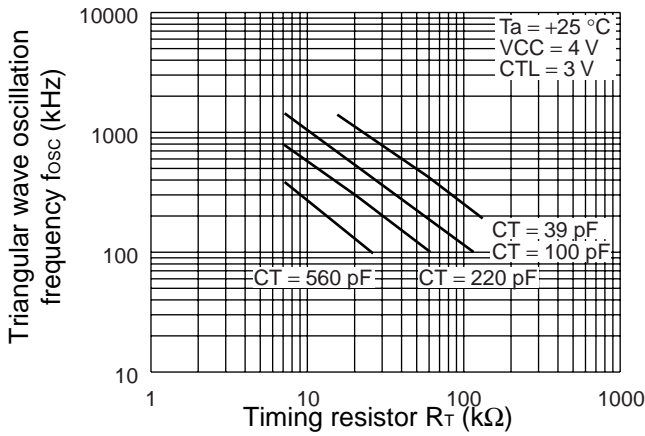


CTL terminal Current vs. CTL terminal Voltage

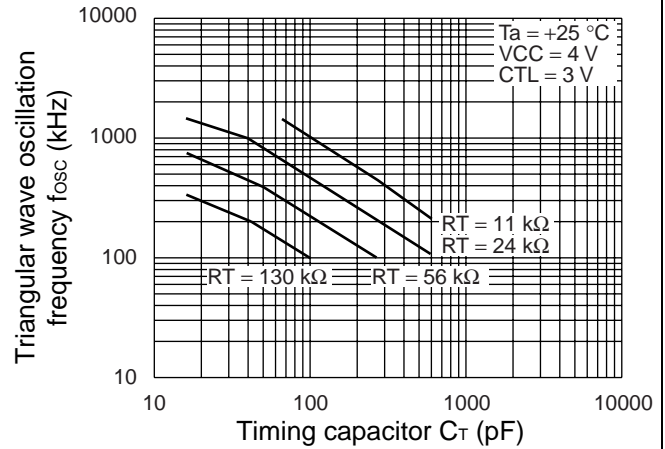


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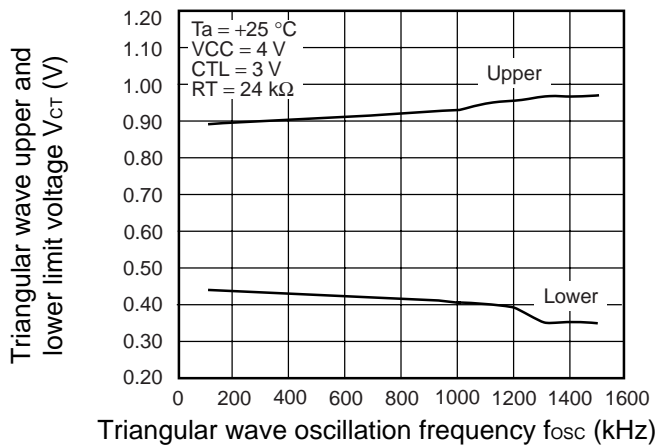
Triangular Wave Oscillation Frequency vs. Timing Resistor



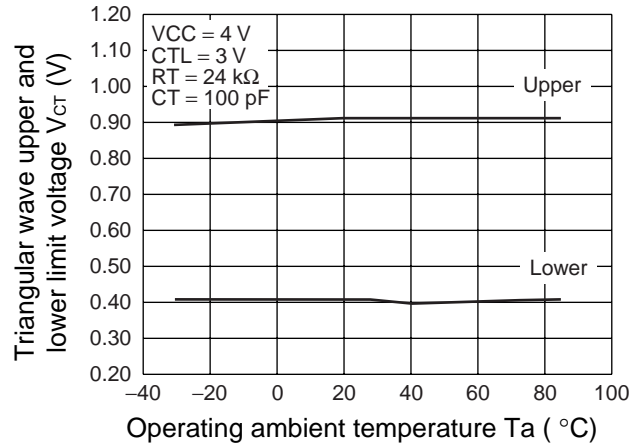
Triangular Wave Oscillation Frequency vs. Timing Capacitor



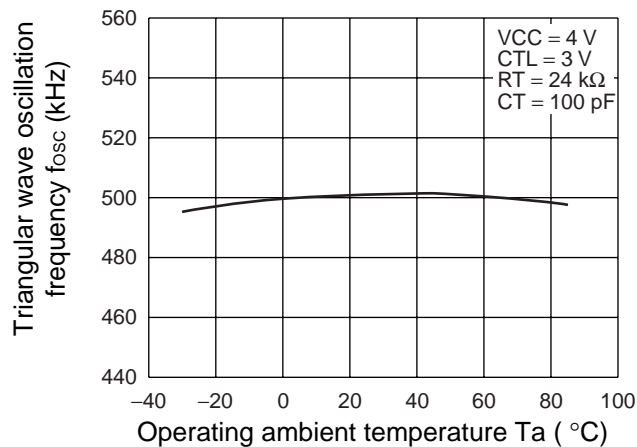
Triangular Wave Upper and Lower Limit Voltage vs. Triangular Wave Oscillation Frequency



Triangular Wave Upper and Lower Limit Voltage vs. Operating Ambient Temperature



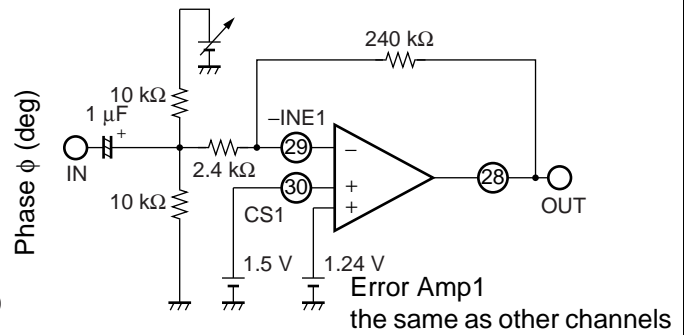
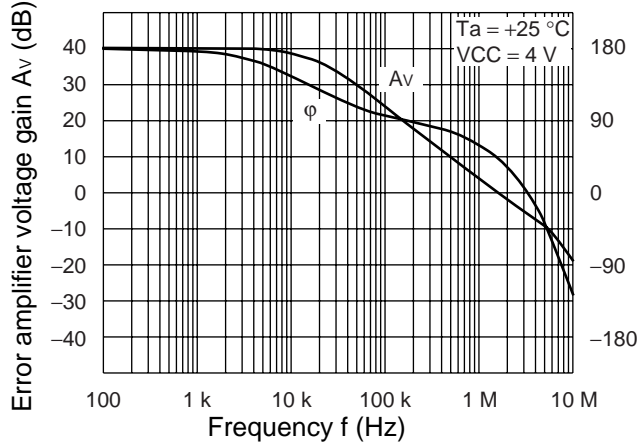
Triangular Wave Oscillation Frequency vs. Operating ambient Temperature



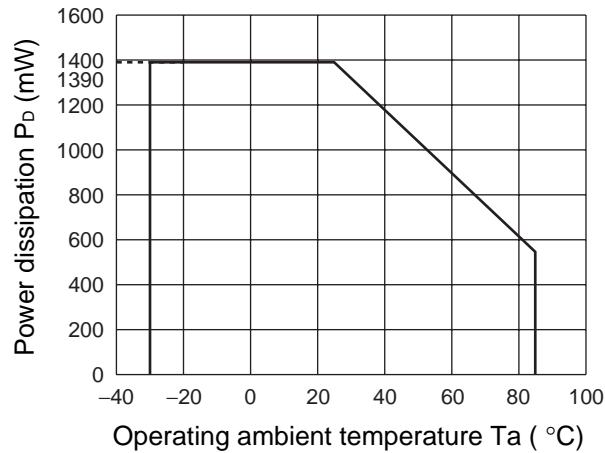
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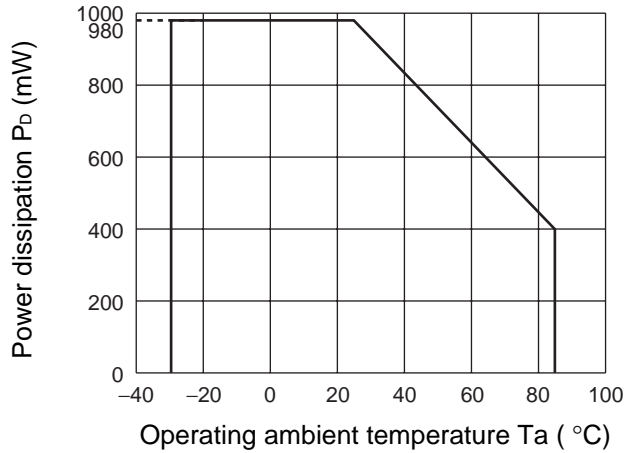
Error Amplifier Voltage Gain, Phase vs. Frequency



Power Dissipation vs. Operating Ambient Temperature (TSSOP-30P)



Power Dissipation vs. Operating Ambient Temperature (BCC-32P)



■ FUNCTIONS

1. DC/DC Converter Functions

(1) Reference voltage block (Ref)

The reference voltage circuit generates a temperature-compensated reference voltage (2.0 V Typ) from the voltage supplied from the VCC terminal (pin 5). The voltage is used as the reference voltage for the IC's internal circuitry.

The reference voltage can supply a load current of up to 1 mA to an external device through the VREF terminal (pin 7).

(2) Triangular-wave oscillator block (OSC)

The triangular wave oscillator incorporates a timing capacitor and a timing resistor connected respectively to the CT terminal (pin 9) and RT terminal (pin 8) to generate triangular oscillation waveform amplitude of 0.4 V to 0.9 V.

The triangular waveforms are input to the PWM comparator in the IC.

(3) Error amplifier block (Error Amp1 to Error Amp4)

The error amplifier detects the DC/DC converter output voltage and outputs PWM control signals. In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the output terminal to inverted input terminal of the error amplifier, enabling stable phase compensation to the system.

Also, it is possible to prevent rush current at power supply start-up by connecting a soft-start capacitor with the CS1 terminal (pin 30) to CS4 terminal (pin 16) while are the non-inverted input terminal for Error Amp. The use of Error Amp for soft-start detection makes it possible for a system to operate on a fixed soft-start time that is independent of the output load on the DC/DC converter.

(4) PWM comparator block (PWM Comp.1 to PWM Comp.4)

The PWM comparator is a voltage-to-pulse width modulator that controls the output duty depending on the input/output voltage.

The output transistor turns on while the error amplifier output voltage and DTC voltage remain higher than the triangular wave voltage.

(5) Output block (Drive1 to Drive4)

The output block is in the totem pole configuration, capable of driving an external P-channel MOS FET (channels 1 to 3), and N-channel MOS FET (channel 4).

2. Channel Control Function

The main or each channel is turned on and off depending on the voltage levels at the CTL terminal (pin 6), CS1 terminal (pin 30), CS2 terminal (pin 1), CS3 terminal (pin 15), and CS4 terminal (pin 16).

Channel On/Off Setting Conditions

| CTL | CS1 | CS2 | CS3 | CS4 | Power | CH1 | CH2 | CH3 | CH4 |
|-----|--------|--------|--------|--------|-------|-----|-----|-----|-----|
| L | —* | —* | —* | —* | OFF | OFF | OFF | OFF | OFF |
| H | GND | GND | GND | GND | ON | OFF | OFF | OFF | OFF |
| H | High-Z | GND | GND | GND | ON | ON | OFF | OFF | OFF |
| H | GND | High-Z | GND | GND | ON | OFF | ON | OFF | OFF |
| H | GND | GND | High-Z | GND | ON | OFF | OFF | ON | OFF |
| H | GND | GND | GND | High-Z | ON | OFF | OFF | OFF | ON |
| H | High-Z | High-Z | High-Z | High-Z | ON | ON | ON | ON | ON |

*: Undefined

3. Protective Functions

(1) Timer-latch short-circuit protection circuit (SCP, SCP Comp.)

The short-circuit detection comparator in each channel detects the output voltage level of Error Amp, and if any channel output voltage of Error Amp reaches the short-circuit detection voltage, the timer circuits are actuated to start charging the external capacitor C_{SCP} connected to the CSCP terminal (pin 11).

When the capacitor (C_{SCP}) voltage reaches about 0.7 V, the circuit is turned off the output transistor and sets the dead time to 100 %.

In addition, the short-circuit detection from external input is capable by using $-INS$ terminal (pin 20) on short-circuit detection comparator (SCP Comp.) .

To release the actuated protection circuit, either the power supply turn off and on again or set the CTL terminal (pin 6) to the "L" level to lower the VREF terminal (pin 7) voltage to 1.5 V (Min) or less. (See "■SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT".)

(2) Under voltage lockout protection circuit (UVLO)

The transient state or a momentary decrease in supply voltage, which occurs when the power supply is turned on, may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, under voltage lockout protection circuit detects a decrease in internal reference voltage with respect to the power supply voltage, turns off the output transistor, and sets the dead time to 100% while holding the CSCP terminal (pin 11) at the "L" level.

The circuit restores the output transistor to normal when the supply voltage reaches the threshold voltage of the under voltage lockout protection circuit.

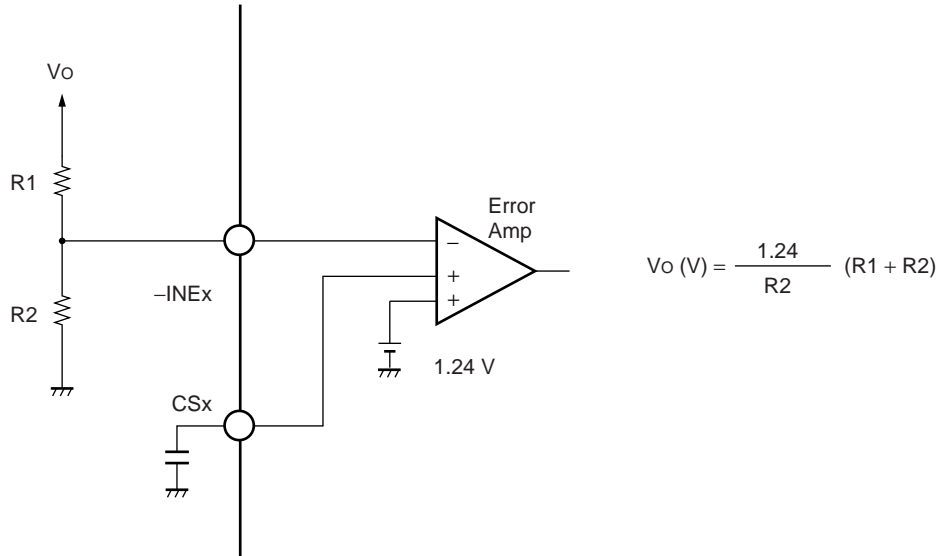
■ PROTECTION CIRCUIT OPERATING FUNCTION TABLE

This table refers to output condition when protection circuit is operating.

| Operating circuit | OUT1 | OUT2 | OUT3 | OUT4 |
|--|------|------|------|------|
| Short-circuit protection circuit | H | H | H | L |
| Under voltage lockout protection circuit | H | H | H | L |

■ SETTING THE OUTPUT VOLTAGE

- CH1 to CH4



$$V_o (V) = \frac{1.24}{R_2} (R_1 + R_2)$$

x : Each channel No.

■ SETTING THE TRIANGULAR OSCILLATION FREQUENCY

The triangular oscillation frequency is determined by the timing capacitor (C_T) connected to the CT terminal (pin 9), and the timing resistor (R_T) connected to the RT terminal (pin 8).

Moreover, it shifts more greatly than the calculated values according to the constant of timing resistor (R_T) when the triangular wave oscillation frequency exceeds 1 MHz. Therefore, set it referring to "Triangular Wave Oscillation Frequency vs. Timing Resistor" and "Triangular Wave Oscillation Frequency vs. Timing Capacitor" in "■ TYPICAL CHARACTERISTICS".

Triangular oscillation frequency : f_{osc}

$$f_{osc} (kHz) \doteq \frac{1200000}{C_T (pF) \times R_T (k\Omega)}$$

■ SETTING THE SOFT-START TIME

To prevent rush currents when the IC is turned on, you can set a soft-start by connecting soft-start capacitors (C_{S1} to C_{S4}) to the CS1 terminal (pin 30) to the CS4 terminal (pin 16), respectively.

Setting each \overline{CTLx} from "H" to "L" switches to charge the external soft-start capacitors (C_{S1} to C_{S4}) connected to the CS1 terminal (pin 30) to CS4 terminal (pin 16) at $12 \mu\text{A}$.

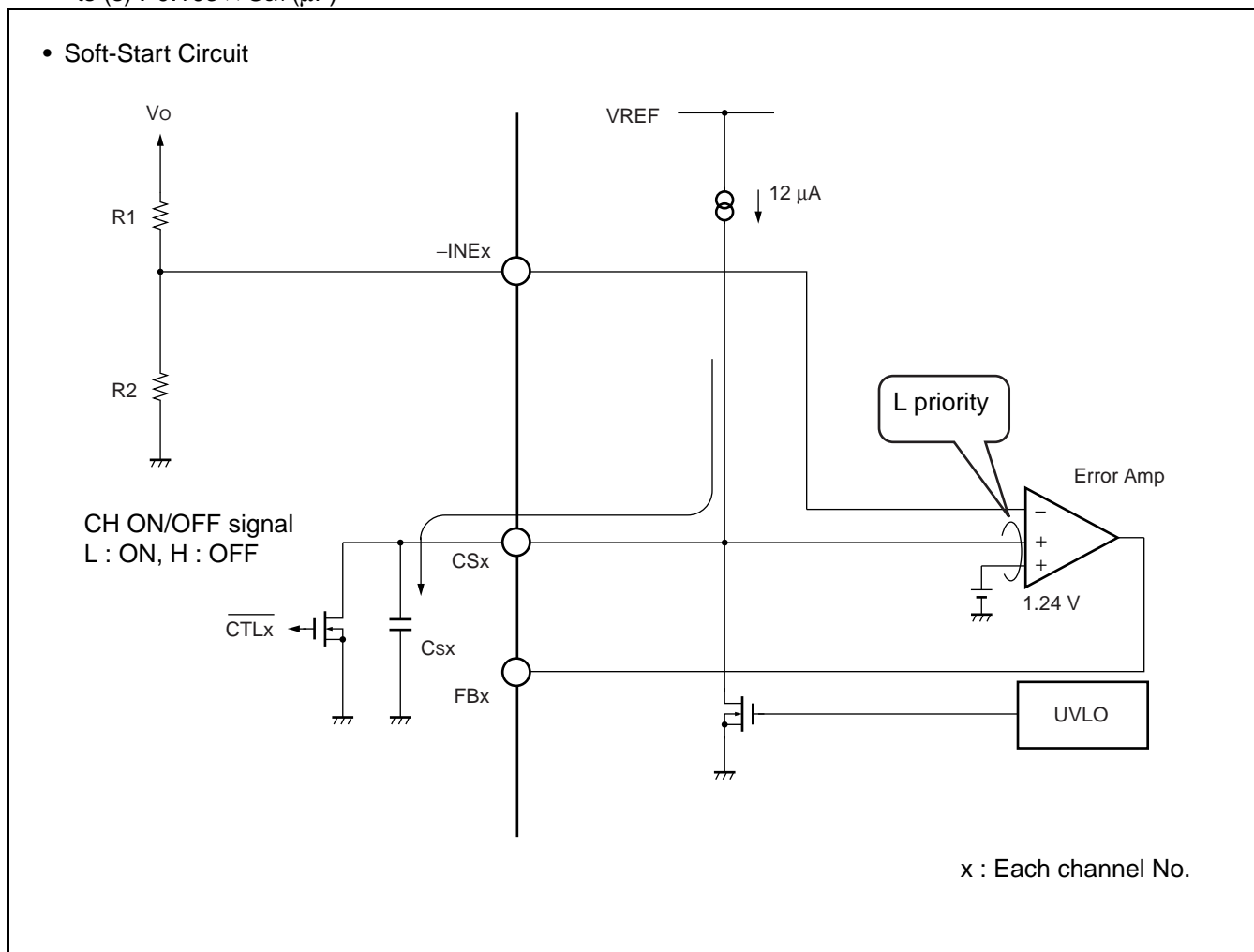
The error amplifier output (FB1 to FB4) is determined by comparison between the lower one of the potentials at two non-inverted input terminals (1.24 V , CS terminal voltages) and the inverted input terminal voltage ($-\text{INE1}$ to $-\text{INE4}$).

The FB terminal voltage during the soft-start period (CS terminal voltage $< 1.24 \text{ V}$) is therefore determined by comparison between the $-\text{INE}$ terminal and CS terminal voltages. The DC/DC converter output voltage rises in proportion to the CS terminal voltage as the soft-start capacitor connected to the CS terminal is charged.

The soft-start time is obtained from the following formula:

Soft-start time: t_s (time to output 100%)

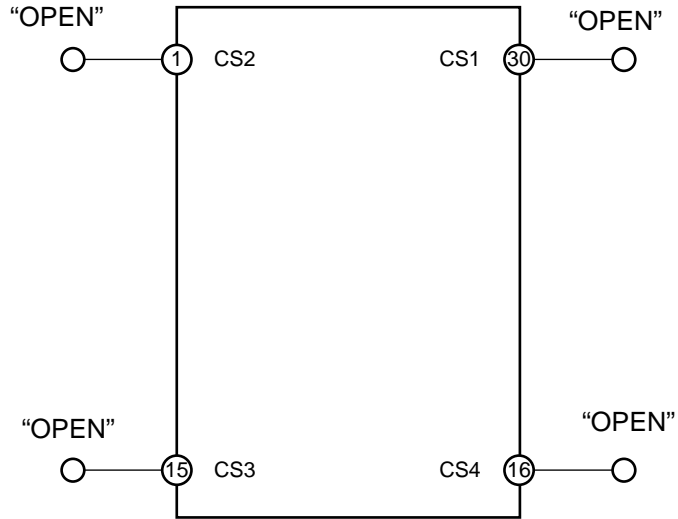
$$t_s (\text{s}) \approx 0.103 \times C_{Sx} (\mu\text{F})$$



■ TREATMENT WITHOUT USING CS TERMINAL

When not using the soft-start function, open the CS1 terminal (pin 30) , the CS2 terminal (pin 1) , the CS3 terminal (pin 15) , the CS4 terminal (pin 16) .

- Without Setting Soft-Start Time



SETTING TIME CONSTANT FOR TIMER-LATCH SHORT-CIRCUIT PROTECTION CIRCUIT

Each channel uses the short-circuit detection comparator (SCP) to always compare the error amplifier's output level to the reference voltage.

While DC/DC converter load conditions are stable on all channels, the short-circuit detection comparator output remains at "L" level, and the CSCP terminal (pin 11) is held at "L" level.

If the load condition on a channel changes rapidly due to a short-circuit of the load, causing the output voltage to drop, the output of the short-circuit detection comparator on that channel goes to "H" level. This causes the external short-circuit protection capacitor C_{SCP} connected to the CSCP terminal (pin 11) to be charged at $1 \mu\text{A}$. Short-circuit detection time (t_{CSCP})

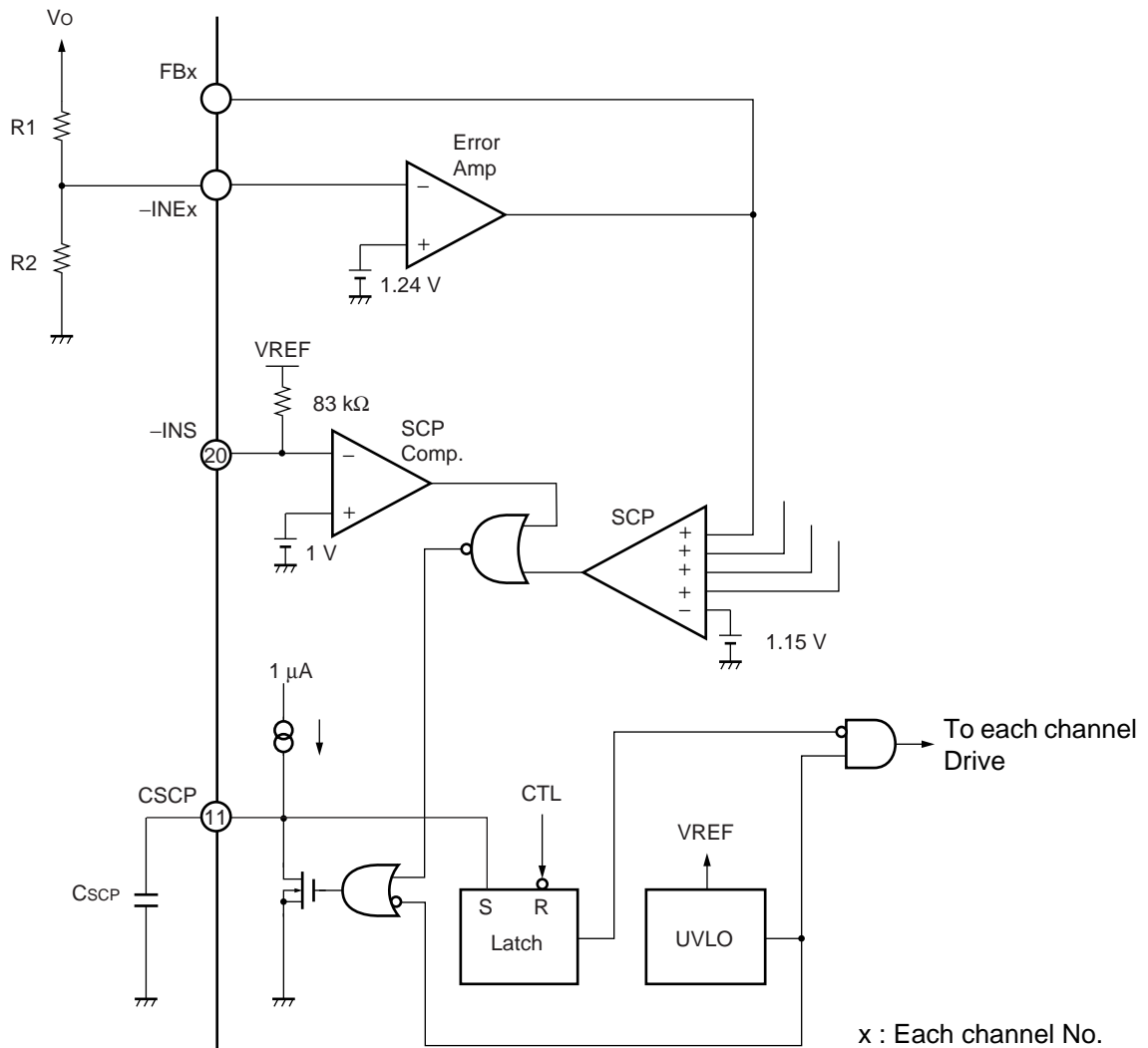
$$t_{CSCP} \text{ (s)} \approx 0.70 \times C_{SCP} \text{ (\mu F)}$$

When the capacitor C_{SCP} is charged to the threshold voltage ($V_{TH} \approx 0.70 \text{ V}$), the latch is set and the external FET is turned off (dead time is set to 100%). At this point, the latch input is closed and the CSCP terminal (pin 11) is held at "L" level.

In addition, the short-circuit detection from external input is capable by using $-\text{INS}$ terminal (pin 20) on the short-circuit detection comparator (SCP Comp.). The short-circuit detection operation starts when $-\text{INS}$ terminal voltage is less than threshold voltage ($V_{TH} \approx 1 \text{ V}$).

When the power supply is turn on back or V_{REF} terminal (pin 7) voltage is less than 1.5 V (Min) by setting CTL terminal (pin 6) to "L" level, the latch is released.

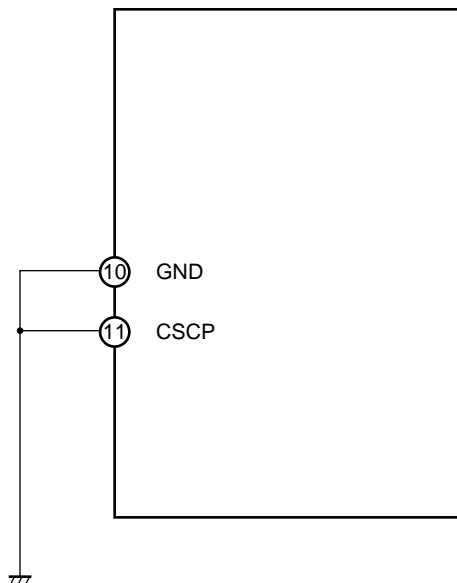
• Timer-latch short-circuit protection circuit



■ TREATMENT WITHOUT USING CSCP TERMINAL

When not using the timer-latch short-circuit protection circuit, connect the CSCP terminal (pin 11) to GND (pin 10) with the shortest distance.

- Treatment without using CSCP



■ SETTING THE DEAD TIME

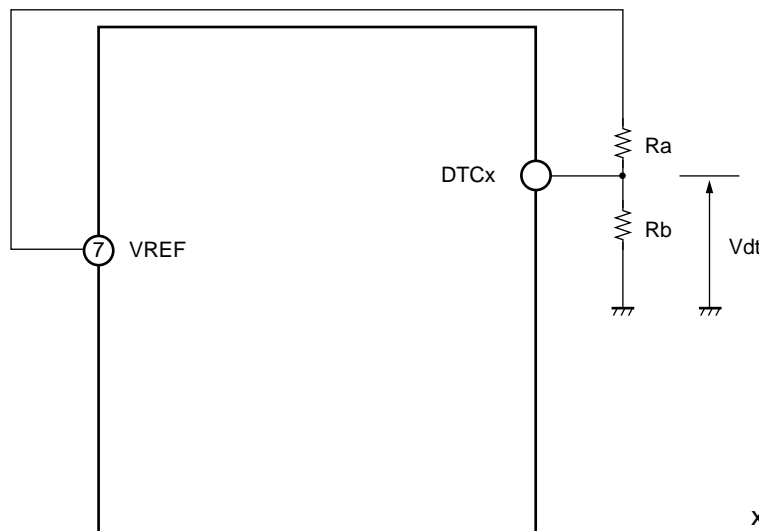
When the device is set for step-up inverted output based on the step-up or step-up/down Zeta conversion, step-up/down Sepic conversion or flyback conversion, the FB terminal voltage may reach and exceed the triangular wave voltage due to load fluctuation. If this is the case, the output transistor is fixed to a full-ON state (ON duty = 100 %). To prevent this, set the maximum duty of the output transistor. To set it, set the voltage at the DTC terminal by applying a resistive voltage divider to the VREF voltage as shown below.

When the DTC terminal voltage is higher than the triangular wave voltage, the output transistor is turned on. The maximum duty calculation formula assuming that triangular wave amplitude = 0.5 V and triangular wave lower voltage = 0.4 V is given below.

$$\text{DUTY (ON) Max} = \frac{V_{dt} - 0.4 \text{ V}}{0.5 \text{ V}} \times 100 (\%), \quad V_{dt} = \frac{R_b}{R_a + R_b} \times V_{REF}$$

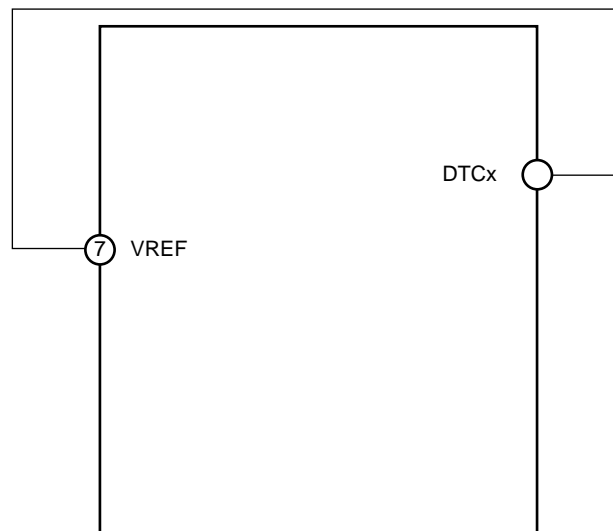
When the DTC terminal is not used, connect it directly to the VREF terminal (pin 7) as shown below (when no dead time is set).

- When using DTC to set dead time



x : Each channel No.

- When no dead time is set



x : Each channel No.

■ OPERATION EXPLANATION WHEN CTL TURNING ON AND OFF

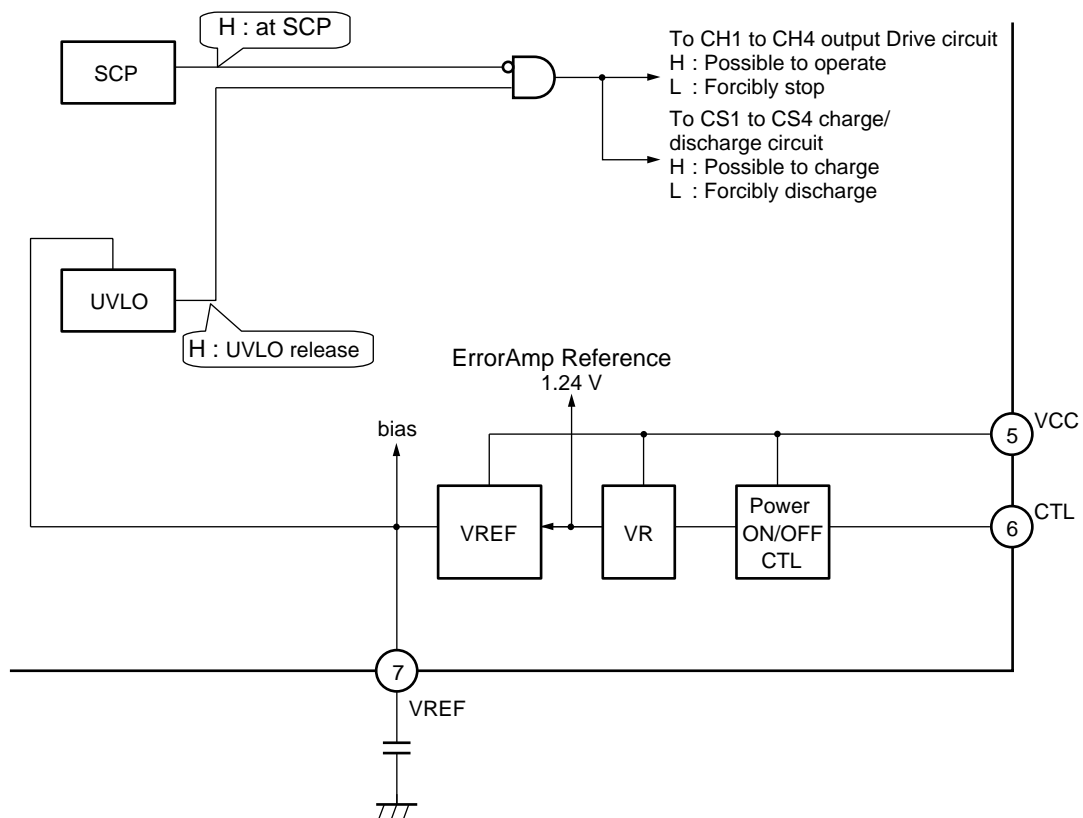
When CTL is turned on, internal reference voltage VR and VREF generate. When VREF exceeds threshold voltage (VTH) of UVLO (under voltage lockout protection circuit), UVLO are released, and the operation of output Drive circuit of each channel becomes possible.

When CTL is off, VR and VREF fall. When VREF decreases and UVLO fall below each reset voltage (VRST), UVLO operates and output Drive circuit of each channel is forcibly done the operation stop, and makes the output off state.

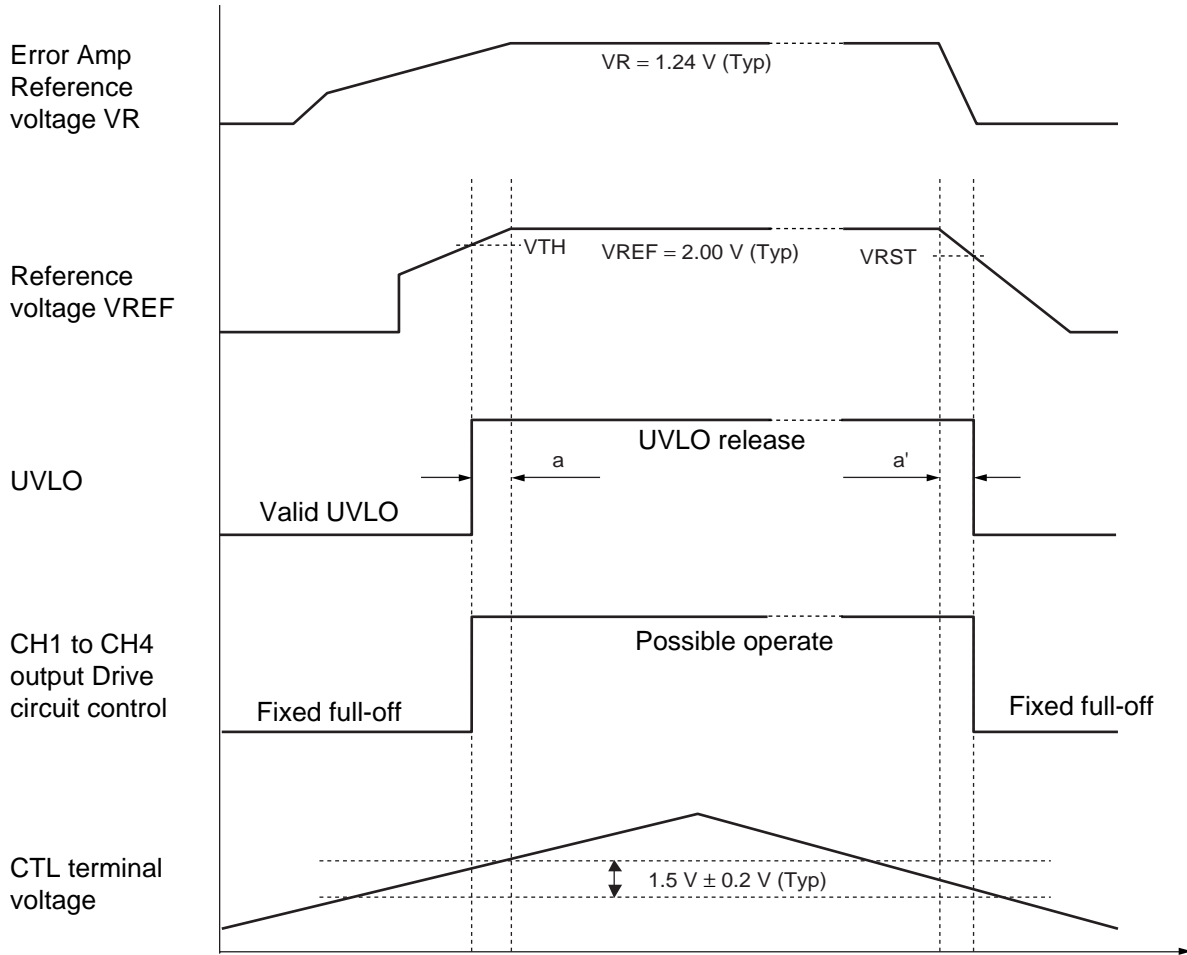
When period to reaching to 2.0 V by VREF voltage after UVLO are released by turning on CTL (refer to a in “• Timing Chart”), and VREF decreases from 2.0 V after turning off CTL and the period until do the operation of UVLO (refer to a' in “• Timing Chart”), the bias voltage and the bias current in IC do not reach a prescribed value because VREF which is the reference voltage does not reach 2.0 V, and the speed of response for IC has decreased.

Note : Moreover, when it does the turning on and off of the input sudden change, the load sudden change, IC cannot conform and the output might overshoot.
Therefore, impress the voltage to CTL terminal by which the VREF terminal voltage never stays in the above-mentioned period.

• CTL Block Equivalent Circuit

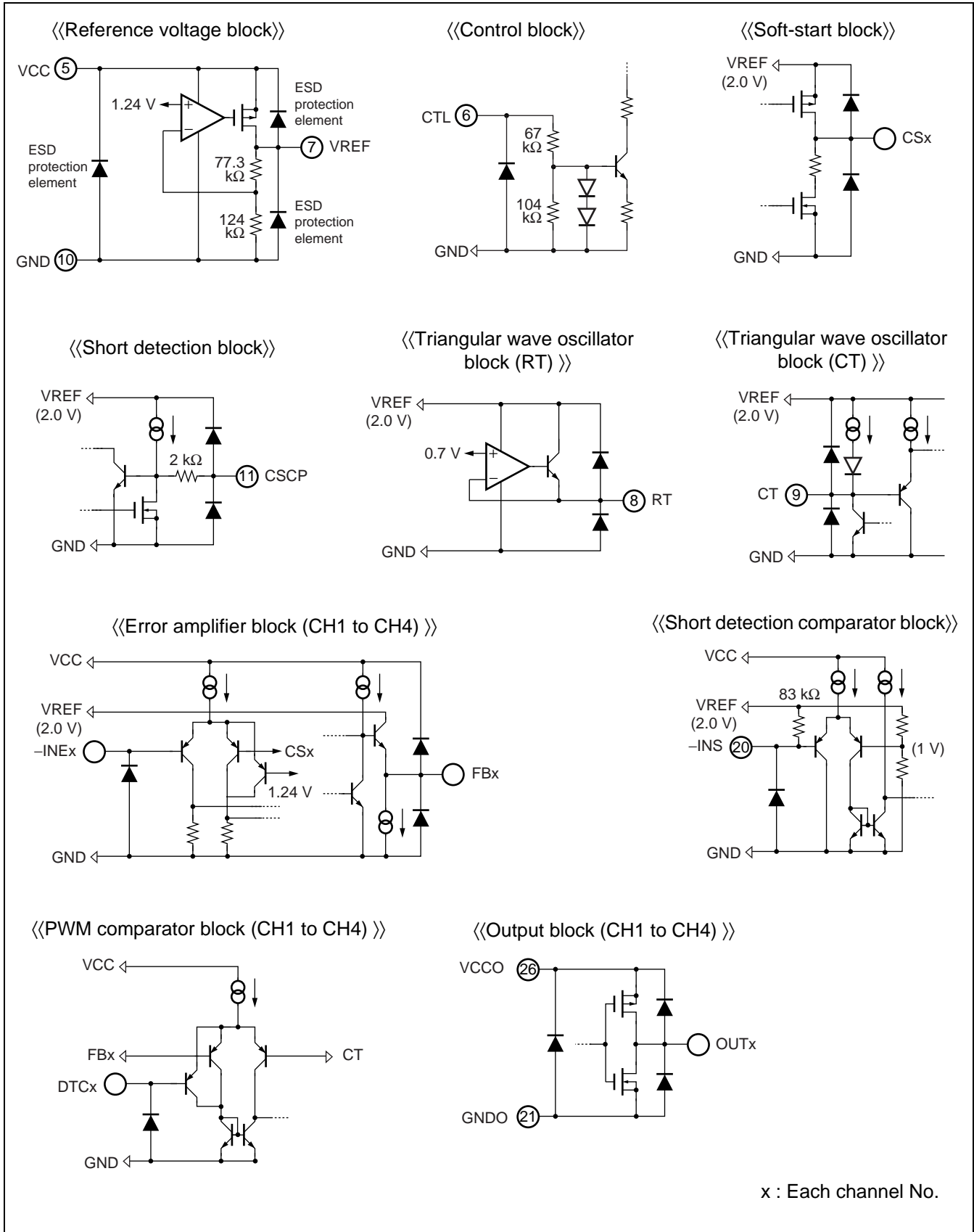


• Timing Chart

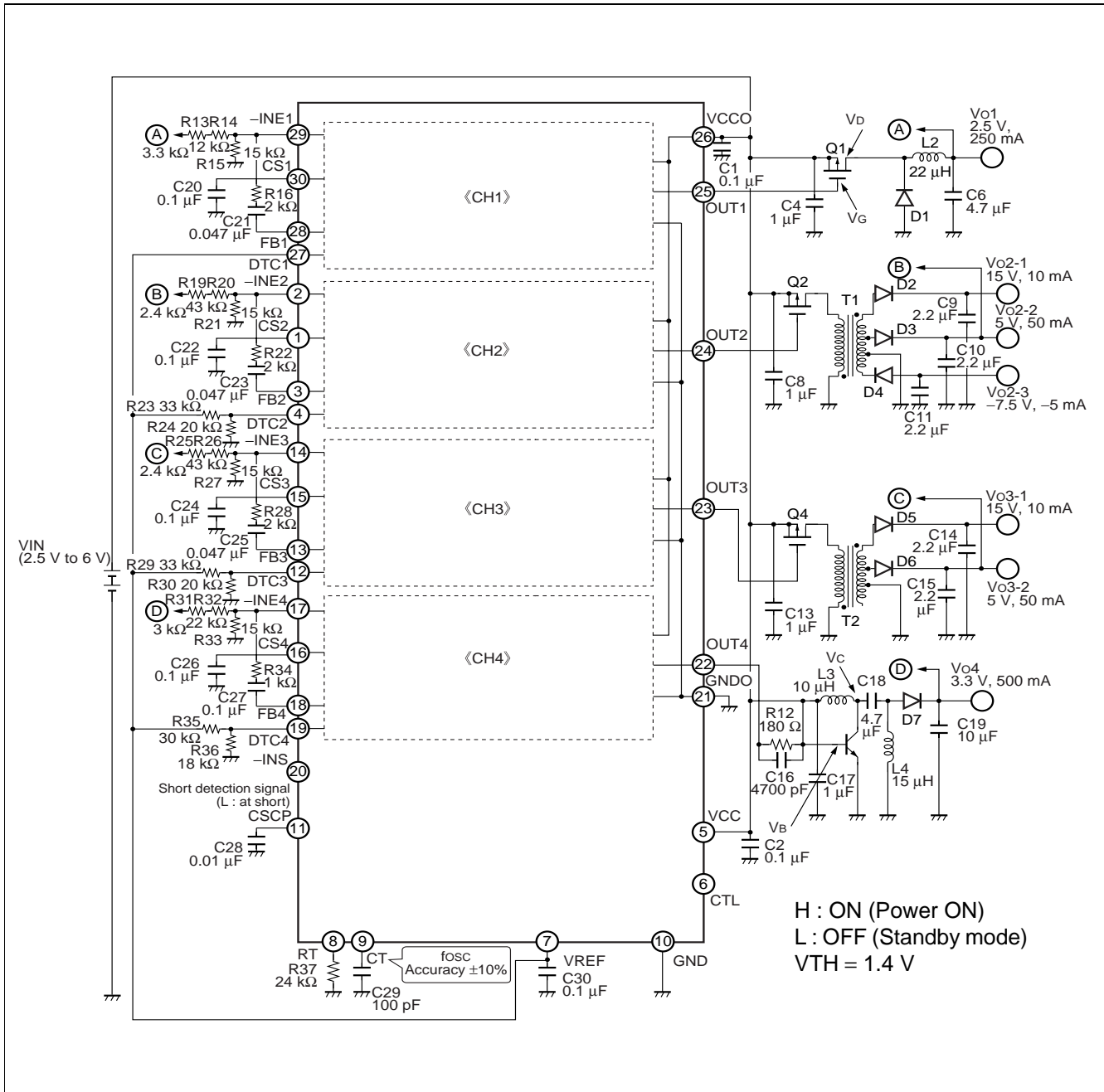


MB39A102

I/O EQUIVALENT CIRCUIT



APPLICATION EXAMPLE



MB39A102

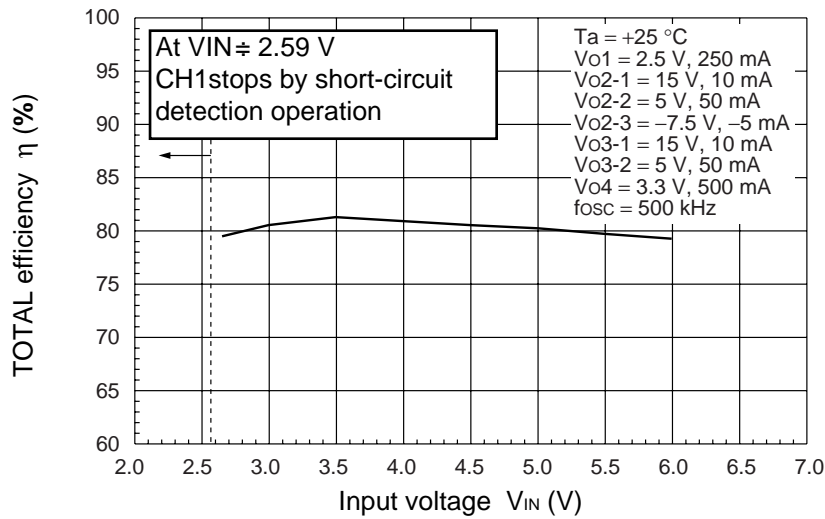
■ PARTS LIST

| COMPONENT | ITEM | SPECIFICATION | | VENDOR | PARTS NO. |
|--|--|--|--|--|--|
| Q1, Q2, Q4 Q5 | Pch FET NPN Tr | VDS = -20 V, ID = -1.5 A VCEO = 15 V, IC = 3 A | | SANYO SANYO | MCH3309 CPH3206 |
| D1, D7 D2 to D6 | Diode Diode | VF = 0.4 V (Max) , at IF = 1 A VF = 0.55 V (Max) , at IF = 0.5 A | | SANYO SANYO | SBS004 SB05-05CP |
| L2 L3 L4 | Inductor Inductor Inductor | 22 μ H 10 μ H 15 μ H | 0.63 A, 160 m Ω 0.94 A, 67 m Ω 0.76 A, 120 m Ω | TDK TDK TDK | RLF5018T-220MR63 RLF5018T-100MR94 RLF5018T-150MR76 |
| T1, T2 | Transformer | — | — | SUMIDA | CLQ52 5388-T095 |
| C1, C2 C4, C8, C13 C6 C9 to C11 C14, C15 C16 C17 C18 C19 C20, C22, C24 C21, C23, C25 C26, C27, C30 C28 C29 | Ceramics Condenser | 0.1 μ F 1 μ F 4.7 μ F 2.2 μ F 2.2 μ F 4700 pF 1 μ F 4.7 μ F 10 μ F 0.1 μ F 0.047 μ F 0.1 μ F 0.01 μ F 100 pF | 50 V 25 V 10 V 16 V 16 V 50 V 25 V 10 V 6.3 V 50 V 50 V 50 V 50 V 50 V | TDK | C1608JB1H104K C3216JB1E105K C3216JB1A475M C3216JB1C225K C3216JB1C225K C1608JB1H472K C3216JB1E105K 3216JB1A475M C3216JB0J106M C1608JB1H104K C1608JB1H473K C1608JB1H104K C1608JB1H103K C1608CH1H101J |
| R12 R13 R14 R15, R21, R27 R16, R22, R28 R19, R25 R20, R26 R23, R29 R24, R30 R31 R32 R33 R34 R35 R36 R37 | Resistor | 180 Ω 3.3 k Ω 12 k Ω 15 k Ω 2 k Ω 2.4 k Ω 43 k Ω 33 k Ω 20 k Ω 3 k Ω 22 k Ω 15 k Ω 1 k Ω 30 k Ω 18 k Ω 24 k Ω | 0.5 % | ssm | RR0816P-181-D RR0816P-332-D RR0816P-123-D RR0816P-153-D RR0816P-202-D RR0816P-242-D RR0816P-433-D RR0816P-333-D RR0816P-203-D RR0816P-302-D RR0816P-223-D RR0816P-153-D RR0816P-102-D RR0816P-303-D RR0816P-183-D RR0816P-243-D |

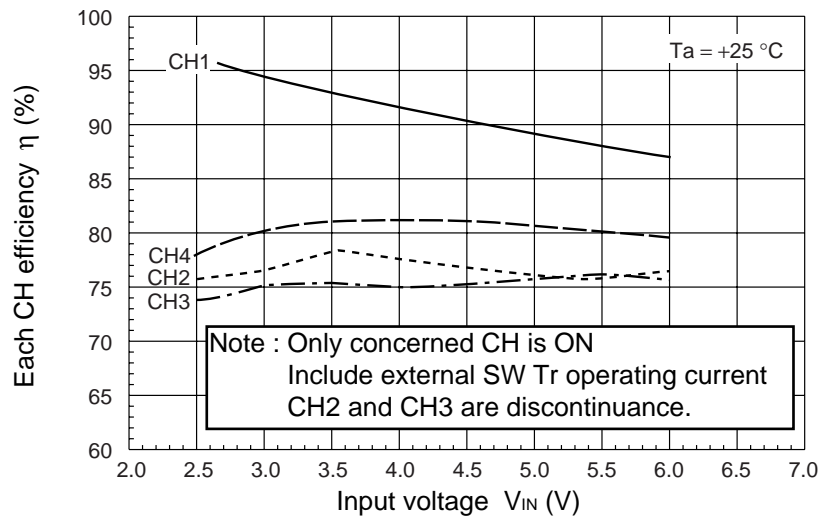
Note : SANYO : SANYO Electric Co., Ltd.
 TDK : TDK Corporation
 SUMIDA : SUMIDA Electric Co., Ltd.
 ssm : SUSUMU Co., Ltd.

REFERENCE DATA

TOTAL Efficiency vs. Input Voltage

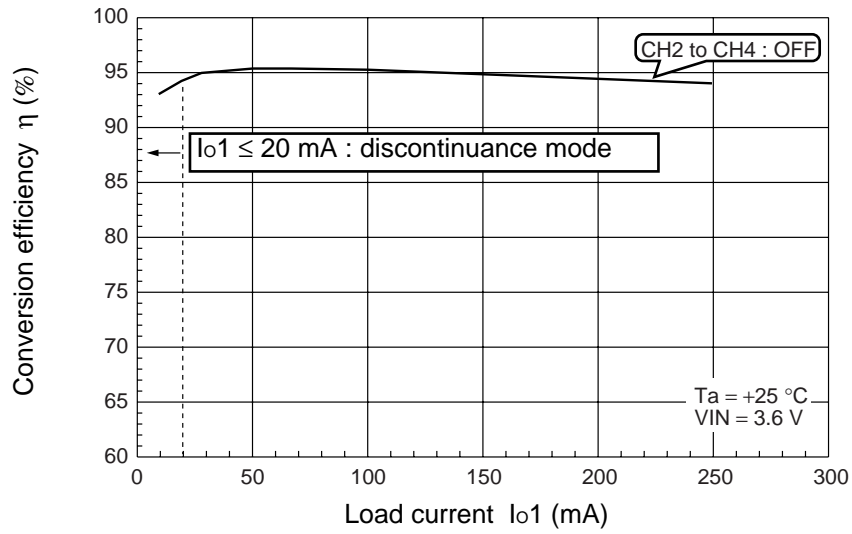


Each CH Efficiency vs. Input Voltage

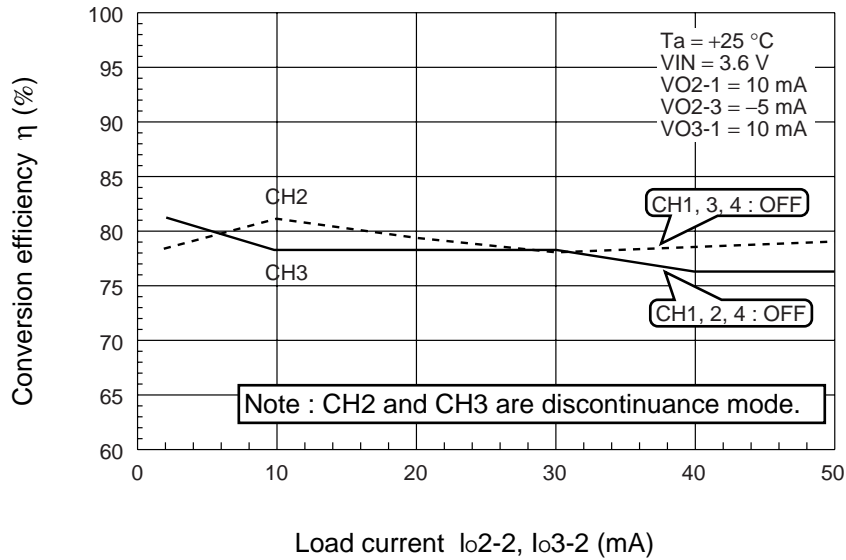


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Conversion Efficiency vs. Load Current (CH1)

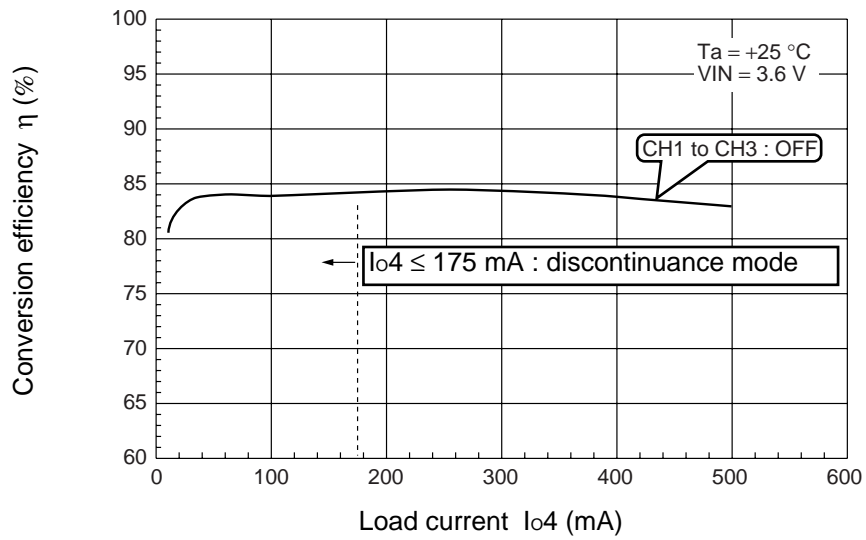


Conversion Efficiency vs. Load Current (CH2, CH3)



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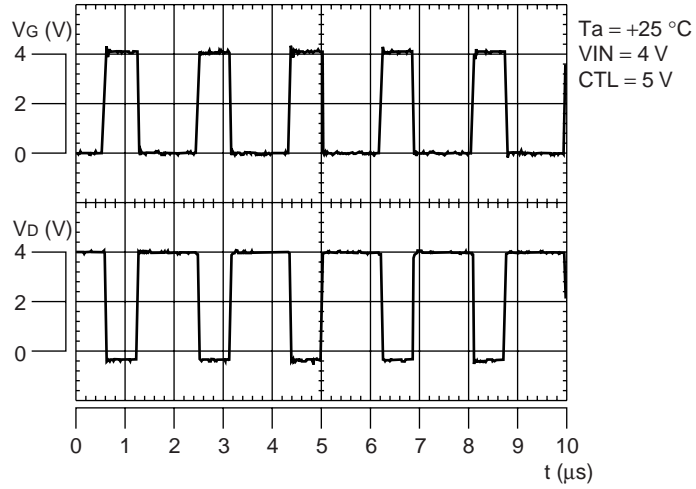
Conversion Efficiency vs. Load Current (CH4)



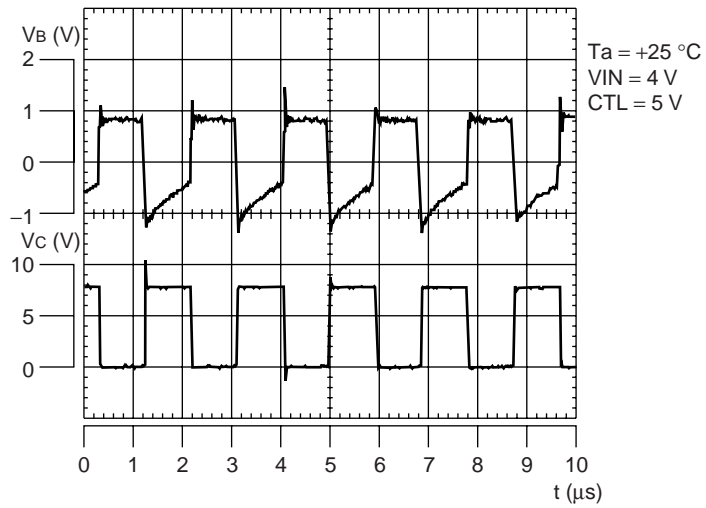
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Switching Wave Form (CH1)



Switching Wave Form (CH4)



■ USAGE PRECAUTION

- Printed circuit board ground lines should be set up with consideration for common impedance.
- Take appropriate static electricity measures.
 - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
 - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
 - Work platforms, tools, and instruments should be properly grounded.
 - Working personnel should be grounded with resistance of 250 k Ω to 1 M Ω between body and ground.
- Do not apply negative voltages.

The use of negative voltages below -0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

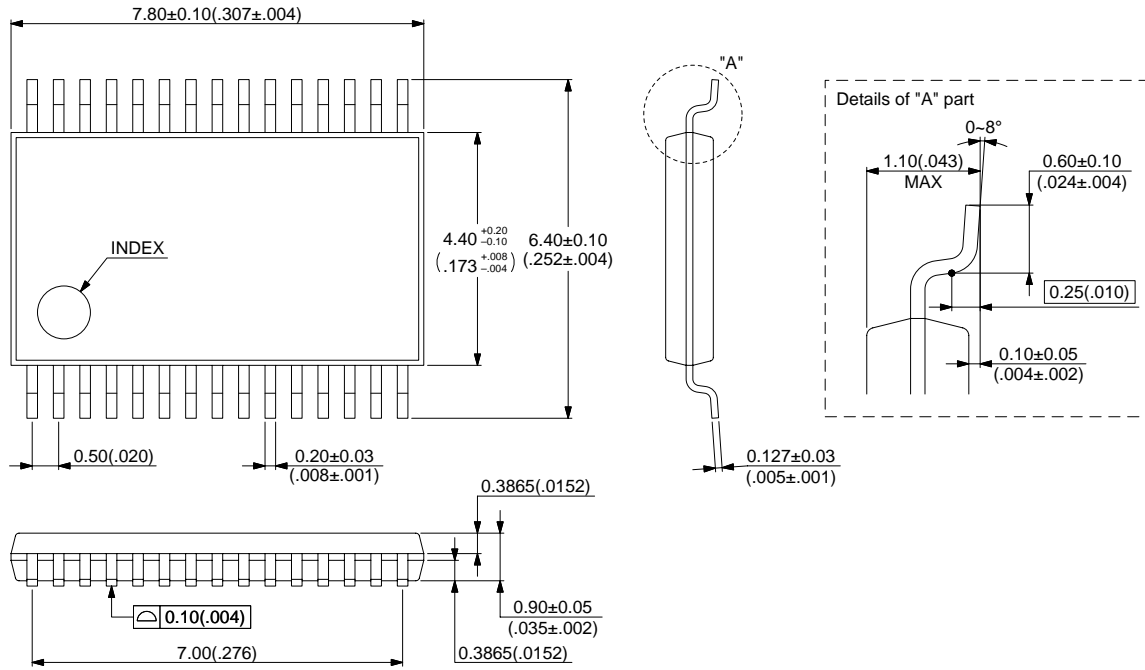
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|---------------------------------------|---------|
| MB39A102PFT | 30-pin plastic TSSOP (FPT-30P-M04) | |
| MB39A102PV3 | 32-pad plastic BCC (LCC-32P-M15) | |

MB39A102

■ PACKAGE DIMENSIONS

30-pin plastic TSSOP
(FPT-30P-M04)



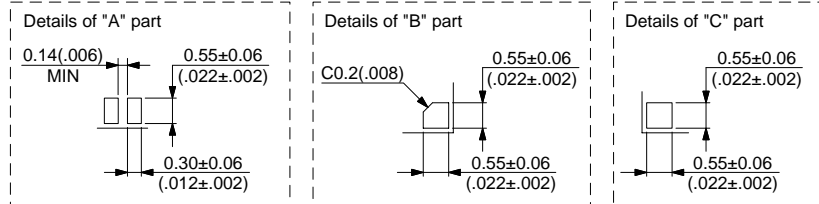
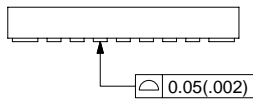
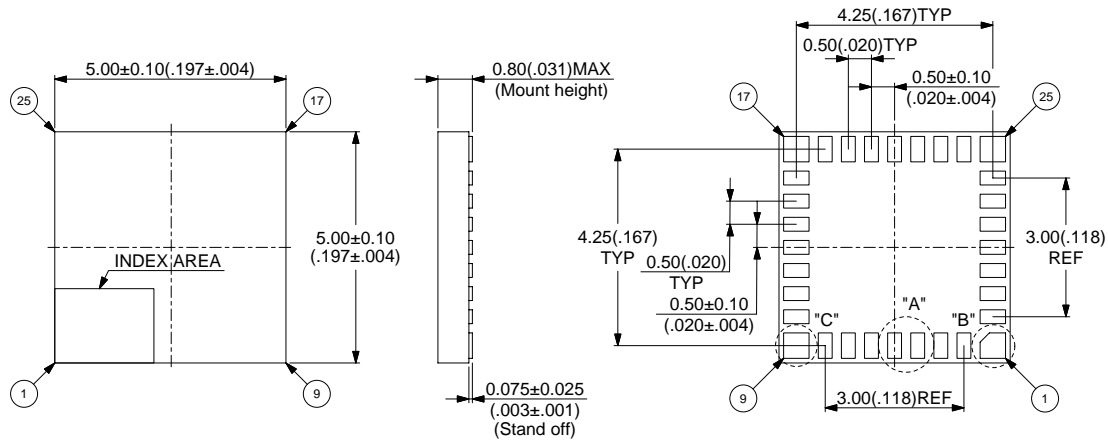
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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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32-pad plastic BCC (LCC-32P-M15)



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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