

# 8-BIT, ECL-INTERFACED PROGRAMMABLE DELAY LINE (SERIES PDU10256H)



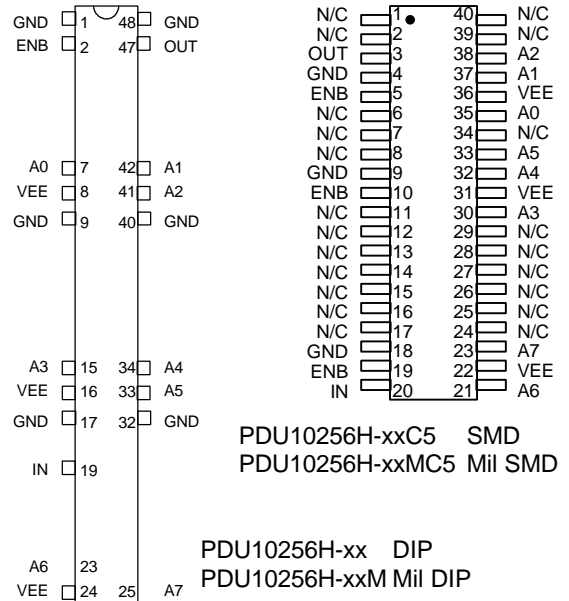
## FEATURES

- Digitally programmable in 128 delay steps
- Monotonic delay-versus-address variation
- Precise and stable delays
- Input & outputs fully 10KH-ECL interfaced & buffered
- Fits 48-pin DIP socket

## PIN DESCRIPTIONS

- IN Signal Input
- OUT Signal Output
- A0-A7 Address Bits
- ENB Output Enable
- VEE -5 Volts
- GND Ground

## PACKAGES



## FUNCTIONAL DESCRIPTION

The PDU10256H-series device is an 8-bit digitally programmable delay line. The delay,  $TD_A$ , from the input pin (IN) to the output pin (OUT) depends on the address code (A7-A0) according to the following formula:

$$TD_A = TD_0 + T_{INC} * A$$

where A is the address code,  $T_{INC}$  is the incremental delay of the device, and  $TD_0$  is the inherent delay of the device. The incremental delay is specified by the dash number of the device and can range from 0.5ns through 10ns, inclusively. The enable pin (ENB) is held LOW during normal operation. When this signal is brought HIGH, OUT is forced into a LOW state. The address is not latched and must remain asserted during normal operation.

## SERIES SPECIFICATIONS

- Total programmed delay tolerance:** 5% or 2ns, whichever is greater
- Inherent delay ( $TD_0$ ):** 12ns typical
- Setup time and propagation delay:**
  - Address to input setup ( $T_{AIS}$ ):** 3.6ns
  - Disable to output delay ( $T_{DISO}$ ):** 1.7ns typical
- Operating temperature:** 0° to 70° C
- Temperature coefficient:** 100PPM/°C (excludes  $TD_0$ )
- Supply voltage  $V_{EE}$ :** -5VDC  $\pm$  5%
- Power Dissipation:** 925mw typical (no load)
- Minimum pulse width:** 16% of total delay

## DASH NUMBER SPECIFICATIONS

Part Number	Incremental Delay Per Step (ns)	Total Delay (ns)
PDU10256H-.5	0.5 $\pm$ 0.3	127.5 $\pm$ 6.4
PDU10256H-1	1.0 $\pm$ 0.5	255 $\pm$ 12.8
PDU10256H-2	2.0 $\pm$ 0.5	510 $\pm$ 25.5
PDU10256H-3	3.0 $\pm$ 1.0	765 $\pm$ 38.2
PDU10256H-4	4.0 $\pm$ 1.0	1020 $\pm$ 51.0
PDU10256H-5	5.0 $\pm$ 1.5	1275 $\pm$ 63.8
PDU10256H-6	6.0 $\pm$ 1.5	1530 $\pm$ 76.5
PDU10256H-8	8.0 $\pm$ 2.0	2040 $\pm$ 102
PDU10256H-10	10.0 $\pm$ 2.0	2550 $\pm$ 128

**NOTE:** Any dash number between .5 and 10 not shown is also available.

## APPLICATION NOTES

### ADDRESS UPDATE

The PDU10256H is a memory device. As such, special precautions must be taken when changing the delay address in order to prevent spurious output signals. The timing restrictions are shown in Figure 1.

After the last signal edge to be delayed has appeared on the OUT pin, a minimum time,  $T_{OAX}$ , is required before the address lines can change. This time is given by the following relation:

$$T_{OAX} = \max \{ (A_i - A_{i-1}) * T_{INC} , 0 \}$$

where  $A_{i-1}$  and  $A_i$  are the old and new address codes, respectively. Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The possibility of spurious signals persists until the required  $T_{OAX}$  has elapsed.

A similar situation occurs when using the ENB signal to disable the output while IN is active. In this case, the unit must be held in the disabled state until the device is able to “clear” itself. This is achieved by holding the ENB signal high and the IN signal low for a time given by:

$$T_{DISH} = A_i * T_{INC}$$

Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The

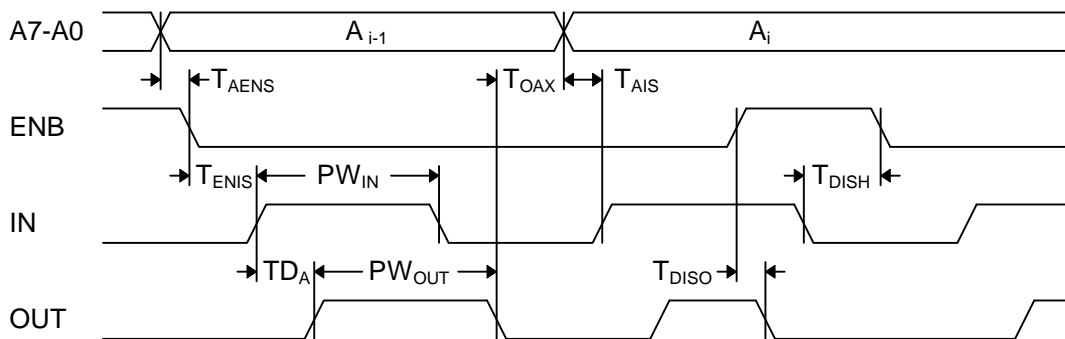
possibility of spurious signals persists until the required  $T_{DISH}$  has elapsed.

### INPUT RESTRICTIONS

There are three types of restrictions on input pulse width and period listed in the **AC Characteristics** table. The **recommended** conditions are those for which the delay tolerance specifications and monotonicity are guaranteed. The **suggested** conditions are those for which signals will propagate through the unit without significant distortion. The **absolute** conditions are those for which the unit will produce some type of output for a given input.

When operating the unit between the recommended and absolute conditions, the delays may deviate from their values at low frequency. However, these deviations will remain constant from pulse to pulse if the input pulse width and period remain fixed. In other words, the delay of the unit exhibits frequency and pulse width dependence when operated beyond the recommended conditions. Please consult the technical staff at Data Delay Devices if your application has specific high-frequency requirements.

Please note that the increment tolerances listed represent a design goal. Although most delay increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.



**Figure 1: Timing Diagram**

## DEVICE SPECIFICATIONS

### TABLE 1: AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	UNITS
Total Programmable Delay	$TD_T$		127	$T_{INC}$
Inherent Delay	$TD_0$		12.0	ns
Disable to Output Low Delay	$T_{DISO}$		1.7	ns
Address to Enable Setup Time	$T_{AENS}$	1.0		ns
Address to Input Setup Time	$T_{AIS}$	3.6		ns
Enable to Input Setup Time	$T_{ENIS}$	3.6		ns
Output to Address Change	$T_{OAX}$	See Text		
Disable Hold Time	$T_{DISH}$	See Text		
Input Period	Absolute	$PER_{IN}$	12	% of $TD_T$
	Suggested	$PER_{IN}$	32	% of $TD_T$
	Recommended	$PER_{IN}$	200	% of $TD_T$
Input Pulse Width	Absolute	$PW_{IN}$	6	% of $TD_T$
	Suggested	$PW_{IN}$	16	% of $TD_T$
	Recommended	$PW_{IN}$	100	% of $TD_T$

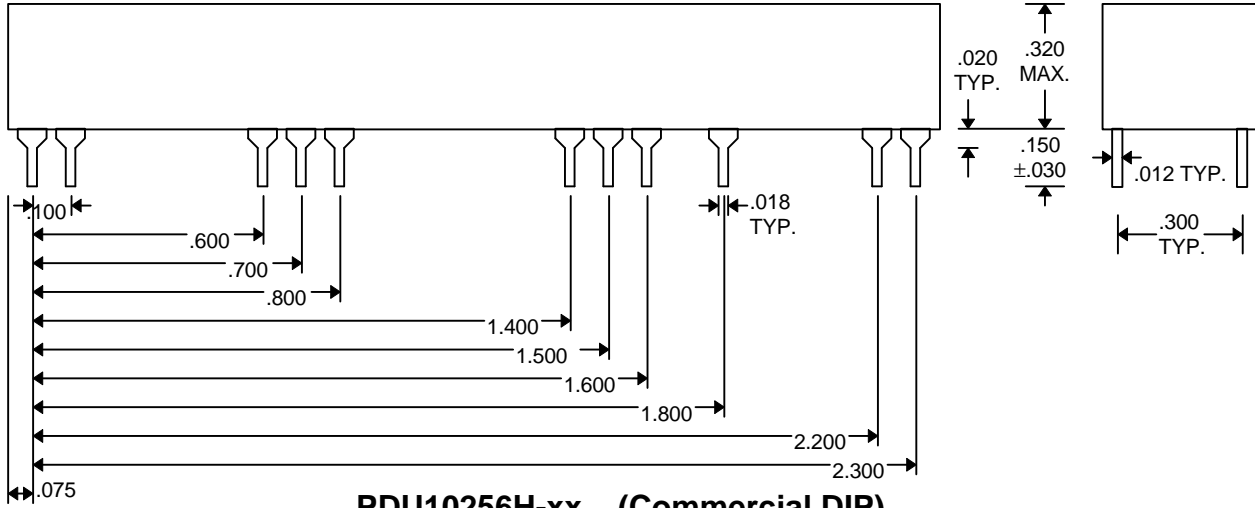
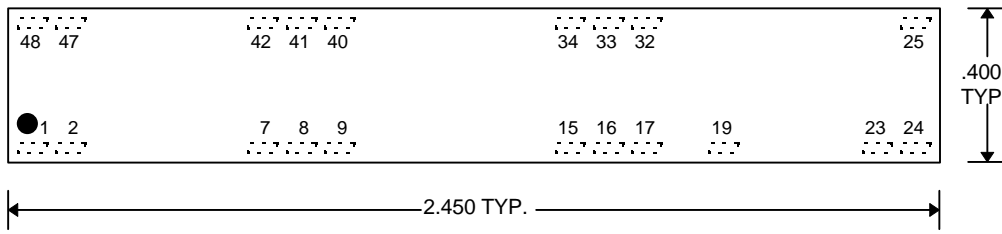
### TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	$V_{EE}$	-7.0	0.3	V	
Input Pin Voltage	$V_{IN}$	$V_{EE} - 0.3$	0.3	V	
Storage Temperature	$T_{STRG}$	-55	150	C	
Lead Temperature	$T_{LEAD}$		300	C	10 sec

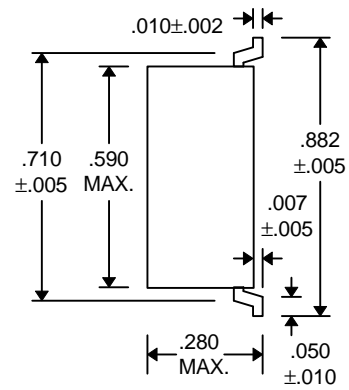
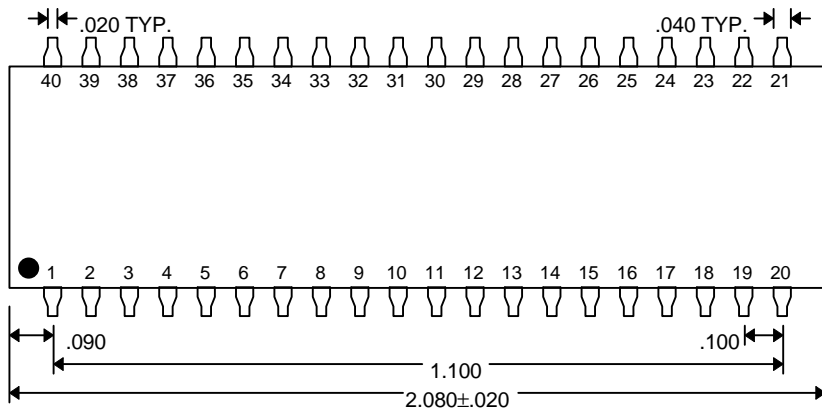
### TABLE 3: DC ELECTRICAL CHARACTERISTICS (0C to 75C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	$V_{OH}$	-1.020		-0.735	V	$V_{IH} = \text{MAX}, 50\Omega$ to -2V
Low Level Output Voltage	$V_{OL}$	-1.950		-1.600	V	$V_{IL} = \text{MIN}, 50\Omega$ to -2V
High Level Input Voltage	$V_{IH}$			-1.070	V	
Low Level Input Voltage	$V_{IL}$	-1.480			V	
High Level Input Current	$I_{IH}$			475	$\mu\text{A}$	$V_{IH} = \text{MAX}$
Low Level Input Current	$I_{IL}$	0.5			$\mu\text{A}$	$V_{IL} = \text{MIN}$

PACKAGE DIMENSIONS



**PDU10256H-xx (Commercial DIP)**  
**PDU10256H-xxM (Military DIP)**



**PDU10256H-xxC5 (Commercial SMD)**  
**PDU10256H-xxMC5 (Military SMD)**

## DELAY LINE AUTOMATED TESTING

### TEST CONDITIONS

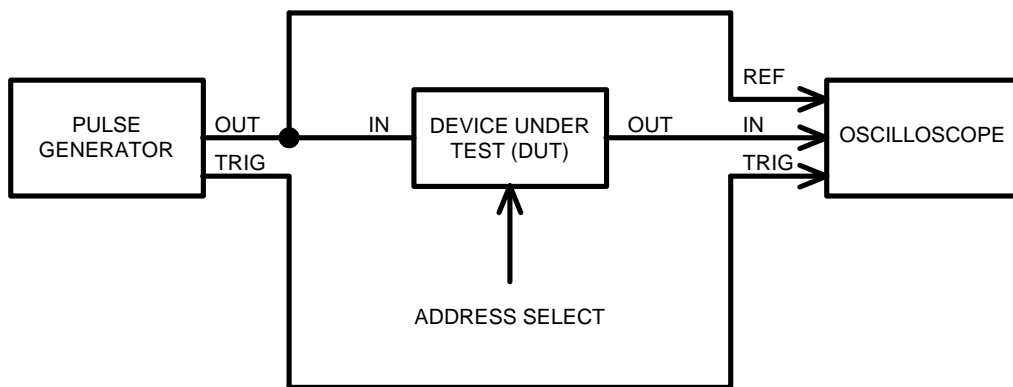
**INPUT:**

**Ambient Temperature:**  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$   
**Supply Voltage (Vcc):**  $-5.0\text{V} \pm 0.1\text{V}$   
**Input Pulse:** Standard 10KH ECL levels  
**Source Impedance:**  $50\Omega$  Max.  
**Rise/Fall Time:** 2.0 ns Max. (measured between 20% and 80%)  
**Pulse Width:**  $PW_{IN} = 1.5 \times \text{Total Delay}$   
**Period:**  $PER_{IN} = 10 \times \text{Total Delay}$

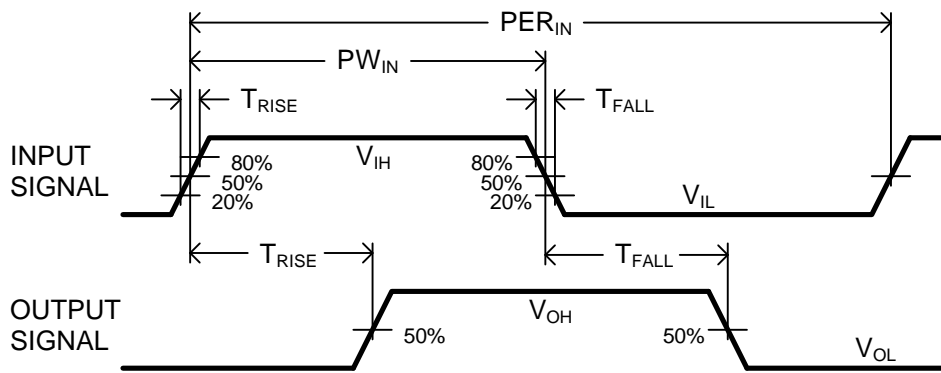
**OUTPUT:**

**Load:**  $50\Omega$  to  $-2\text{V}$   
**C<sub>load</sub>:**  $5\text{pf} \pm 10\%$   
**Threshold:**  $(V_{OH} + V_{OL}) / 2$   
 (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.



**Test Setup**



**Timing Diagram For Testing**