

# 74LVX174

## Low Voltage Hex D-Type Flip-Flop with Master Reset

### General Description

The LVX174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

### Features

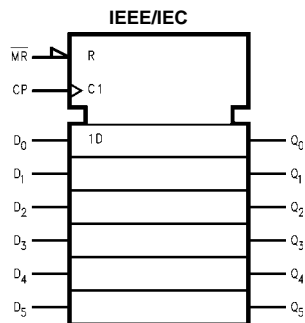
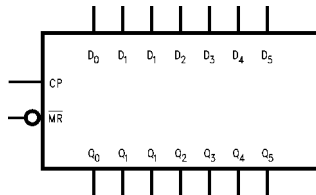
- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

### Ordering Code:

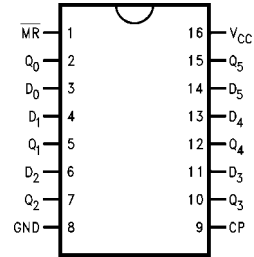
Order Number	Package Number	Package Description
74LVX174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>5</sub>	Data Inputs
CP	Clock Pulse Input
MR	Master Reset Input
Q <sub>0</sub> -Q <sub>5</sub>	Outputs

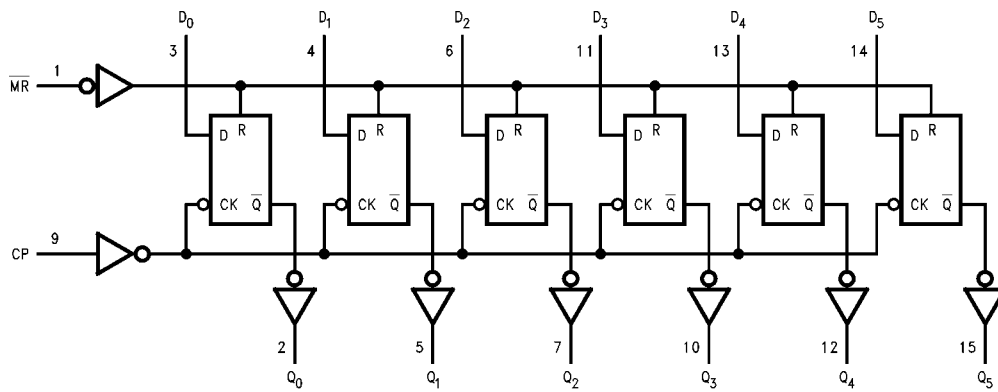
74LVX174 Low Voltage Hex D-Type Flip-Flop with Master Reset

**Truth Table**

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	$D_n$	$Q_n$
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↗	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

**Logic Diagram**



**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current	
( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	180 mW

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0	1.5			1.5		V		
		3.0	2.0			2.0				
		3.6	2.4			2.4				
$V_{IL}$	LOW Level Input Voltage	2.0			0.5		0.5	V		
		3.0			0.8		0.8			
		3.6			0.8		0.8			
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IL}$ or $V_{IH}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				$I_{OH} = -50 \mu\text{A}$
		3.0	2.58			2.48				$I_{OH} = -4 \text{ mA}$
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IL}$ or $V_{IH}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			$I_{OL} = 50 \mu\text{A}$
		3.0			0.36		0.44			$I_{OL} = 4 \text{ mA}$
$I_{IN}$	Input Leakage Current	3.6			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	3.6			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

**Noise Characteristics** (Note 3)

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	$C_L$ (pF)
			Typ	Limit		
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.3	0.5	V	50
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.3	-0.5	V	50
$V_{IHD}$	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
$V_{ILD}$	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

**Note 3:** (Input  $t_r = t_f = 3$  ns)

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	C <sub>L</sub> (pF)
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time	2.7		7.6	14.5	1.0	17.5	ns	15
t <sub>PHL</sub>	CP to Q <sub>n</sub>			10.1	18.0	1.0	21.0		50
		3.3 ± 0.3		5.9	9.3	1.0	11.0		15
				8.4	12.8	1.0	14.5		50
t <sub>PHL</sub>	Propagation Delay MR to Q <sub>n</sub>	2.7		7.9	15.0	1.0	18.5	ns	15
				10.4	18.5	1.0	22.0		50
		3.3 ± 0.3		6.2	9.7	1.0	11.5		15
				8.7	13.2	1.0	15.0		50
t <sub>S</sub>	Setup Time D <sub>n</sub> to CP	2.7	7.5			8.5		ns	
		3.3 ± 0.3	5.0			6.0			
t <sub>H</sub>	Hold Time D <sub>n</sub> to CP	2.7	0			0		ns	
		3.3 ± 0.3	0			0			
t <sub>REC</sub>	Removal Time MR to CP	2.7	4.5			4.5		ns	
		3.3 ± 0.3	3.0			3.0			
t <sub>W</sub>	Clock Pulse Width	2.7	6.5			7.5		ns	
		3.3 ± 0.3	5.0			5.0			
t <sub>W</sub>	MR Pulse Width	2.7	6.5			7.5		ns	
		3.3 ± 0.3	5.0			5.0			
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	65	130		55		MHz	15
			45	60		40			50
		3.3 ± 0.3	115	180		95			15
			65	95		55			50
t <sub>OSLH</sub>	Output to Output	2.7			1.5		1.5	ns	50
t <sub>OSHL</sub>	Skew (Note 4)	3.3			1.5		1.5		

Note 4: Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|

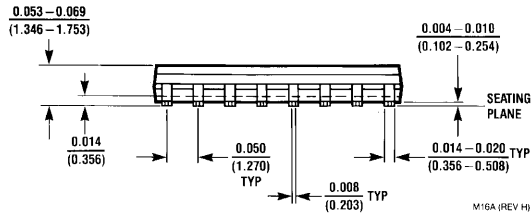
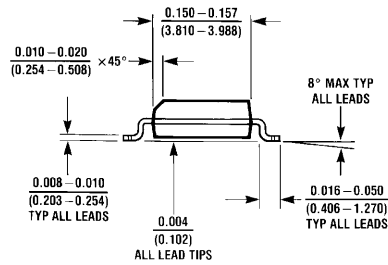
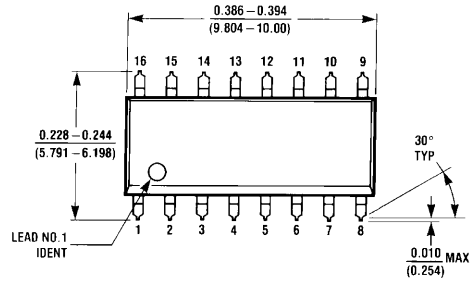
## Capacitance

Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)		29				pF

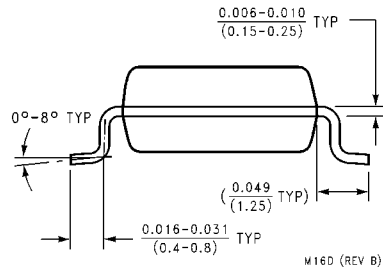
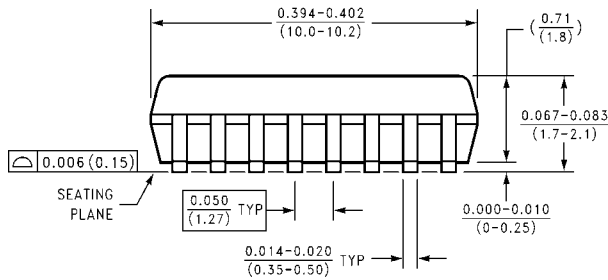
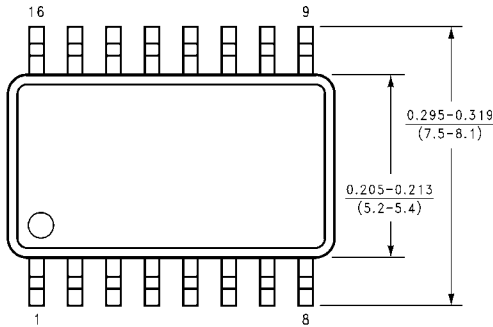
Note 5: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per F/F)}}$$

**Physical Dimensions** inches (millimeters) unless otherwise noted

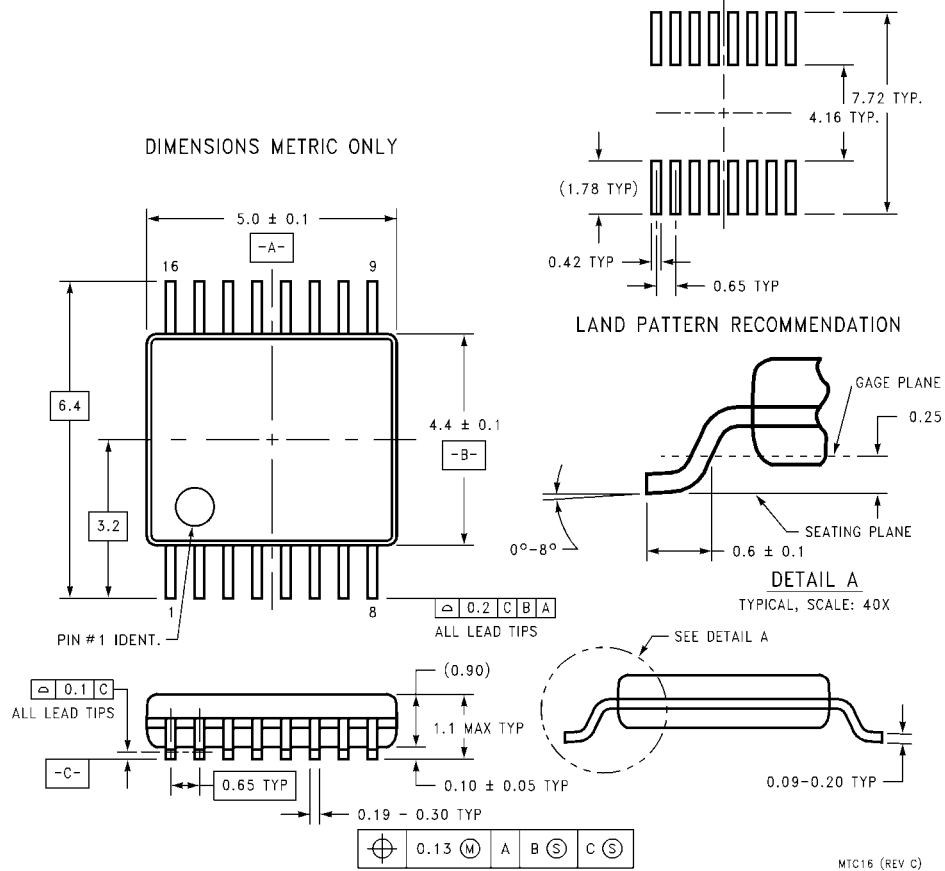


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

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