

Typical Applications

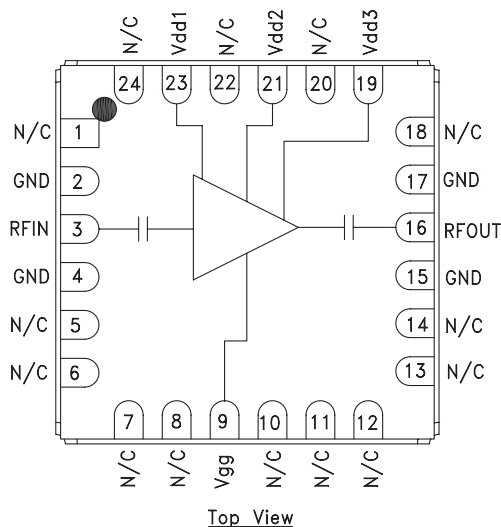
The HMC498LC4 is ideal for use as a LNA or Driver amplifier for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios & VSAT
- Test Equipment & Sensors
- Military End-Use

Features

- +36 dBm Output IP3
- Saturated Power: +26 dBm @ 23% PAE
- 22 dB Gain
- +5.0 V @ 250 mA Supply
- 50 Ohm Matched Input/Output
- RoHS Compliant 4x4 mm SMT Package

Functional Diagram



General Description

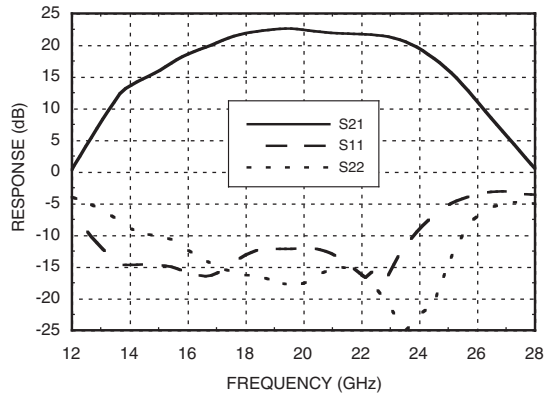
The HMC498LC4 is a high dynamic range GaAs PHEMT MMIC Medium Power Amplifier housed in a leadless "Pb free" SMT package. Operating from 17 to 24 GHz, the amplifier provides 22 dB of gain, +26 dBm of saturated power and 23% PAE from a +5.0 V supply voltage. Noise figure is 4 dB while output IP3 is +36 dBm typical enabling the HMC498LC4 to function as a low noise front end as well as a driver amplifier. The RF I/Os are DC blocked and matched to 50 Ohms for ease of use. The HMC498LC4 eliminates the need for wire bonding, allowing use of surface mount manufacturing techniques.

Electrical Specifications, $T_A = +25^\circ \text{C}$, $V_{dd1, 2, 3} = 5\text{V}$, $I_{dd} = 250 \text{ mA}^*$

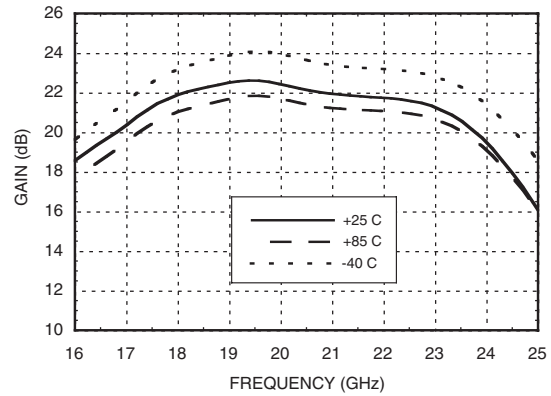
| Parameter | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Units |
|--|---------|------|------|---------|------|------|---------|------|------|-------|
| Frequency Range | 17 - 19 | | | 19 - 23 | | | 23 - 24 | | | GHz |
| Gain | 18 | 22 | | 20 | 22.5 | | 18 | 21 | | dB |
| Gain Variation Over Temperature | | 0.02 | 0.03 | | 0.02 | 0.03 | | 0.02 | 0.03 | dB/°C |
| Input Return Loss | | 13 | | | 13 | | | 10 | | dB |
| Output Return Loss | | 15 | | | 15 | | | 20 | | dB |
| Output Power for 1 dB Compression (P1dB) | 22 | 25 | | 21.5 | 24.5 | | 22.5 | 25.5 | | dBm |
| Saturated Output Power (Psat) | | 26.5 | | | 25.5 | | | 26.5 | | dBm |
| Output Third Order Intercept (IP3) | | 35 | | | 36 | | | 35.5 | | dBm |
| Noise Figure | | 4.0 | | | 4.0 | | | 4.5 | | dB |
| Supply Current (I _{dd})(V _{dd} = +5V, V _{gg} = -0.8V Typ.) | | 250 | | | 250 | | | 250 | | mA |

* Adjust V_{gg} between -2 to 0V to achieve I_{dd} = 250 mA typical.

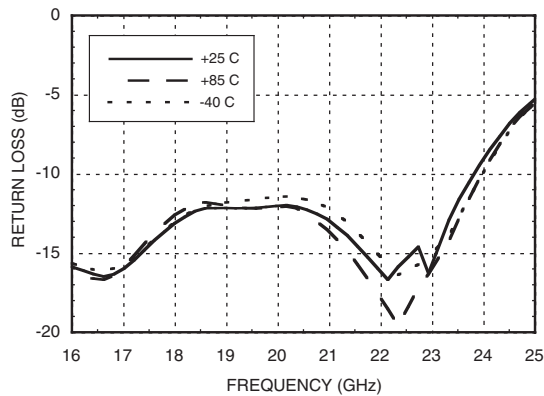
Broadband Gain & Return Loss



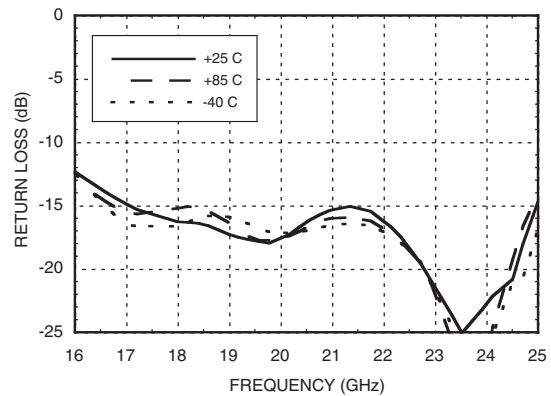
Gain vs. Temperature



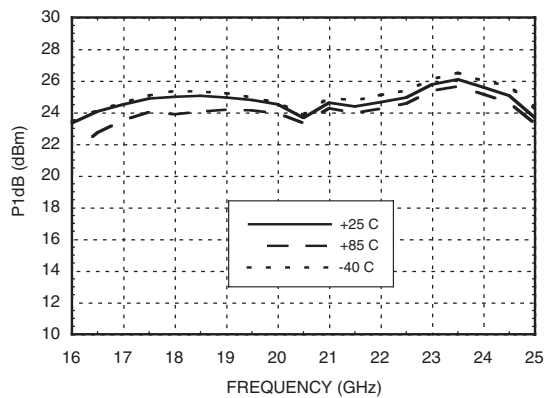
Input Return Loss vs. Temperature



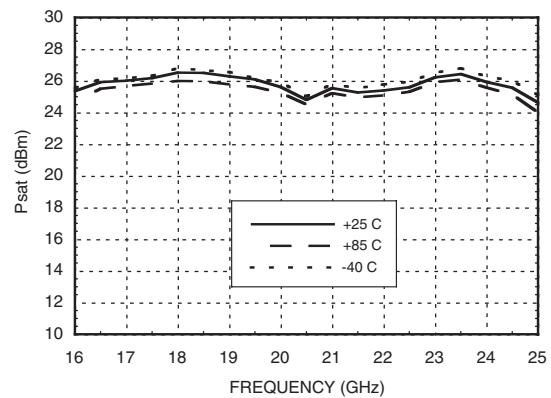
Output Return Loss vs. Temperature



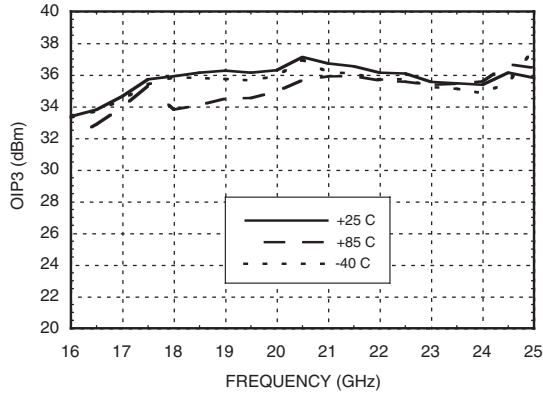
P1dB vs. Temperature



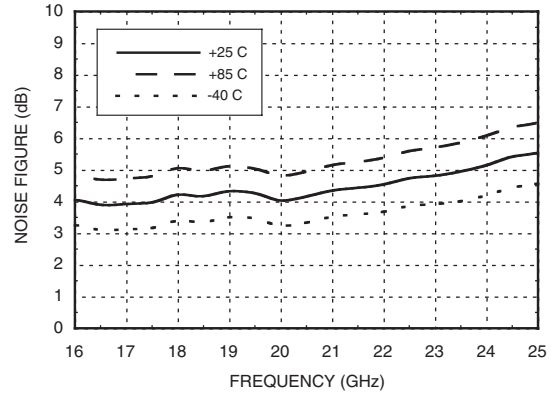
Psat vs. Temperature



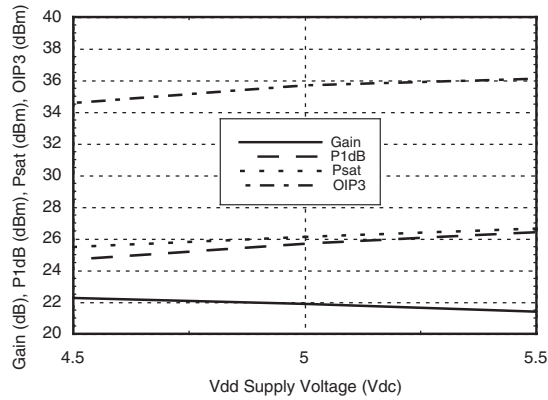
Output IP3 vs. Temperature



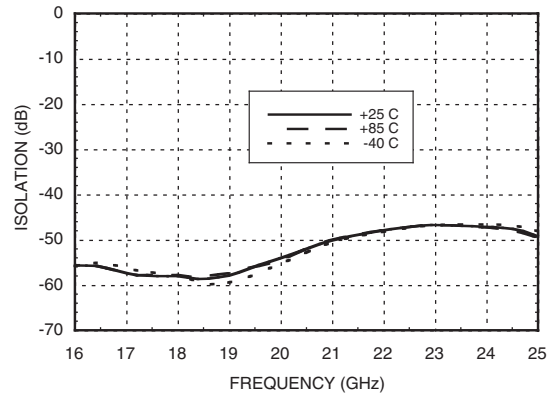
Noise Figure vs. Temperature



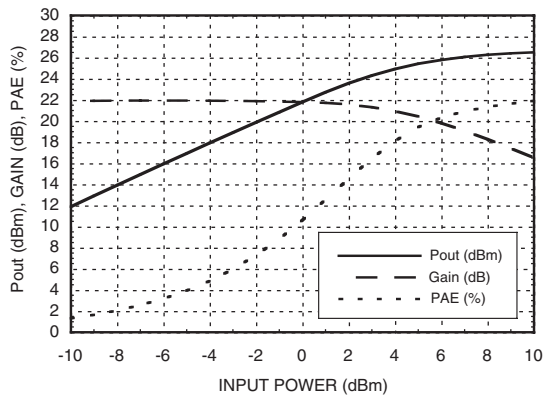
Gain, Power & OIP3 vs. Supply Voltage @ 23 GHz



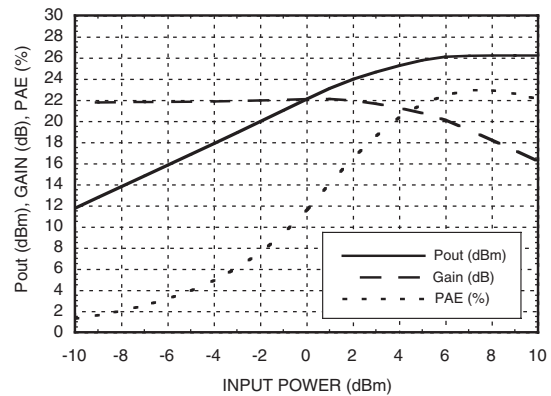
Reverse Isolation vs. Temperature



Power Compression @ 18GHz



Power Compression @ 23 GHz



Absolute Maximum Ratings

| | |
|--|----------------|
| Drain Bias Voltage (Vdd1, Vdd2, Vdd3) | +5.5 Vdc |
| Gate Bias Voltage (Vgg) | -4.0 to 0 Vdc |
| RF Input Power (RFIn)(Vdd = +5.0 Vdc) | +10 dBm |
| Channel Temperature | 175 °C |
| Continuous Pdiss (T= 85 °C) (derate 18 mW/°C above 85 °C) | 1.62 W |
| Thermal Resistance (channel to ground paddle) | 55.6 °C/W |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1A |

Typical Supply Current vs. Vdd

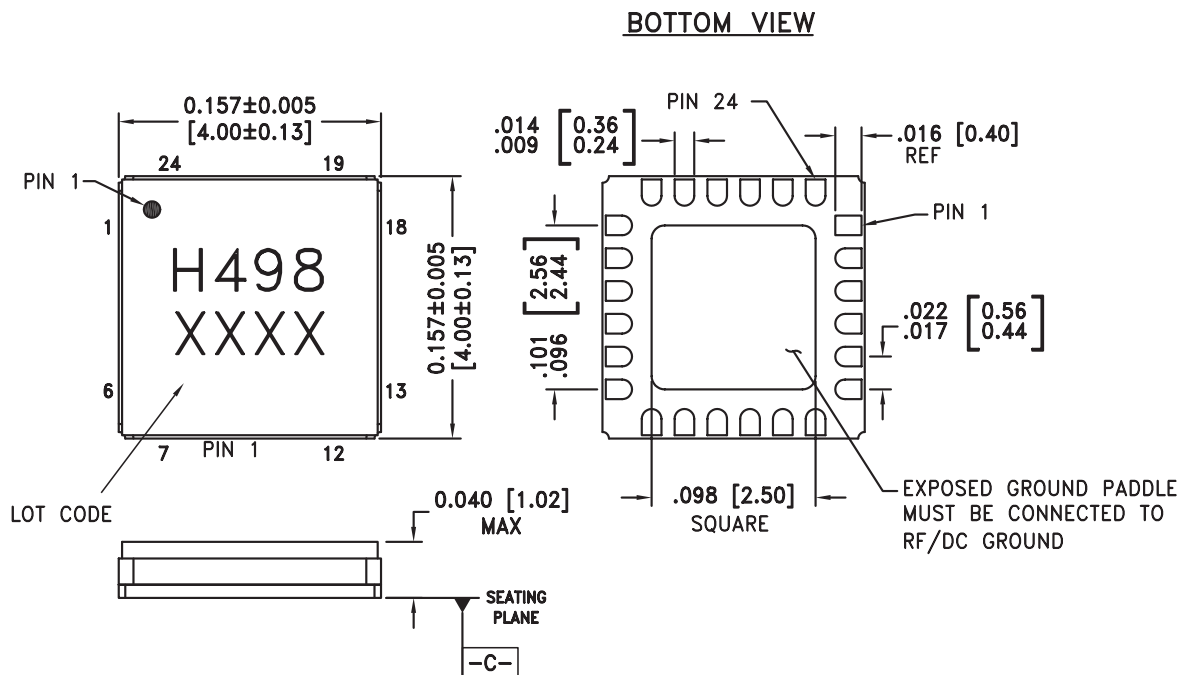
| Vdd (Vdc) | Idd (mA) |
|-----------|----------|
| +4.5 | 239 |
| +5.0 | 250 |
| +5.5 | 262 |

Note: Amplifier will operate over full voltage ranges shown above. Vgg adjusted to achieve Idd= 250 mA at +5.0V.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS


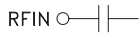
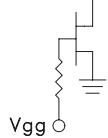
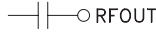

Outline Drawing



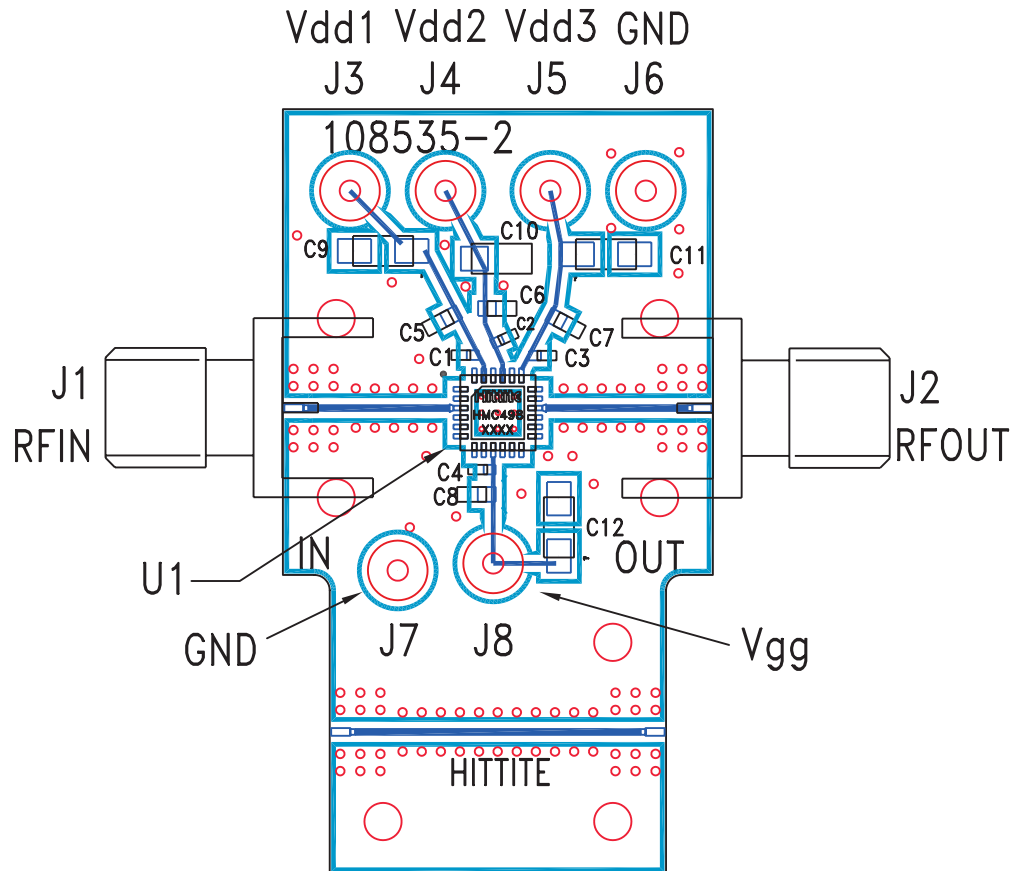
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA.
2. LEAD AND GROUND PADDLE PLATING: GOLD FLASH OVER NICKEL.
3. DIMENSIONS ARE IN INCHES (MILLIMETERS).
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, BLACK INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05MM DATUM $\square-C-\square$
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|-------------------------------|------------------|---|--|
| 1, 5-8, 10-14, 18, 20, 22, 24 | N/C | No connection required. These pins may be connected to RF/DC ground without affecting performance. | |
| 2, 4, 15, 17 | GND | Package bottom has an exposed metal paddle that must also be connected to RF/DC ground. |  |
| 3 | RFIN | This pin is AC coupled and matched to 50 Ohms from 17 - 24 GHz. |  |
| 9 | Vgg | Gate control for amplifier. Adjust to achieve Id of 250 mA. Please follow "MMIC Amplifier Biasing Procedure" Application Note. External bypass capacitors of 100 pF, 1000 pF and 2.2 μF are required. |  |
| 16 | RFOUT | This pad is AC coupled and matched to 50 Ohms from 17 - 24 GHz. |  |
| 23, 21, 19 | Vdd1, Vdd2, Vdd3 | Power Supply Voltage for the amplifier. External bypass capacitors of 100 pF, 1000pF, and 2.2 μF are required. |  |

Evaluation PCB



List of Materials for Evaluation PCB 108537 ^[1]

| Item | Description |
|--------------------|-------------------------------|
| J1, J2 | 2.92 mm PC mount K-connector |
| J3 - J8 | DC Pin |
| C1 - C4 | 100 pF capacitor, 0402 pkg. |
| C5 - C8 | 1,000 pF Capacitor, 0603 pkg. |
| C9 - C12 | 2.2µF Capacitor, Tantalum |
| U1 | HMC498LC4 Amplifier |
| PCB ^[2] | 108535 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350.

The circuit board used in this application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of VIA holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.