



SRAM MODULE 4Mbyte(1Mx32Bit) ,LOW POWER,72Pin SIMM,5V
Part No. HMS1M32M8LA

GENERAL DESCRIPTION

The HMS1M32M8LA is a static random access memory (SRAM) module containing 1,048,576 bits organized in a x32-bit configuration. The module consists of eight 512K x 8 SRAMs mounted on a 72-pin, double-sided, FR4-printed circuit board. The HMS1M32M8LA also support low data retention voltage for battery back-up operations with low data retention current. Eight chip enable inputs, (/CE0, /CE1, /CE2, /CE3, /CE4, /CE5, /CE6, /CE7) are used to enable the module's 4M bytes independently. Output enable(/OE) and write enable(/WE) can set the memory input and output.

Data is written into the SRAM memory when write enable (/WE) and chip enable (/CE) inputs are both LOW. Reading is accomplished when /WE remains HIGH and /CE and output enable (/OE) are LOW.

For reliability, this SRAM module is designed as multiple power and ground pin. All module components may be powered from a single +5V DC power supply and all inputs and outputs are fully TTL-compatible.

FEATURES

- w Part identification
 - HMS1M32M8LA : SIMM design
- w Access times : 55ns, 70ns
- w High-density 4MByte design
- w High-reliability, low-power design
- w Single + 5V \pm 0.5V power supply
- w Low data retention voltage : 2V(min)
- w Three state output and TTL-compatible
- w FR4-PCB design
- w Low profile 72-Pin SIMM

OPTIONS

- w Timing
 - 55ns access
 - 70ns access
- w Packages
 - 72-pin SIMM
 - 72-pin ZIP

MARKING

-55
-70

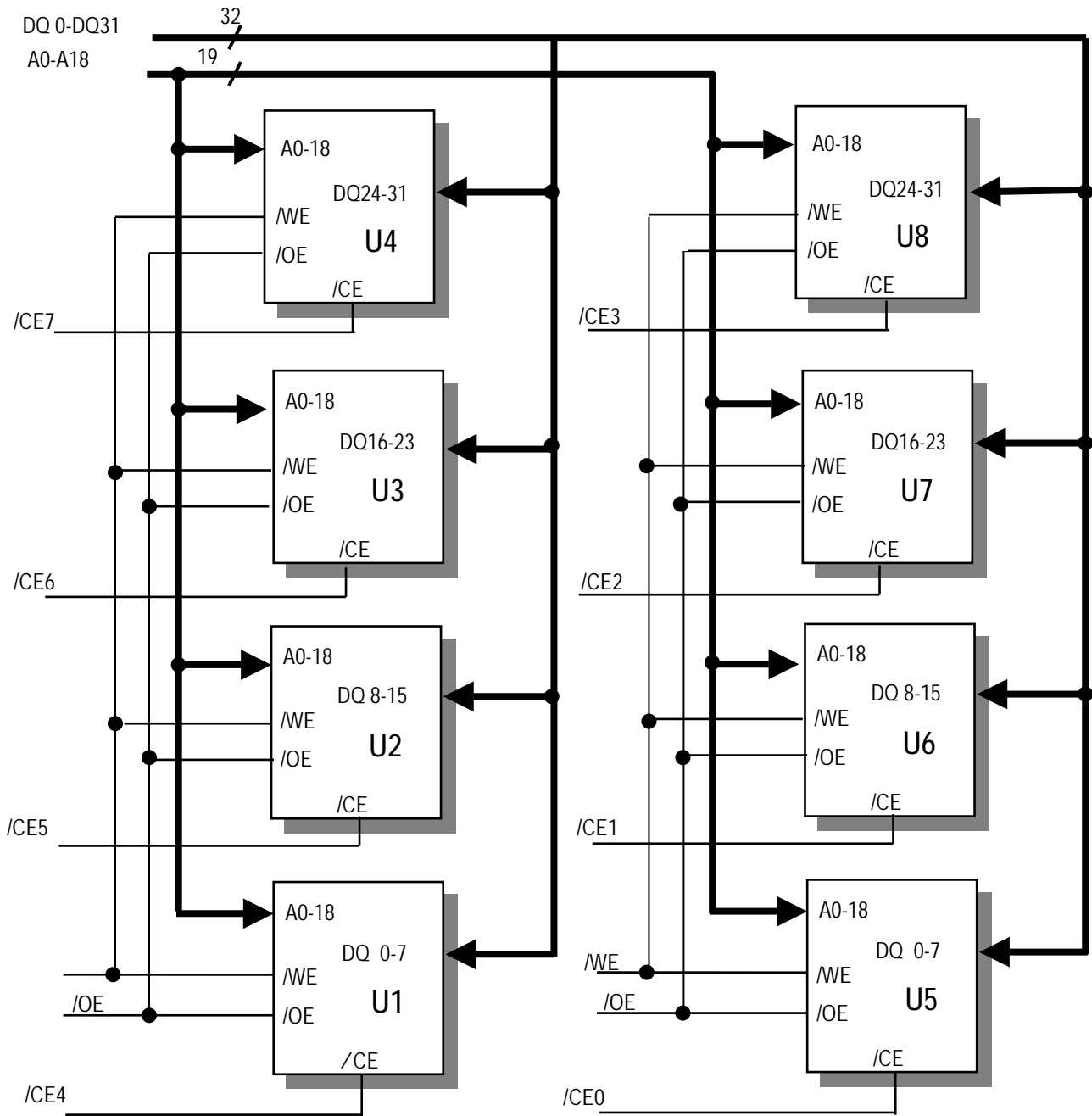
M
Z

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vcc	25	DQ13	49	DQ27
2	Vcc	26	DQ5	50	DQ19
3	Vss	27	DQ14	51	A3
4	Vss	28	DQ6	52	A10
5	Vss	29	DQ15	53	A4
6	Vss	30	DQ7	54	A11
7	Vss	31	/OE	55	A5
8	DQ0	32	/CE3	56	A12
9	DQ8	33	A15	57	Vcc
10	DQ1	34	A14	58	A13
11	DQ9	35	/CE6	59	A6
12	DQ2	36	/CE7	60	DQ20
13	DQ10	37	/CE4	61	DQ28
14	DQ3	38	/CE5	62	DQ21
15	DQ11	39	A17	63	DQ29
16	Vcc	40	A16	64	DQ22
17	A0	41	/CE2	65	DQ30
18	A7	42	Vss	66	DQ23
19	A1	43	DQ24	67	DQ31
20	A8	44	DQ16	68	Vss
21	A2	45	DQ25	69	A18
22	A9	46	DQ17	70	/WE
23	DQ12	47	DQ26	71	/CE1
24	DQ4	48	DQ18	72	/CE0

SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Q	ACTIVE
WRITE or ERASE	X	L	L	D	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to V _{SS}	V _{IN,OUT}	-0.5V to +7.0V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.5V to +7.0V
Power Dissipation	P _D	8W
Storage Temperature	T _{STG}	-65°C to +150°C
Operating Temperature	T _A	0°C to +70°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70 ° C)

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V _{CC}	4.5V	5.0V	5.5V
Ground	V _{SS}	0	0	0
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5V**
Input Low Voltage	V _{IL}	-0.5*	-	0.8V

* V_{IL}(Min.) = -2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

** V_{IH}(Min.) = V_{CC}+2.0V (Pulse Width ≤ 10ns) for I ≤ 20 mA

DC AND OPERATING CHARACTERISTICS (1)

(0°C ≤ T_A ≤ 70 °C ; V_{CC} = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V _{IN} = V _{SS} to V _{CC}	IL _I	-8	8	μA
Output Leakage Current	/CE=V _{IH} or /OE =V _{IH} or /WE=V _{IL} V _{OUT} =V _{SS} to V _{CC}	IL _O	-8	8	μA
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V

* V_{CC}=5.0V, Temp=25 °C

DC AND OPERATING CHARACTERISTICS (2)

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX		UNIT
			-55	-70	
Power Supply Current:Operating	$I_{IO}=0mA, /CE=V_{IL}, V_{IN}=V_{IL}$ or V_{IH}, Read	I_{CC}	80	80	mA
Power Supply Current:Standby	$/CE=V_{IH}, \text{Other inputs}=V_{IL}$ or V_{IH}	I_{SB}	24	24	mA
	$/CE \geq V_{CC}-0.2V, \text{Other inputs}=0 \sim V_{CC}$	I_{SB1}	640	640	μA

CAPACITANCE

DESCRIPTION	TEST CONDITIONS	SYMBOL	MAX	UNIT
Input /Output Capacitance	$V_{IO}=0V$	C_{IO}	64	pF
Input Capacitance	$V_{IN}=0V$	C_{IN}	80	pF

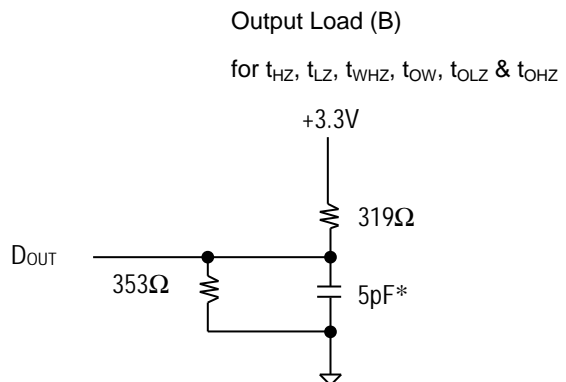
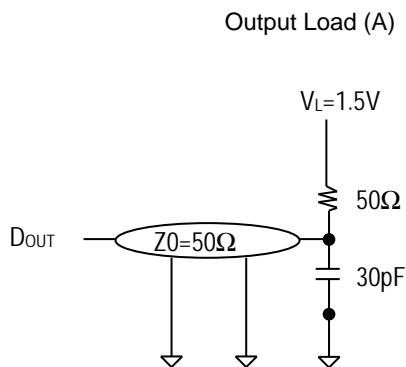
* NOTE : Capacitance is sampled and not 100% tested

AC CHARACTERISTICS ($0^{\circ}C \leq T_A \leq 70^{\circ}C$; $V_{CC} = 5V \pm 0.5V$, unless otherwise specified)

Test conditions

PARAMETER	VALUE
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=100pF + 1TTL$

* See test condition of DC and Operating characteristics



READ CYCLE

PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC}	55		70		ns
Address Access Time	t_{AA}		55		70	ns
Chip Select to Output	t_{CO}		55		70	ns
Output Enable to Output	t_{OE}		25		35	ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		ns

WRITE CYCLE

PARAMETER	SYMBOL	-55		-70		UNIT
		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{WC}	55		70		ns
Chip Select to End of Write	t_{CW}	45		60		ns
Address Set-up Time	t_{AS}	0		0		ns
Address Valid to End of Write	t_{AW}	45		60		ns
Write Pulse Width	t_{WP}	40		50		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
Data to Write Time Overlap	t_{DW}	25		30		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End of Write to Output Low-Z	t_{OW}	5		5		ns

TIMING DIAGRAMS

Please refer to timing diagram chart(II)

FUNCTIONAL DESCRIPTION

/CE	/WE	/OE	MODE	I/O PIN	SUPPLY CURRENT
H	X*	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

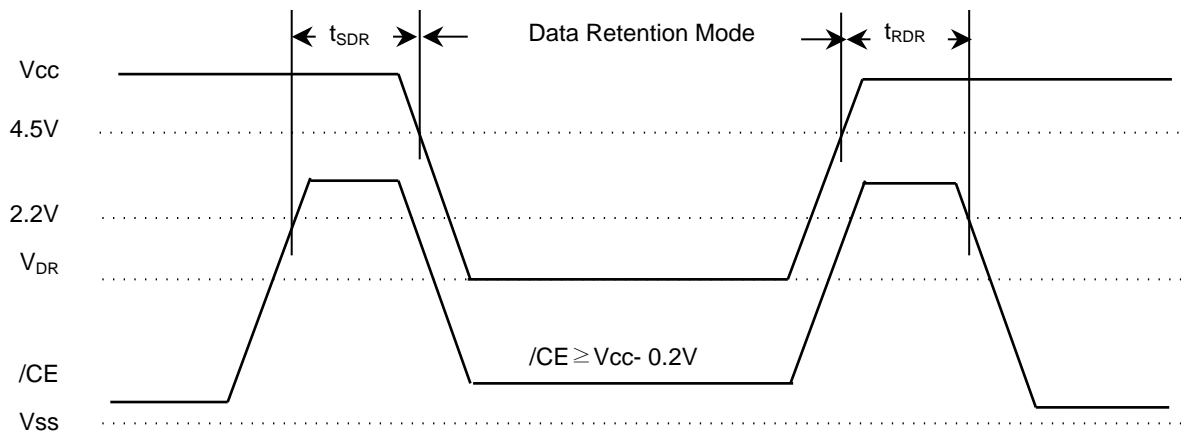
Note: X means Don't Care

DATA RETENTION CHARACTERISTICS* (TA = 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
V_{CC} for Data Retention	V_{DR}	$/CE \geq V_{CC}-0.2V$	2	5.5	V
Data Retention Current	I_{DR}	$V_{CC}=3.0V, /CE \geq V_{CC}-0.2V$ $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	-	320	μA
Data Retention Set-up Time	t_{SDR}	See Data Retention	0	-	ns
Recovery Time	t_{RDR}	Wave forms(below)	5	-	ns

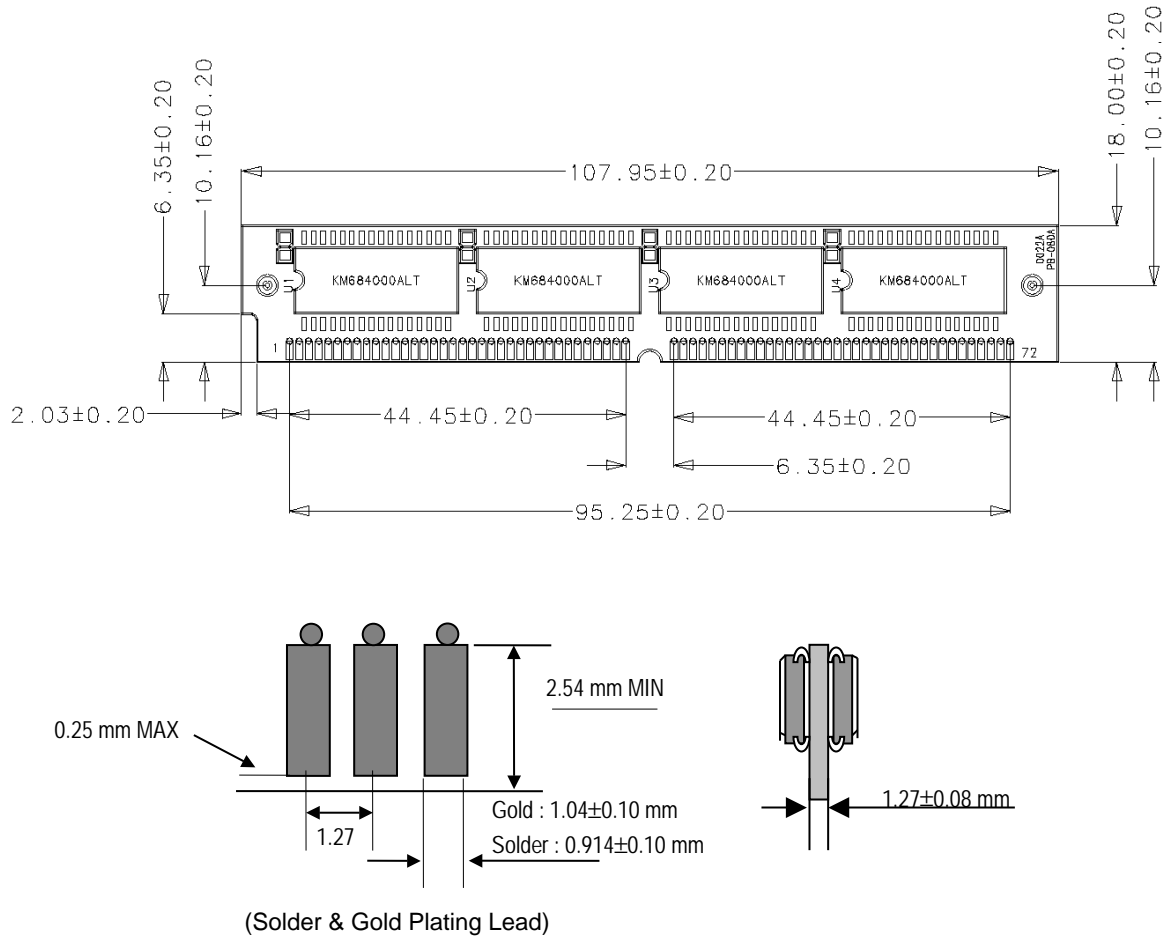
* L-Version Only

DATA RETENTION WAVEFORM 1 (/CE Controlled)



PACKAGING DIMENSIONS

SIMM Design



ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HMS1M32M8LA-55	4MByte	1Mx32bit	72Pin-SIMM	8EA	5.0V	55ns
HMS1M32M8LA-70	4MByte	1Mx32bit	72Pin--SIMM	8EA	5.0V	70ns