FR-V™ *Family*

FR400 Series
VLIW Embedded Microprocessor

MB93423

■ DESCRIPTION

This specifications describe the implementation of the MB93423, incorporating a processor core (FR403-SoC) designed for embedded applications, which is based on a VLIW (Very Long Instruction Word) architecture (the FR-V architecture) .

This processor can issue the integer operation instruction, media instruction, and branch instruction, up to two instructions, in units called the "VLIW instruction" on a cycle-by-cycle basis.

Also, the processor incorporates the following resources : SDRAM controller (SDRAMC) , interrupt controller (IRC) , DMA controller (DMAC) , asynchronous transfer module (UART) , timer/counter (TIMER/COUNTER) , general-purpose I/O (GPIO) , video display controller (VDC) , video capture controller (VCC) , scaler, audio interface, serial interface (I^{2}C*) , USB interface, and memory stick interface. The VLIW instruction and these resources achieve an excellent cost performance in a complex of high-performance general-purpose processing and media processing, such as multifunction printers, digital cameras, and portable information terminals.

* : Purchase of Fujitsu I^{2}C components conveys a license under the Philips I^{2}C Patent Rights to use, these components in an I^{2}C system provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

■ PACKAGE

337-ball plastic PFBGA

(BGA-337P-M03)

FUJITSU
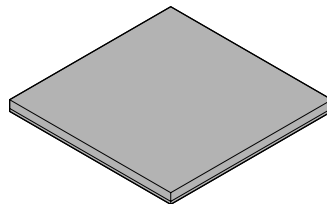
MB93423

■ FEATURES

CPU Core
- 2-way 240 MHz or 266 MHz VLIW Processor Core
- Peak Performance
  480 MIPS (Integer operation performance) at 240 MHz
  1920 MOPS + 240 MIPS (media operation performance) at 240 MHz
  532 MIPS (Integer operation performance) at 266 MHz
  2128 MOPS + 266 MIPS (media operation performance) at 266 MHz
- 64 32-bit registers (32GR + 32FR)

Cache
- Instruction cache : 8 Kbyte (2way) , line size 32 byte
- Data cache : 8 Kbyte (2way) , line size 32 byte
- Cache line replace algorithm : LRU
- Instruction cache preload instruction (ICPL) , Data cache preload instruction (DCPL) support
- Cache lock support of both instruction and data for each line
- Non-blocking cache (data cache)
- Store buffer : 64-byte (data cache)

SDRAM Interface
- SDRAM in accordance with the PC100 or PC133 standard can be connected.
- Changeable 32/16-bit data bus
- Four CS (2 support only registered-DIMM)

DMAC
- Four channels (dual address mode)
- Data transfer size is selected from 1, 2, 4 and 32 bytes
- Maximum 4G-byte data transfer
- Priority is fixed or round robin.
- Four external request demand signals (DREQ#[3 : 0])
- 32-byte FIFO is built in each DMA channel
- Address update
  Select from increment, holding and decrement
- Circular addressing
  When the transfer byte count reaches the specified value, the transfer address is reset to the initial value and transfer continues.
  When internal request is specified while circular addressing is specified, the internal request will be ignored.
- 2D addressing
  When the transfer byte count reaches the specified value, "initial value + AP value" is set to transfer address and transfer continues.

Local Bus Interface
- 24-bit address / 16-bit or 8-bit data
- Can directly connect SRAM, ROM, etc.
- The programmable address decoder is built into, and maximum 4 chip select pins are equipped with.
- Can specify the bus width by each chip select. (Select from 16 bits or 8 bits)
- The programmable wait state generator is built into.

Interrupt Controller
- Maximum 4 external interrupt factors are input (IRQ3-0) / 11 internal interrupt factors are input : (DMA = 4, Timer = 3, UART = 2 and Error response = 2)
- Interrupt factors are mapped in 15 levels of interrupt requests.

(Continued)

UART
- 16550 subsets
- 2 channels of UART are equipped.
- Prescaler to generate baud rate is built into.
- Modem control signal external pins (RTS#/CTS#) are equipped (to only channel 0) .

Timer
- 8254 subsets
- 3 channels of 16-bit timer are equipped.
- Supports mode 0 (terminal count interrupt) , mode 2 (rate generator) , mode 4 (software trigger strobe) , and mode 5 (hardware trigger strobe) . No other mode is supported.
- Supports the binary counter. (BCD counter is not supported.)
- One channel of prescaler is mounted on the former steps in the timer block.

GPIO
- 16-bit general-purpose I/O port is equipped with. (Other peripheral functions and I/O pins are shared.)

JTAG
- Supports the IEEE1149.1 JTAG Boundary Scan function.

Video Output
- Progressive or interlaced scan method
- 320 to 1920 pixels horizontal resolution, 240 to 1200 pixels vertical resolution
- Supports 4 : 2 : 2 YCbCr   8 bits (Time-shared; CbYCrY; conforms to BT.656) , 4 : 2 : 2 YCbCr 16 bits (Cb and Cr output time-shared; Cb precedes Cr) , 4 : 2 : 2 YCbCr 24 bits (Cb and Cr output concurrently; 2 clocks output) , 4 : 4 : 4 RGB   24 bits for output format
- Supports 4 : 2 : 2 YCbCr 16 bits (Cb and Cr time-shared; Cb precedes Cr) , 4 : 4 : 4 RGB 24 bits (No filler byte) for input data
- Hardware cursor : 1 piece (32 × 32; 2 colors + transparent color)

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- Hardware cursor : 1 piece (32 × 32; 2 colors + transparent color)

Scaler
- Maximum pixel count in horizontal direction for input image size   : 1920 (brightness component)
- Maximum pixel count in vertical direction for input image size   : 768
- Maximum pixel count in horizontal direction for output image size : 360 (brightness component)
- Maximum pixel count in vertical direction for output image size   : 288

Audio Output
- This is an interface supporting the 3-wire serial (supporting I^2S which is MSB-justified) and the PCM highway.
- Maximum : 32 bits/sample (I^2S which is MSB-justified)
- Fixed at 8 bits/sample (PCM highway)
- Depends on frequency of supplied clock (Either of the following is supplied from outside : 256/384/512/768 fs.)

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(Continued)

Audio Input
- This is an interface supporting the 3-wire serial (supporting I^{2}S which is MSB-justified) and the PCM highway. Input data is arranged in the front-justified format (starting with MSB) .
- Maximum : 32 bits/sample (I^{2}S which is MSB-justified)
- Fixed at 8 bits/sample (PCM highway)
- Depends on frequency of supplied clock (Either of the following is supplied from outside : 256/384/512/768 fs.)

USB
- Compliant with USB 2.0 FS function.
- V bus and isochronous transfer are not supported.

I²C
- Standard mode (100 Kbps) and the Fast mode (400 Kbps) are supported.

Memory Stick
- Compliant with Memory Stick Standard Format Specification ver1.4.
- Memory Stick Pro and Memory Stick Duo are supported. (However, excluded Magic Gate function.)

AV GPIO
- 32 bits (correspond to the pins shared with other functions.)

Clock Control
- Clock supply can be turned on/off for each unit.

Recommended Operation Condition
- Power supply voltage : Externally 3.3 V $\pm$ 0.15 V, Internally 1.8 V $\pm$ 0.1 V
- Operating temperature range from 0 °C to + 70 °C

■ PRODUCT LINEUP

These specifications have indicated two kinds of following products.

Part number	MB93423BGL-GE1	MB93423-26BGL-GE1
Core frequency	240 MHz	266 MHz
Voltage external / internal	3.3 V $\pm$ 0.15 V / 1.8 V $\pm$ 0.1 V	3.3 V $\pm$ 0.15 V / 1.8 V $\pm$ 0.1V
Ta	0 °C to + 70 °C	
Package (Code)	PFBGA337 (BGA-337P-M03)	
Thermal resistance Rth (ja)	45 °C/W (0 m/s)	
Remarks	Lead-free Solder ball	

■ PIN ASSIGNMENT

49 pins from K10 to T16 are for thermal. Connect them to VSS.

(TOP-VIEW)

INDEX

(BGA-337P-M03)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A	1	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73
B	2	97	184	183	182	181	180	179	178	177	176	175	174	173	172	171	170	169	168	167	166	165	164	163	72
C	3	98	185	264	263	262	261	260	259	258	257	256	255	254	253	252	251	250	249	248	247	246	245	162	71
D	4	99	186	265	336	335	334	333	332	331	330	329	328	327	326	325	324	323	322	321	320	319	244	161	70
E	5	100	187	266	337																	318	243	160	69
F	6	101	188	267																		317	242	159	68
G	7	102	189	268																		316	241	158	67
H	8	103	190	269																		315	240	157	66
J	9	104	191	270																		314	239	156	65
K	10	105	192	271						VSS	VSS	VSS	VSS	VSS	VSS	VSS						313	238	155	64
L	11	106	193	272						VSS	VSS	VSS	VSS	VSS	VSS	VSS						312	237	154	63
M	12	107	194	273						VSS	VSS	VSS	VSS	VSS	VSS	VSS						311	236	153	62
N	13	108	195	274						VSS	VSS	VSS	VSS	VSS	VSS	VSS						310	235	152	61
P	14	109	196	275						VSS	VSS	VSS	VSS	VSS	VSS	VSS						309	234	151	60
R	15	110	197	276						VSS	VSS	VSS	VSS	VSS	VSS	VSS						308	233	150	59
T	16	111	198	277						VSS	VSS	VSS	VSS	VSS	VSS	VSS						307	232	149	58
U	17	112	199	278																		306	231	148	57
V	18	113	200	279																		305	230	147	56
W	19	114	201	280																		304	229	146	55
Y	20	115	202	281																		303	228	145	54
AA	21	116	203	282																		302	227	144	53
AB	22	117	204	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	226	143	52
AC	23	118	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	142	51
AD	24	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	50
AE	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49

Pin No.	Position	Pin Name	Pin No.	Position	Pin Name	Pin No.	Position	Pin Name
1	A1	N.C.	36	AE12	VSS	71	C25	DDQ[31]
2	B1	CLKIN	37	AE13	N.C.	72	B25	VDE
3	C1	VDDP	38	AE14	N.C.	73	A25	N.C.
4	D1	BS#	39	AE15	TOUT[0]	74	A24	MTESTMODE
5	E1	WE#	40	AE16	RXD[1]	75	A23	RSTOUT#
6	F1	CS#[3]	41	AE17	IRQ#[1]	76	A22	CMODE[1]
7	G1	VCR[7]	42	AE18	VDE	77	A21	TESTMODE
8	H1	VCR[3]	43	AE19	DREQ#[3]	78	A20	TDO
9	J1	VSS	44	AE20	VDD	79	A19	TDI
10	K1	VCB[5]	45	AE21	VDE	80	A18	ERST#
11	L1	VCB[1]	46	AE22	DDQ[5]	81	A17	VDD
12	M1	VSS	47	AE23	DDQ[6]	82	A16	D[19]
13	N1	VDE	48	AE24	VDE	83	A15	D[21]
14	P1	VDD	49	AE25	N.C.	84	A14	D[25]
15	R1	VCG[3]	50	AD25	DDQ[9]	85	A13	D[26]
16	T1	VCG[1]	51	AC25	DDQ[8]	86	A12	D[28]
17	U1	VDR[5]	52	AB25	DDQ[12]	87	A11	BE[0]
18	V1	VSS	53	AA25	DDQ[14]	88	A10	VDE
19	W1	VDB[7]	54	Y25	DDQM[0]	89	A9	A[4]
20	Y1	VDB[3]	55	W25	VDE	90	A8	VSS
21	AA1	VDB[0]	56	V25	DRAS#	91	A7	A[10]
22	AB1	VSS	57	U25	VSS	92	A6	A[14]
23	AC1	VDCLKOUT	58	T25	DA[5]	93	A5	A[16]
24	AD1	VDE	59	R25	VSS	94	A4	A[20]
25	AE1	N.C.	60	P25	DCLKFB	95	A3	A[21]
26	AE2	VDG[5]	61	N25	VSS	96	A2	VDE
27	AE3	VDG[6]	62	M25	DA[10]	97	B2	A[22]
28	AE4	VDE	63	L25	DBA[1]	98	C2	A[23]
29	AE5	VDG[1]	64	K25	VSS	99	D2	VSS
30	AE6	SDI	65	J25	DDQ[16]	100	E2	RDY#
31	AE7	VSS	66	H25	VDE	101	F2	VSS
32	AE8	LRCKI	67	G25	DDQ[22]	102	G2	CS#[1]
33	AE9	SDA[0]	68	F25	VDE	103	H2	VCR[5]
34	AE10	MSINS	69	E25	DDQ[28]	104	J2	VCR[1]
35	AE11	MSDIO[2]	70	D25	DDQ[30]	105	K2	VCB[7]

(Continued)

Pin No.	Position	Pin Name	Pin No.	Position	Pin Name	Pin No.	Position	Pin Name
106	L2	VCB[3]	141	AD24	DDQ[7]	176	B11	BE[2]
107	M2	VCHSYNC	142	AC24	DDQ[11]	177	B10	A[2]
108	N2	VSS	143	AB24	DDQ[10]	178	B9	A[6]
109	P2	VCG[5]	144	AA24	VSS	179	B8	A[8]
110	R2	VSS	145	Y24	DWE#	180	B7	A[12]
111	T2	VDR[7]	146	W24	DCS#[0]	181	B6	VDD
112	U2	VDR[3]	147	V24	DCS#[2]	182	B5	A[18]
113	V2	VDR[1]	148	U24	DA[1]	183	B4	A[19]
114	W2	VDB[5]	149	T24	DA[3]	184	B3	N.C.
115	Y2	VDB[2]	150	R24	DA[7]	185	C3	VDD
116	AA2	VDVSYNC	151	P24	VSS	186	D3	N.C.
117	AB2	ENABLE	152	N24	DA[8]	187	E3	RD#
118	AC2	N.C.	153	M24	VDE	188	F3	ERR#
119	AD2	VDG[7]	154	L24	DA[12]	189	G3	DIR
120	AD3	VDG[3]	155	K24	DDQM[2]	190	H3	VDE
121	AD4	VDG[4]	156	J24	DDQ[18]	191	J3	VCR[6]
122	AD5	VSS	157	H24	DDQ[20]	192	K3	VCR[0]
123	AD6	TOPFIELD	158	G24	DDQ[24]	193	L3	VCB[4]
124	AD7	BCKI	159	F24	DDQ[26]	194	M3	VCVSYNC
125	AD8	LRCKO	160	E24	VSS	195	N3	VCDCLKIN
126	AD9	SCL[0]	161	D24	VDD	196	P3	VCG[4]
127	AD10	VDE	162	C24	N.C.	197	R3	VCG[0]
128	AD11	MSDIO	163	B24	CPUHOLD	198	T3	VDR[2]
129	AD12	VDD	164	B23	CMODE[2]	199	U3	VDB[6]
130	AD13	N.C.	165	B22	CMODE[3]	200	V3	VDHSYNC
131	AD14	USCKI	166	B21	RAMBOOT#	201	W3	VDR[0]
132	AD15	RXD[0]	167	B20	TDC	202	Y3	VDD
133	AD16	TXD[1]	168	B19	TCK	203	AA3	N.C.
134	AD17	IRQ#[3]	169	B18	ECV	204	AB3	VSS
135	AD18	DREQ#[1]	170	B17	VSS	205	AC3	VDD
136	AD19	MSDIRP#	171	B16	D[17]	206	AC4	N.C.
137	AD20	DDQ[1]	172	B15	VSS	207	AC5	VDG[2]
138	AD21	DDQ[3]	173	B14	D[23]	208	AC6	VDG[0]
139	AD22	DDQ[4]	174	B13	VSS	209	AC7	VDPCLKIN
140	AD23	N.C.	175	B12	D[30]	210	AC8	DISABLE

(Continued)

Pin No.	Position	Pin Name	Pin No.	Position	Pin Name	Pin No.	Position	Pin Name
211	AC9	SDO	246	C22	N.C.	281	Y4	VDB[4]
212	AC10	SDA[1]	247	C21	PRST#	282	AA4	VDB[1]
213	AC11	MSBS	248	C20	VSS	283	AB4	VSS
214	AC12	MSCLK	249	C19	CMODE[0]	284	AB5	FSCKI
215	AC13	UDP	250	C18	VDE	285	AB6	VDDE
216	AC14	VSS	251	C17	VSS	286	AB7	BCKO
217	AC15	TXD[0]	252	C16	ECLK	287	AB8	SCL[1]
218	AC16	VSS	253	C15	D[20]	288	AB9	VSS
219	AC17	MSDIRS#	254	C14	D[24]	289	AB10	XMSCKI
220	AC18	DDQ[2]	255	C13	D[27]	290	AB11	MSDIO[1]
221	AC19	DREQ#[2]	256	C12	D[31]	291	AB12	MSDIO[3]
222	AC20	DDQ[0]	257	C11	BE[3]	292	AB13	UDM
223	AC21	N.C.	258	C10	A[7]	293	AB14	VDE
224	AC22	VSS	259	C9	A[11]	294	AB15	TOUT[1]
225	AC23	VDD	260	C8	A[17]	295	AB16	VDD
226	AB23	N.C.	261	C7	A[9]	296	AB17	IRQ#[0]
227	AA23	VDE	262	C6	VSS	297	AB18	IRQ#[2]
228	Y23	DDQ[15]	263	C5	N.C.	298	AB19	DREQ#[0]
229	W23	DDQ[13]	264	C4	VSS	299	AB20	VSS
230	V23	DCAS#	265	D4	VSS	300	AB21	VSS
231	U23	DCS#[1]	266	E4	CS#[2]	301	AB22	VSS
232	T23	DA[2]	267	F4	CS#[0]	302	AA22	DDQM[1]
233	R23	DA[6]	268	G4	VCR[4]	303	Y22	VSS
234	P23	VDDP	269	H4	VCR[2]	304	W22	DCS#[3]
235	N23	VDD	270	J4	VDE	305	V22	DA[0]
236	M23	DBA[0]	271	K4	VCB[6]	306	U22	VDE
237	L23	VDE	272	L4	VCB[2]	307	T22	DA[4]
238	K23	VSS	273	M4	VCB[0]	308	R22	VDE
239	J23	DDQ[23]	274	N4	VCG[7]	309	P22	DCLK
240	H23	DDQ[29]	275	P4	VCG[6]	310	N22	DA[9]
241	G23	DDQ[21]	276	R4	VCG[2]	311	M22	VSS
242	F23	DDQ[25]	277	T4	VDE	312	L22	DA[11]
243	E23	N.C.	278	U4	VDR[6]	313	K22	DCKE
244	D23	VSS	279	V4	VDR[4]	314	J22	DDQM[3]
245	C23	VDD	280	W4	VDE	315	H22	DDQ[17]

(Continued)

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(Continued)

Pin No.	Position	Pin Name
316	G22	DDQ[19]
317	F22	VSS
318	E22	DDQ[27]
319	D22	VSS
320	D21	TRST#
321	D20	TMS
322	D19	HRST#
323	D18	ED
324	D17	D[16]
325	D16	D[18]
326	D15	VDE
327	D14	D[22]
328	D13	VDE
329	D12	D[29]
330	D11	BE[1]
331	D10	VSS
332	D9	A[3]
333	D8	A[5]
334	D7	VDE
335	D6	A[13]
336	D5	A[15]
337	E5	N.C.

Note : The power supply pins are classified as follow.
      VDD pin is the internal power supply pin.
      VDDP pin is the analog power supply pin of PLL.
      VDE pin is the external power supply pin.
      VSS pin is the ground pin (0 V).

■ PIN DESCRIPTION

1.   Format

This section explains the pin functions of this LSI chip.

The pin function list is in the format shown below :

Pin No.	Pin Name	Direction	Type	BS	Description

Pin Name : Indicates name of external pin

If several signals share the same pin, the names are separated by a slash (/) .

"XX#" in a signal line name indicates "active low".

Direction : Indicates I/O of signal with reference to LSI chip

Input   : Indicates pin for input signal to LSI chip

Output   : Indicates pin for output signal from LSI chip

Input/output   : Indicates pin for bidirectional signal

Type : Indicates pin input/output circuit type

Each symbol has the following meaning :

Symbol	Description
SD	Solid Drive Type of output pin. Normal output. The pin never becomes high impedance.
TS	Tri-State Type of output or input/output pin. The pin may become high impedance.
PU	Pull-up Type of input pin or input/output pin. A pull-up resistor is built into the circuit.
PD	Pull-down Type of input pin or input/output pin. A pull-down resistor is built into the circuit.
OD	Open-drain Type of output pin. The pin may become high impedance.

Note : Explains outline of function and relationship with other pins

BS : Indicates whether the target of boundary-scan or not.

2. Local Bus Interface

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
98 97 95 94 183 182 260 93 336 92 335 180 259 91 261 179 258 178 333 89 332 177	A[23] A[22] A[21] A[20] A[19] A[18] A[17] A[16] A[15] A[14] A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2]	Output	TS	Yes	Address A word address is output. When the local bus is released, these pins become input.
256 175 329 86 255 85 84 254 173 327 83 253 82 325 171 324	D[31] D[30] D[29] D[28] D[27] D[26] D[25] D[24] D[23] D[22] D[21] D[20] D[19] D[18] D[17] D[16]	Input/ output	TS	Yes	Data This is the data bus; D[31] is MSB. When connecting a 16-bit slave device to this signal, connect it to D[31 : 16] (higher) . When connecting a 8-bit slave device to this signal, connect it to D[31 : 24] (higher) .
4	BS#	Output	TS	Yes	Bus Cycle Start This is asserted for only 1 CLKIN cycle at the beginning of a bus cycle to indicate the start of the bus cycle. This pin becomes input when the bus is released.

(Continued)

Pin No.	Pin Name	Direction	Type	BS	Description
PFBGA					

87
330
176
257
	BE[0] / BE#[0]
	BE[1] / BE#[1]
	BE[2] / BE#[2]
	BE[3] / BE#[3]
		Output	TS	Yes	Byte Enable
					This specifies byte lanes for data transfer.
					BE [0 : 1] is used to access a 16-bit slave device; the correspondence between this signal and the data bus is shown below :
					    BE[0] → D [31 : 24] (higher byte)
					    BE[1] → D [23 : 16] (lower byte)
					    BE [2] is used to access halfword address.
					    BE [2] → A[1]
					BE [0] is used to access a 8-bit slave device; the correspondence between this signal and the data bus is shown below :
					    BE [0] → D [31 : 24]
					    BE [2 : 3] is used to access byte address.
					    BE [2] → A[1]
					    BE [3] → A[0]
					These pins become input when the bus is released. To access this LSI as the slave device when this bus is released, it must be treated as a 32-bit slave device.

187	RD#	Output	TS	Yes	Read This pin is asserted during the second or later CLKIN cycles of read local bus cycles. This pin becomes high impedance when the local bus is released.
5	WE#	Output	TS	Yes	Write Enable This pin is asserted during a write cycles. It can be used as a strobe pulse for write data. This pin becomes high impedance when the bus is released.
189	DIR	Output	TS	Yes	Direction Indicates transfer direction of D[31 : 16] pins L : input (read) , H : output (write) This pin becomes input when the bus is released. This LSI determines whether the local bus cycles that performed by external devices are reads or writes, based on the DIR signal. This pin becomes "L" when bus is idle.
100	RDY#	Input	—	Yes	Ready The bus cycle completion notice from the slave device is input. The value of RDY# is reflected to LCR0.RC at power-on reset.
188	ERR#	Input	—	Yes	Error This is sampled at the end of the bus cycle; the error notice is input from the slave device to this pin. This pin is ignored when the bus is released.

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(Continued)

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
6 266 102 267	CS#[3] CS#[2] CS#[1] CS#[0]	Output	SD	Yes	Chip Select This signal selects slave device under control of MB93423. The corresponding address is determined from the settings of the programmable address decoder built into MB93423. Connect the boot ROM to the CS#[0] pin.

3. SDRAM Interface

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
304 147 231 146	DCS#[3] DCS#[2] DCS#[1] DCS#[0]	Output	SD	Yes	Chip select This signal is determined by programmable address de-coder build into MB93423. DCS#[2] and DCS#[3] are used to specify 168pin registered DIMM.
63 236	DBA[1] DBA[0]	Output	SD	Yes	Bank Address The bank address is output.
154 312 62 310 152 150 233 58 307 149 232 148 305	DA[12] DA[11] DA[10] DA[9] DA[8] DA[7] DA[6] DA[5] DA[4] DA[3] DA[2] DA[1] DA[0]	Output	SD	Yes	Multiplexed Address The address multiplexed for SDRAM is output.
56	DRAS#	Output	SD	Yes	Row Address Strobe Row Address Strobe signal to SDRAM.
230	DCAS#	Output	SD	Yes	Column Address Strobe Column Address Strobe signal to SDRAM.
145	DWE#	Output	SD	Yes	Write Enable Write Enable signal to SDRAM.
313	DCKE	Output	SD	Yes	Clock Enable Clock Enable signal to SDRAM.

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314
	DDQM[0]
	DDQM[1]
	DDQM[2]
	DDQM[3]
		Output	SD	Yes	Data Mask
					These pins (signal) are combined with other signals to specify the byte lane to be written.
					At read, all the bits are driven Low.
					The correspondence between this signal and the data bus when connecting 32-bit SDRAM is shown below :
					    DDQM[0] → DDQ[31 : 24]
					    DDQM[1] → DDQ[23 : 16]
					    DDQM[2] → DDQ[15 : 8]
					    DDQM[3] → DDQ[7 : 0]
					The correspondence between this signal and the data bus when connecting 16-bit SDRAM is shown below :
					    DDQM[0] → DDQ[31 : 24]
					    DDQM[1] → DDQ[23 : 16]

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Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
71 70 240 69 318 159 242 158 239 67 241 157 316 156 315 65 228 53 229 52 142 143 50 51 141 47 46 139 138 220 137 222	DDQ [31] DDQ[30] DDQ[29] DDQ[28] DDQ[27] DDQ[26] DDQ[25] DDQ[24] DDQ[23] DDQ[22] DDQ[21] DDQ[20] DDQ[19] DDQ[18] DDQ[17] DDQ[16] DDQ[15] DDQ[14] DDQ[13] DDQ[12] DDQ[11] DDQ[10] DDQ[9] DDQ[8] DDQ[7] DDQ[6] DDQ[5] DDQ[4] DDQ[3] DDQ[2] DDQ[1] DDQ[0]	Input/ output	TS	Yes	Data This signal is connected to the SDRAM data bus; DDQ[31] is MSB. When connecting 16-bit SDRAM, connect it to DDQ[31 : 16] When the bus width is set to 16 bits by DCFG.BW, DDQ[15 : 0] is fixed to the high-impedance state.
309	DCLK	Output	SD	Yes	SDRAM Clock This is the output of the clock signal supplied to SDRAM. The output is supplied when MB93423 is in self refresh mode. The output is halted while the PLL is halted. The output is also halted during a power-on reset.
60	DCLKFB	Input	—	Yes	Feedback for SDRAM Clock To adjust the DCLK phase, feedback input to the PLL built into this LSI chip.

4. General Peripheral Resource

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
296 41 297 134	IRQ#[0] / PP[0] IRQ#[1] / PP[1] IRQ#[2] / PP[2] IRQ#[3] / PP[3]	Input/ output	TS	Yes	Interrupt Request 0 to 3/ GPIO 0 to 3 These pins are used as the interrupt input and as a general-purpose I/O port (GPIO) .
39	TOUT[0] / GATE[0] / PP[4]	Input/ output	TS	Yes	Timer ch 0 Output/Timer ch 0 Gate/GPIO 4 This pin is used as the timer ch 0 pin and as a general-purpose I/O port (GPIO) .
294	TOUT[1] / GATE[1] / PP[5]	Input/ output	TS	Yes	Timer ch 1 Output/Timer ch 1 Gate/GPIO 5 This pin is used as the timer ch 1 pin and as a general-purpose I/O port (GPIO) .
132	RXD[0] / PP[6]	Input/ output	TS	Yes	UART ch 0 Receive Data/GPIO 6 This pin is used as the UART ch 0 receive data and as a general-purpose I/O port (GPIO) .
217	TXD[0] / PP[7]	Input/ output	TS	Yes	UART ch 0 Transmit Data/GPIO 7 This pin is used as the UART ch 0 transmit data and as a general-purpose I/O port (GPIO) .
219	MSDIRS# / PP[8]	Input/ output	TS	Yes	Memory Stick Direction Serial/GPIO 8 **[Memory stick licensees]** Customers are advised to consult with our sales representatives, if you use MS interface. **[Non-licensees]** This pin is used as a general-purpose input port (GPIO) . The output mode must not be used.
136	MSDIRP# / PP[9]	Input/ output	TS	Yes	Memory Stick Direction Parallel/GPIO 9 **[Memory stick licensees]** Customers are advised to consult with our sales representatives, if you use MS interface. **[Non-licensees]** This pin is used as a general-purpose input port (GPIO) . The output mode must not be used.
40	RXD[1] / PP[10]	Input/ output	TS	Yes	UART ch 1 Receive Data/GPIO 10 This pin is used as the UART ch 1 receive data and as a general-purpose I/O port (GPIO) .
133	TXD[1] / PP[11]	Input/ output	TS	Yes	UART ch 1 Transmit Data/GPIO 11 This pin is used as the UART ch 1 transmit data and as a general-purpose I/O port (GPIO) .
298	DREQ#[0] / PP[12]	Input/ output	TS	Yes	DMAC ch 0 Request/GPIO 12 This pin is used as the UART ch 0 transfer request and as a general-purpose I/O port (GPIO) .
135	DREQ#[1] / PP[15]	Input/ output	TS	Yes	DMAC ch 1 Transfer Request/GPIO 15 This pin is used as the DMAC ch 1 transfer request and as a general-purpose I/O port (GPIO) .

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Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
221	DREQ#[2] / PP[18]	Input/ output	TS	Yes	DMAC ch 2 Transfer Request/GPIO 18 This pin is used as the DMAC ch 2 transfer request and as a general-purpose I/O port (GPIO) .
43	DREQ#[3] / PP[19]	Input/ output	TS	Yes	DMAC ch 3 Transfer Request/GPIO 19 This pin is used as the DMAC ch 3 transfer request and as a general-purpose I/O port (GPIO) .

5. ICE Interface

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
80	ERST#	Input	PD	Yes	ESB Reset For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
322	HRST#	Input	—	Yes	Hard Reset This is the reset input dedicated to the ICE. This pin function is equivalent to reset by the debugger hardware reset command. Reset by this pin will not reset debug related settings, so this pin can be used for debugging the reset sequence, etc. When using this pin, connect the reset switch signal to this pin; when not using this pin, fix it to the High level.
169	ECV	Input	PU	Yes	ESB Command Valid Command valid signal for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
323	ED	Input/ output	TS PD	Yes	ESB Data Data I/O signal for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
252	ECLK	Output	TS	Yes	ESB Clock Clock signal (output) for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.

6. Reset

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
247	PRST#	Input	—	Yes	Power-on Reset This is the level trigger initialization signal. Apply the Low level to this pin for 16 CLKIN clock cycles or more. This pin is used to cause a power-on reset; it initializes all registers and sequencers except cache and GR/FR.
75	RSTOUT#	Output	SD	Yes	Reset Output This signal is asserted during a power-on reset. The power-on reset operation is prolonged in the LSI until the oscillation stabilization wait time for the internal PLL has elapsed. Consequently, use this signal to detect that the power-on reset operation has been completed in the LSI. When HRST# is asserted when the ICE used, this signal (RSTOUT#) is asserted as in the power-on reset.

166	RAMBOOT#	Input	—	Yes	RAM Boot
					A software reset can be caused by applying a Low level to this pin.
					When this signal and the PRST# pin are asserted simultaneously, the power-on reset operation is prefered.
					At a power-on reset, the level input to this pin is reflected in the SA bit of the register HSR0, and then the reset vector address is determined as shown below based on the SA bit.
					   Low level : 0x00000000
					   High level : 0xFF000000

7. CPU Status

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
163	CPUHOLD	Output	SD	Yes	CPU Hold Signal indicating that CPU stops in hold state

8. Clocks

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
2	CLKIN	Input	—	Yes	Clock Input External clock are input to this pin.
165 164 76 249	CMODE[3] CMODE[2] CMODE[1] CMODE[0]	Input	—	Yes	Clock Mode Determines operating frequency of each section in LSI

9. JTAG

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
79	TDI	Input	PU	No	Test Data Input This is the test data input pin. This signal is sampled on the rising edge of TCK.
78	TDO	Output	TS	No	Test Data Output This is the test data output pin. This drives active when the ATP controller is the Shift-IR or Shift-DR state. This signal changes on the falling edge of TCK.
321	TMS	Input	PU	No	Test Mode Select This is the test mode select pin. This signal is sampled on the rising edge of TCK.
168	TCK	Input	PU	No	Test ClocK This is the test clock pin.
320	TRST#	Input	PU	No	Test Reset This is the TAP controller asynchronous reset. This pin initializes the TAP controller When not using the JTAG function on the printed circuit board, input the same signal as PRST# to this pin.

10. Test

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
77	TESTMODE	Input	—	Yes	Test Mode Input Fix it at Low level on the printed circuit board.
167	TDC	Input	—	No	Test Input Fix it at Low level on the printed circuit board.
74	MTESTMODE	Input	—	Yes	MTEST Mode Input Fix it at Low level on the printed circuit board.

11. VDC

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
111 278 17 279 112 198 113 201	VDR[7]/VDCR[7]/AVPP[23] VDR[6]/VDCR[6]/AVPP[22] VDR[5]/VDCR[5]/AVPP[21] VDR[4]/VDCR[4]/AVPP[20] VDR[3]/VDCR[3]/AVPP[19] VDR[2]/VDCR[2]/AVPP[18] VDR[1]/VDCR[1]/AVPP[17] VDR[0]/VDCR[0]/AVPP[16]	Input/ output	TS	Yes	R component output / C_r component output / GPIO These pins are display video data output pins. In the RGB mode, the red component is output. In the 24-bit YC mode, C_r component is output. These pins are shared by GPIO unit and set as GPIO input setting after reset.
119 27 26 121 120 207 29 208	VDG[7]/VDY[7]/VDX[7] VDG[6]/VDY[6]/VDX[6] VDG[5]/VDY[5]/VDX[5] VDG[4]/VDY[4]/VDX[4] VDG[3]/VDY[3]/VDX[3] VDG[2]/VDY[2]/VDX[2] VDG[1]/VDY[1]/VDX[1] VDG[0]/VDY[0]/VDX[0]	Output	TS	Yes	G Component output / Y component output / YC multiplexed output These pins are display video data output pins. In the RGB mode, the green component is output. Also, in the 16-bit or 24-bit YC mode, the Y component is output. When 8-bit YC mode is selected, multiplexed pixel data is output.
19 199 114 281 20 115 282 21	VDB[7]/VDCX[7]/VDCB[7]/AVPP[39] VDB[6]/VDCX[6]/VDCB[6]/AVPP[38] VDB[5]/VDCX[5]/VDCB[5]/AVPP[37] VDB[4]/VDCX[4]/VDCB[4]/AVPP[36] VDB[3]/VDCX[3]/VDCB[3]/AVPP[35] VDB[2]/VDCX[2]/VDCB[2]/AVPP[34] VDB[1]/VDCX[1]/VDCB[1]/AVPP[33] VDB[0]/VDCX[0]/VDCB[0]/AVPP[32]	Input/ output	TS	Yes	B Component output / C component output / C_b component output / GPIO These pins are display video data output pins. In the RGB mode, the blue component is output. In the 16-bit YC mode, the C_b component and the C_r component are time-shared and output. Moreover, in the 24-bit YC mode, C_b component is output. These pins are shared by GPIO unit and set as GPIO input setting after reset.
200	VDHSYNC/VDHSYNC#	Output	TS	Yes	Horizontal synchronous signal output This pin is for display synchronous signal output. Its polarity is programmable.
116	VDVSYNC/VDVSYNC#	Output	TS	Yes	Vertical synchronous signal output This pin is for display synchronous signal output. Its polarity is programmable.
209	VDPCLKIN	Input	—	Yes	Display pixel clock input This pin inputs a basic clock to generate display pixel clock output.
23	VDCLKOUT	Output	TS	Yes	Display pixel clock output Pixel data is output in synchronization with this signal.

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Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
117	ENABLE/ENABLE#	Output	TS	Yes	Pixel output enable This signal shows that effective pixel data is output. Its polarity is programmable.
123	TOPFIELD/TOPFIELD#	Output	TS	Yes	Top field This pin shows that the top field is displayed. Its polarity is programmable.
210	DISABLE	Input	—	Yes	Video output disable When this signal is asserted, VDR[7 : 0] / VDCR[7 : 0], VDG[7 : 0] / VDY[7 : 0], VDB[7 : 0] / VDCX[7 : 0] / VDCB[7 : 0], VDHSYNC, VDVSYNC and VDCLKOUT go in to the high impedance state. However, ordinary operation continues inside.

12. VCC

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
7 191 103 268 8 269 104 192	VCR[7]/VCCR[7]/AVPP[15] VCR[6]/VCCR[6]/AVPP[14] VCR[5]/VCCR[5]/AVPP[13] VCR[4]/VCCR[4]/AVPP[12] VCR[3]/VCCR[3]/AVPP[11] VCR[2]/VCCR[2]/AVPP[10] VCR[1]/VCCR[1]/AVPP[9] VCR[0]/VCCR[0]/AVPP[8]	Input/output	TS	Yes	R component input / C_r component input / GPIO These pins are capture video data input pins. In the RGB mode, the red component is input. In the 24-bit YC mode, C_r component is input. These pins are shared by GPIO and set as GPIO input setting after reset.
274 275 109 196 15 276 16 197	VCG[7]/VCY[7]/VCX[7] VCG[6]/VCY[6]/VCX[6] VCG[5]/VCY[5]/VCX[5] VCG[4]/VCY[4]/VCX[4] VCG[3]/VCY[3]/VCX[3] VCG[2]/VCY[2]/VCX[2] VCG[1]/VCY[1]/VCX[1] VCG[0]/VCY[0]/VCX[0]	Input	—	Yes	G Component input / Y component input / YC multiplexed input These pins are capture video data input pins. In the RGB mode, the green component is input. Also, in the 24-bit YC mode, the Y component is input. When 8-bit YC mode is selected, multiplexed pixel data is output.
105 271 10 193 106 272 11 273	VCB[7]/VCCX[7]/VCCB[7]/AVPP[31] VCB[6]/VCCX[6]/VCCB[6]/AVPP[30] VCB[5]/VCCX[5]/VCCB[5]/AVPP[29] VCB[4]/VCCX[4]/VCCB[4]/AVPP[28] VCB[3]/VCCX[3]/VCCB[3]/AVPP[27 VCB[2]/VCCX[2]/VCCB[2]/AVPP[26] VCB[1]/VCCX[1]/VCCB[1]/AVPP[25] VCB[0]/VCCX[0]/VCCB[0]/AVPP[24]	Input/output	TS	Yes	B component input / C component input / C_b component input / GPIO These pins are capture video data input pins. In the RGB mode, the blue component is input. Also, in the 16-bit YC mode, C_b component and C_r component are time-shared and input. Moreover, in the 24-bit YC mode, C_b component is input. These pins are shared by GPIO unit and set as GPIO input setting after reset.
107	VCHSYNC/VCHSYNC#	Input	—	Yes	Horizontal synchronous signal input This pin is a capture synchronous signal input pin. Its polarity is programmable.
194	VCVSYNC/VCVSYNC#	Input	—	Yes	Vertical synchronous signal input This pin is a capture synchronous signal input pin. Its polarity is programmable.
195	VCDCLKIN	Input	—	Yes	Capture pixel clock input This pin is a sampling clock for capture. The edge to use is programmable.

13. Audio

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
211	SDO/DX	Output	TS	Yes	Audio data output Audio serial data is output.
125	LRCKO/FS0	Output	SD	Yes	LR clock output / CH0 synchronous signal When performing output that supports I^{2}S or MSB-justified, the LR clock is output. Also, when performing output that supports the PCM highway, the CH0 synchronous signal (FS0) is output.
286	BCKO/MCLK	Output	SD	Yes	Bit clock output This pin is an audio signal I/O bit clock output pin. I/O that supports the PCM highway always operates in the master mode. Consequently, MCLK that is output by MB93423 is used for audio signal input.
30	SDI/DR	Input	—	Yes	Audio data input This pin is for audio serial data input.
32	LRCKI/FS1	Input/ output	TS	Yes	LR clock input / CH1 synchronous signal output When performing input that supports I^{2}S or MSB-justified, this pin becomes an LR clock input pin. Also, when performing I/O that supports the PCM highway, the CH1 synchronous signal (FS1) is output.
124	BCKI	Input	—	Yes	Bit clock input This pin inputs bit clocks used for audio signal input that supports I^{2}S or MSB-justified.
284	FSCKI	Input	—	Yes	Basic clock input for audio output This pin inputs the basic clocks (256/384/512/756 fs) for generating bit clocks and LR clocks of audio signal output that supports I^{2}S or MSB-justified and for generating MCLK, FS0, and FS1 of audio signal output that supports the PCM highway.

14. USB/USB-Host

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
215	UDP	Input/ output	TS	No	USB D+ signal This pin is for differential signal (+) of USB function
292	UDM	Input/ output	TS	No	USB D− signal This pin is for differential signal (−) of USB function
131	USCKI	Input	—	Yes	USB clock input This pin inputs 48 MHz clock that is required by USB interface.

15. I²C

Pin No.	Pin Name	Direction	Type	BS	Description
PFBGA					
287 126	SCL[1] SCL[0]	Input/ output	OD	No	I²C clock These pins are used for a clock signal of the I²C bus. SCL[0] corresponds to I²C channel 0; SCL[1] corresponds to I²C channel 1.
212 33	SDA[1] SDA[0]	Input/ output	OD	No	I²C data These pins are used for data signals for the I²C bus. SDA[0] corresponds to I²C channel 0; SDA[1] corresponds to I²C channel 1.

Note : An I/O driver of I²C for MB93423 omits output through rate control. For this reason, the output through rate standard in the Fast mode (400 Kbps) of the I²C bus is not satisfied.
Since the standard for the Standard mode (100 Kbps) of the I²C bus is satisfied, it is connectable with the chip which is supporting Standard mode in the Standard mode.
If it is connection with the chip of Standard mode down compatible, connection in the Fast mode is also possible.

16. MS

Pin No. PFBGA	Pin Name	Direction	Type	BS	Description
289	XMSCKI	Input	—	Yes	Memory stick clock input **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** This pin should be pulled up on a board.
213	MSBS	Output	SD	Yes	Memory stick bus state signal **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** This pin should be open state on a board.
214	MSCLK	Output	SD	Yes	Memory stick clock output **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** This pin should be open state on a board.
128	MSDIO/MSDIO[0]	Input/ output	PD	Yes	Memory stick serial data signal **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** This pin should be open state on a board.
291 35 290	MSDIO[3] MSDIO[2] MSDIO[1]	Input/ output	PD	Yes	Memory stick serial data signal **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** These pins should be open state on a board.
34	MSINS	Input	—	Yes	Memory stick insert detection signal **[Memory stick licensees]** Customers are advised to consult with our sales repre-sentatives, if you use MS interface. **[Non-licensees]** This pin should be open state on a board.

■ PIN STATE

Initial value : Indicates pin state immediately after power-on reset. The meaning of each symbol is given below :

Symbol	Meaning
H	Indicates high level
L	Indicates low level
HiZ	Indicates high-impedance state
X	Indicates either high level or low level

Pin Name	Initial State	Core Sleep Mode	Bus Sleep Mode	PLL Operation Mode	PLL Stop Mode
A[23 : 2]	HiZ	Operation	X	X	X
D[31 : 16]	HiZ	Operation	HiZ	HiZ	HiZ
BE[0 : 3]/BE#[0 : 3]	HiZ	Operation	X	X	X
BS# , RD# , WE#	HiZ	Operation	H	H	H
DIR	HiZ	Operation	X	X	X
RDY#	—	Operation	HiZ	HiZ	HiZ
ERR#	—	—	—	—	—
CS#[3 : 0]	H	Operation	H	H	H
DCS#[3 : 0]	H	Operation	L	L	L
DBA[1 : 0]	L	Operation	X	X	X
DA[12 : 0]	X	Operation	X	X	X
DRAS# , DCAS#	H	Operation	L	L	L
DWE#	H	Operation	H	H	H
DCKE	H	Operation	L	L	L
DDQM[0 : 3]	H	Operation	H	H	H
DDQ[31 : 0]	HiZ	Operation	HiZ	HiZ	HiZ
DCLK	L	Operation	Operation	Operation	L
DCLKFB	—	—	—	—	—
IRQ#[0 : 3]/PP[0 : 3]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TOUT[0]/GATE[0]/PP[4]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TOUT[1]/GATE[1]/PP[5]	HiZ	Operation	Operation	X or HiZ	X or HiZ
RXD[0]/PP[6]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TXD[0]/PP[7]	HiZ	Operation	Operation	X or HiZ	X or HiZ
MSDIRS#/PP[8]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
MSDIRP#/PP[9]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
RXD[1]/PP[10]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TXD[1]/PP[11]	HiZ	Operation	Operation	X or HiZ	X or HiZ

(Continued)

Pin Name	Initial State	Core Sleep Mode	Bus Sleep Mode	PLL Operation Mode	PLL Stop Mode
DREQ#[0]/PP[12]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[1]/PP[15]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[2]/PP[18]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[3]/PP[19]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
ERST# , HRST#	—	—	—	—	—
ECV	—	—	—	—	—
ED	HiZ	HiZ	HiZ	HiZ	HiZ
ECLK	L	L	L	L	L
PRST#	—	—	—	—	—
RSTOUT#	L	Operation	Operation	Operation	Operation
RAMBOOT#	—	—	—	—	—
CPUHOLD	L	X	X	X	X
CLKIN	—	—	—	—	—
CMODE[3 : 0]	—	—	—	—	—
TDI	—	—	—	—	—
TDO	HiZ	HiZ	HiZ	HiZ	HiZ
TMS , TCK , TRST#	—	—	—	—	—
TESTMODE , TDC , MTESTMODE	—	—	—	—	—
VDR[7 : 0]/VDCR[7 : 0]/ AVPP[23 : 16]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VDG[7 : 0]/VDY[7 : 0]/VDX[7 : 0]	—	Operation	X	X	X
VDB[7 : 0]/VDCX[7 : 0]/ VDCB[7 : 0]/AVPP[39 : 32]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VDHSYNC/VDHSYNC#	—	Operation	X	X	X
VDVSYNC/VDVSYNC#	—	Operation	X	X	X
VDPCLKIN	—	—	—	—	—
VDCLKOUT	—	Operation	Operation	Operation	Operation
ENABLE/ENABLE#	—	Operation	X	X	X
TOPFIELD/TOPFIELD#	—	Operation	X	X	X
DISABLE	—	—	—	—	—
VCR[7 : 0]/VCCR[7 : 0]/ AVPP[15 : 8]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VCG[7 : 0]/VCY[7 : 0]/VCX[7 : 0]	—	—	—	—	—
VCB[7 : 0]/VCCX[7 : 0]/ VCCB[7 : 0]/AVPP[31 : 24]	—	Operation	X or HiZ	X or HiZ	X or HiZ

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Pin Name	Initial State	Core Sleep Mode	Bus Sleep Mode	PLL Operation Mode	PLL Stop Mode
VCHSYNC/VCHSYNC#	—	—	—	—	—
VCVSYNC/VCVSYNC#	—	—	—	—	—
VCDCLKIN	—	—	—	—	—
SDO/DX	—	Operation	X	X	X
LRCKO/FS0	—	Operation	Operation	Operation	Operation
BCKO/MCLK	—	Operation	Operation	Operation	Operation
SDI/DR	—	—	—	—	—
LRCKI/FS1	—	Operation	X or HiZ	X or HiZ	X or HiZ
BCKI	—	—	—	—	—
FSCKI	—	—	—	—	—
UDP	—	Operation	HiZ	HiZ	HiZ
UDM	—	Operation	HiZ	HiZ	HiZ
USCKI	—	—	—	—	—
SCL[1 : 0]	—	HiZ	HiZ	HiZ	HiZ
SDA[1 : 0]	—	HiZ	HiZ	HiZ	HiZ
XMSCKI	—	—	—	—	—
MSBS	—	Operation	X or HiZ	X or HiZ	X or HiZ
MSCLK	—	Operation	Operation	Operation	Operation
MSDIO/MSDIO[0]	—	Operation	X or HiZ	X or HiZ	X or HiZ
MSDIO[3 : 1]	—	Operation	X or HiZ	X or HiZ	X or HiZ
MSINS	—	—	—	—	—

■ HANDLING DEVICES

● Preventing latch-up

MB93423 may suffer latch-up under the following conditions :

- ● A voltage higher than V_{DE} or lower than V_{SS} is applied to an input or output pin.
- ● A voltage higher than the rated voltage is applied between VDE pin and VSS pin.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (V_{DD}) to exceed the digital power-supply voltage.

● Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

● Power supply pins

In products with multiple VDE, VDD or VSS pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect VDE, VDD and VSS pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between VDE, VDD and VSS pins near the device.

● Pull-up/down resistors

The MB93423 does not support internal pull-up/down resistors (except PU/PD Pin Type) . Use external compo-nents where needed.

● N.C. Pin

The N.C. (internally connected) pin must be opened for use.

MB93423

■ BLOCK DIAGRAM
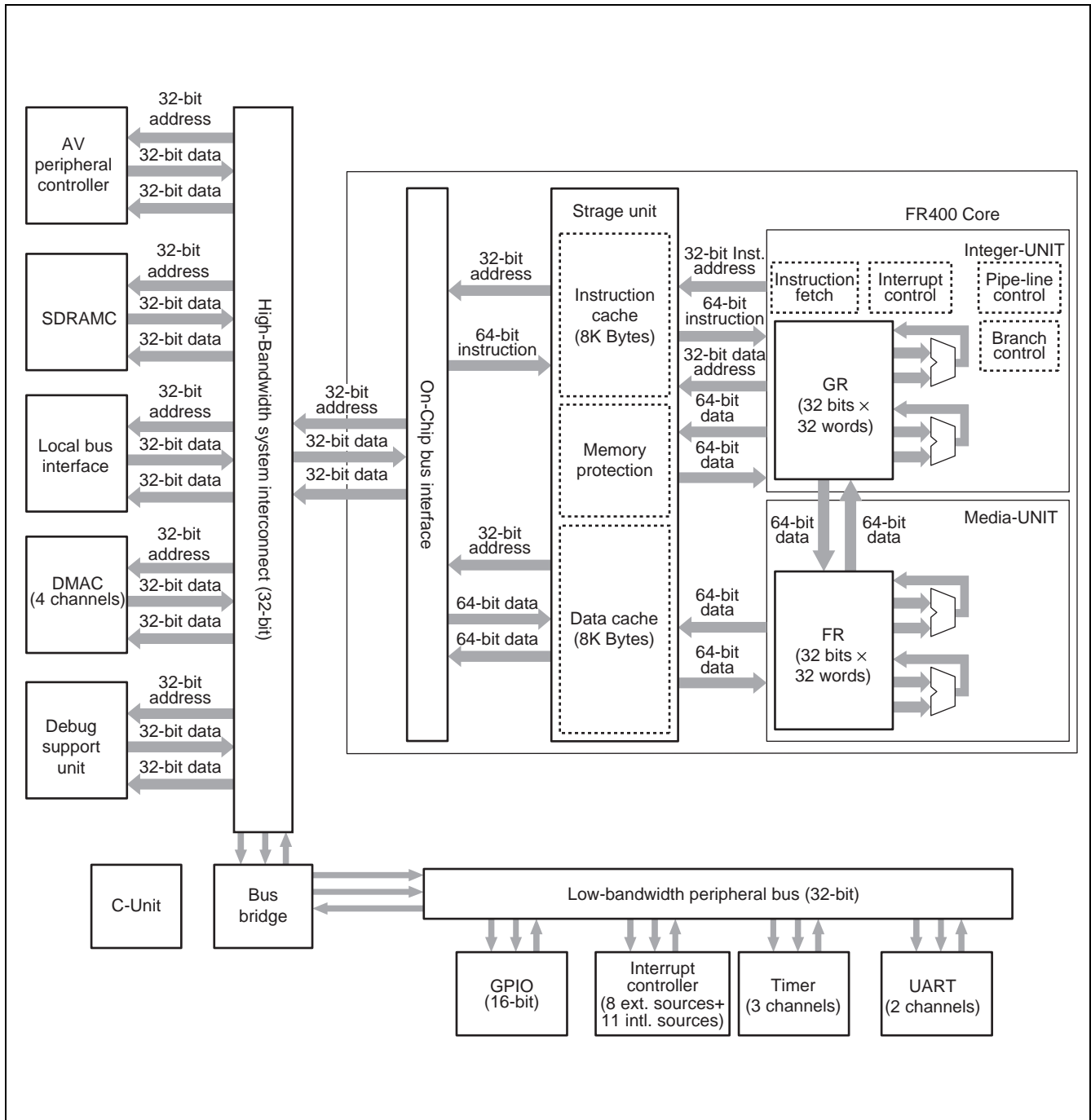
■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage (External) *	V_{DE}	$V_{SS} - 0.5$	$V_{SS} + 4.0$	V
Power supply voltage (Internal) *	V_{DD}	$V_{SS} - 0.5$	$V_{SS} + 2.5$	V
Power supply voltage (PLL) *	V_{DDP}	$V_{SS} - 0.5$	$V_{SS} + 2.5$	V
Input voltage*	V_I	$V_{SS} - 0.5$	$V_{DE} + 0.5\ (\leq 4.0)$	V
Storage temperature	T_{STG}	-55	$+ 125$	°C

* : The parameter is based on $V_{SS} = 0$ V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

$(V_{SS} = 0$ V$)$

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power supply voltage (External)	V_{DE}	240 MHz	3.15	3.3	3.45	V
		266 MHz	3.15	3.3	3.45	V
Power supply voltage (Internal)	V_{DD}	240 MHz	1.7	1.8	1.9	V
		266 MHz	1.7	1.8	1.9	V
Power supply voltage (PLL)	V_{DDP}	240 MHz	1.7	1.8	1.9	V
		266 MHz	1.7	1.8	1.9	V
"L" level input voltage	V_{IL}		-0.3	—	0.8	V
"H" level input voltage	V_{IH}		2.0	—	$V_{DE} + 0.3$	V
Operating temperature	Ta		0	$+ 25$	$+ 70$	°C

USB

(V$_{SS}$ = 0 V)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
"H" level input voltage	V$_{IHU}$	2.0	—	—	V
"L" level input voltage	V$_{ILU}$	—	—	0.8	V
Differential input sensitivity	V$_{DIU}$	0.2	—	—	V
Differential common mode range	V$_{CMU}$	0.8	—	2.5	V
"H" level output voltage	V$_{OHU}$	2.8	—	3.45	V
"L" level output voltage	V$_{OLU}$	0.0	—	0.3	V
Output signal crossover voltage	V$_{CRSU}$	1.3	—	2.0	V
Bus pull-up/down resistor on upstream port	Rpu*	1.425	—	1.575	kΩ
Termination voltage on upstream port pull-up	V$_{TERM}$	3.15	—	3.45	V

* : It is necessary to attach "Rpu" outside.
Notes on Board Wiring
- For connecting the power supply and ground (GND) , use multiple VDD and VSS pins. The system board based on the MB93423 must be a multi-layer board containing power supply (V$_{DD}$) and GND (V$_{SS}$) layers for stable power supply.
- Insert sufficient decoupling capacitors (condensers) near the MB93423. Changes to the output levels of many of the output pins on the MB93423 (in particular, those with large load capacitance) may cause variation in power supply.
- For those systems which run at a high frequency, low-inductance capacitors and mutual wiring are recommended. Inductance can be lowered by shortening the distance between the processor and decoupling capacitor

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Parameter	Symbol		Condition	Value			Unit
				Min	Typ	Max	
"L" level input voltage	V$_{IL}$		—	0	—	0.8	V
"H" level input voltage	V$_{IH}$		—	2.0	—	V$_{DE}$	V
"L" level output voltage	V$_{OL}$		I$_{OL}$ = 2 mA	0	—	0.4	V
"H" level output voltage	V$_{OH}$		I$_{OH}$ = −2 mA	V$_{DE}$ − 0.4	—	V$_{DE}$	V
Input leakage current	I$_{LI}$		V$_{IN}$ = 0 or V$_{DE}$	−5	—	5	μA
Tri-state output leakage current	I$_{LZ}$		V$_{OUT}$ = 0 or V$_{DE}$	−5	—	5	μA
Power supply current (V$_{DE}$)	I$_{DE}$	240 MHz	CMODE = 0x9, CLKIN = 60 MHz, (Dhrystone2.1) No Load	0	20	40	mA
		266 MHz	CMODE = 0x9, CLKIN = 66 MHz, (Dhrystone2.1) No Load	0	22	44	mA
Power supply current (V$_{DD}$)	I$_{DD}$	240 MHz	CMODE = 0x9, CLKIN = 60 MHz, (Dhrystone2.1)	—	300	360	mA
		266 MHz	CMODE = 0x9, CLKIN = 66 MHz, (Dhrystone2.1)	—	310	360	mA
Power supply current (V$_{DDP}$)	I$_{DDP}$	240 MHz	CMODE = 0x9, CLKIN = 60 MHz, (Dhrystone2.1)	—	3	6	mA
		266 MHz	CMODE = 0x9, CLKIN = 66 MHz, (Dhrystone2.1)	—	3	6	mA
At sleep power supply current	I$_{CORESLEEP}$	240 MHz	Core sleep mode, CLKIN = 60 MHz	—	40	—	mA
		266 MHz	Core sleep mode, CLKIN = 66 MHz	—	40	—	mA
	I$_{BUSSLEEP}$	240 MHz	Bus sleep mode, CLKIN = 60 MHz	—	25	—	mA
		266 MHz	Bus sleep mode, CLKIN = 66 MHz	—	25	—	mA
	I$_{PLLON}$	240 MHz	PLL On mode, CLKIN = 60 MHz	—	12	—	mA
		266 MHz	PLL On mode, CLKIN = 66 MHz	—	12	—	mA
	I$_{PLLOFF}$		PLL Stop mode, CLKIN = 0 MHz	—	0.5	—	mA
Capacity of pins	C$_{PIN}$		V$_{DE}$ = V$_{I}$ = 0, f = 1 MHz	—	—	16	pF

USB

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
"L" level output voltage	V$_{OL}$	I$_{OL}$ = 20 mA	0	—	0.4	V
"H" level output voltage	V$_{OH}$	I$_{OH}$ = −20 mA	V$_{DE}$ − 0.5	—	V$_{DE}$	V
"L" level output current	I$_{OL}$	V$_{OL}$ = 0.4 V	20	—	—	mA
"H" level output current	I$_{OH}$	V$_{OH}$ = V$_{DE}$ − 0.4 V	−20	—	—	mA
Output short-circuit current	I$_{OS}$	—	—	—	300	mA

4. AC Characteristics

(1) Local Bus Interface

$(V_{DE} = 3.3\ V \pm 0.15\ V,\ V_{DD} = V_{DDP} = 1.8\ V \pm 0.1\ V,\ V_{SS} = 0\ V,\ Ta = 0\ °C\ to\ +70\ °C)$

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
CLKIN input	CLKIN period (T_{CLKIN})		—	16.7*	30*	15*	30*	ns
	CLKIN high time		—	6.0	—	6.0	—	ns
	CLKIN low time		—	6.0	—	6.0	—	ns
	CLKIN rise time		—	—	1.0	—	1.0	ns
	CLKIN fall time		—	—	1.0	—	1.0	ns
Local-bus I/F output	A [23 : 2]	Output valid delay time	CLKIN rise	1.5	6.0	1.5	6.0	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	D [31 : 16]	Output valid delay time	CLKIN rise	1.5	6.0	1.5	6.0	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BE/BE# [0 : 3]	Output valid delay time	CLKIN rise	1.5	6.0	1.5	6.0	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BS#	Output valid delay time	CLKIN rise	1.5	6.0	1.5	6.0	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	RD#	Output valid delay time	CLKIN rise	1.5	6.0	1.5	6.0	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	WE#	Output valid delay time	CLKIN fall	1.0	7.0	1.0	7.0	ns
		Output hold time	CLKIN fall	1.0	—	1.0	—	ns
	DIR	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	RDY#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	CS# [3 : 0]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
Local-bus I/F input	A [23 : 2]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	D [31 : 16]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BE/BE# [0 : 3]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BS#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

* : Refer to "5. Clock Setting" for details.

(Continued)

(Continued)

$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \text{ °C to } + 70 \text{ °C})$

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Local-bus I/F input	DIR	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RDY#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	ERR#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted. Each voltage value is based on the GND ($V_{SS} = 0.0$ V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less. The external output load capacitance is 30 pF.
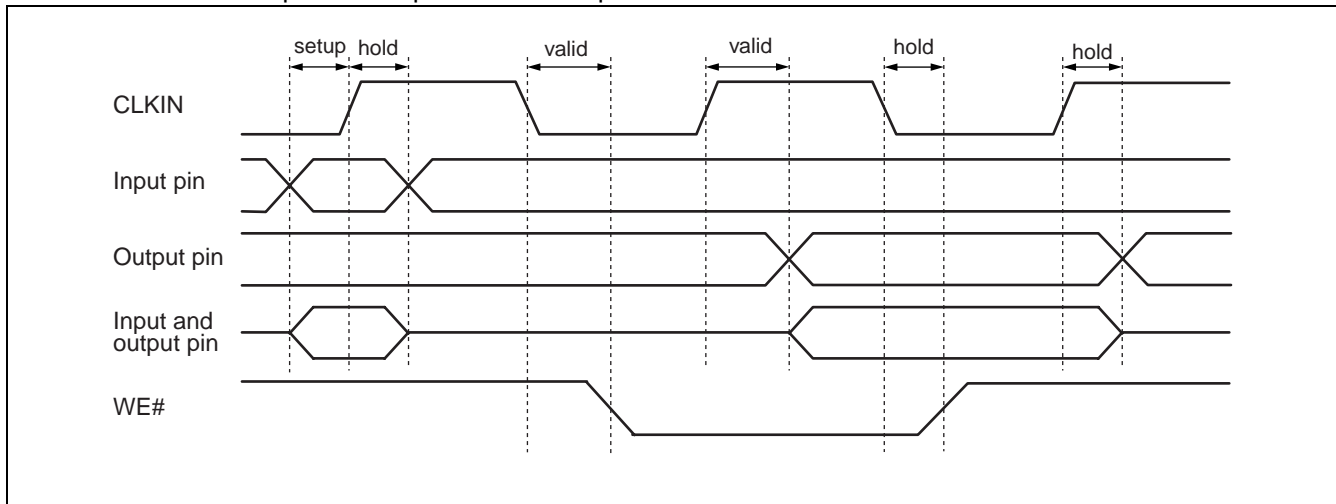
(2) SDRAM Interface

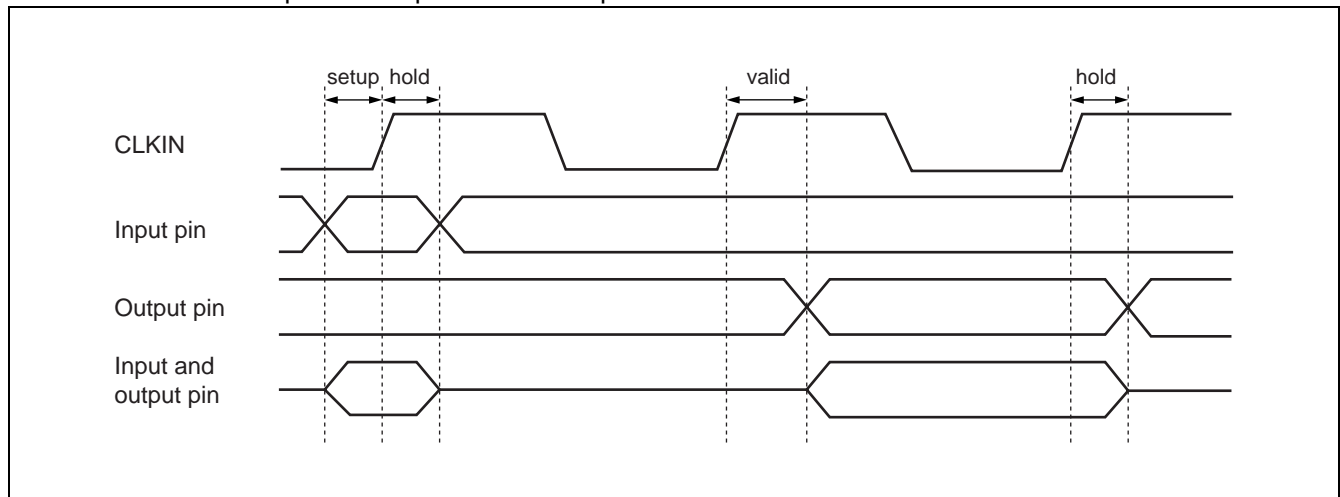$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \text{ °C to } + 70 \text{ °C})$

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
DCLKFB input	DCLKFB period (T_{DCLKFB})		—	8.3*	15*	7.5*	15*	ns
	DCLKFB high time		—	2.5	—	2.5	—	ns
	DCLKFB low time		—	2.5	—	2.5	—	ns
	DCLKFB rise time		—	—	1.0	—	1.0	ns
	DCLKFB fall time		—	—	1.0	—	1.0	ns
SDRAM I/F output	DCS# [3 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DBA [1 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DA [12 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DRAS#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DCAS#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DWE#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DCKE	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DDQM [0 : 3]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DDQ [31 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
		Output hold time	DCLKFB rise	1.0	—	1.0	—	ns
SDRAM I/F input	DDQ [31 : 0]	Input setup time	DCLKFB rise	1.0	—	1.0	—	ns
		Input hold time	DCLKFB rise	1.0	—	1.0	—	ns

* : This value is decided by CMODE.

Notes:
- Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
  Each voltage value is based on the GND ($V_{SS} = 0.0$ V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less unless otherwise noted.
  The external output load capacitance is 30 pF unless otherwise noted.
- The frequency of the input to DCLKFB and the output from DCLK is decided by the input frequency to CLKIN, and setup of a CMODE [3 : 0] pins. Refer to "5. Clock Setting" for details.
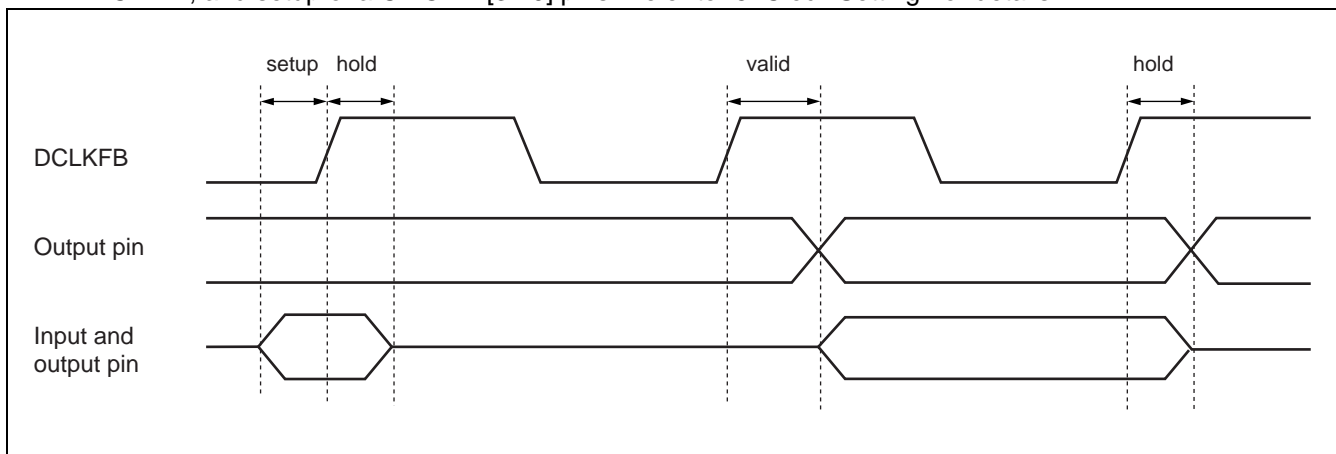
- This LSI outputs DCLK which is supplied to SDRAM as a clock. PLL is built into this LSI. Adjust the phase of DCLK so that the CLK pin of SDRAM and the internal phase in this LSI may be nearly equal. Therefore, when connecting, adjust the delay time of the feedback path from DCLK to DCLKFB, so that the phase of the clock input to DCLKFB which is the feedback signal to PLL, and the phase of the clock (wave shape on the reception edge of DCLK) input to CLK of SDRAM may be nearly equal.

(3) General Peripheral Resources

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Resources output	IRQ# [0 : 3]/ PP [0 : 3]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TOUT[0]/ GATE[0]/ PP[4]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TOUT[1]/ GATE[1]/ PP[5]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	RXD[0]/PP[6]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TXD[0]/PP[7]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	MSDIRS#/ PP[8]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	MSDIRP#/ PP[9]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	RXD[1]/PP[10]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TXD[1]/PP[11]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ# [0]/ PP[12]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ# [1]/ PP[15]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ#[2]/ PP[18]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ#[3]/ PP[19]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
Resources input	IRQ#[0 : 3] / PP [0 : 3]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TOUT[0]/ GATE[0]/ PP[4]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TOUT[1]/ GATE[1]/ PP[5]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

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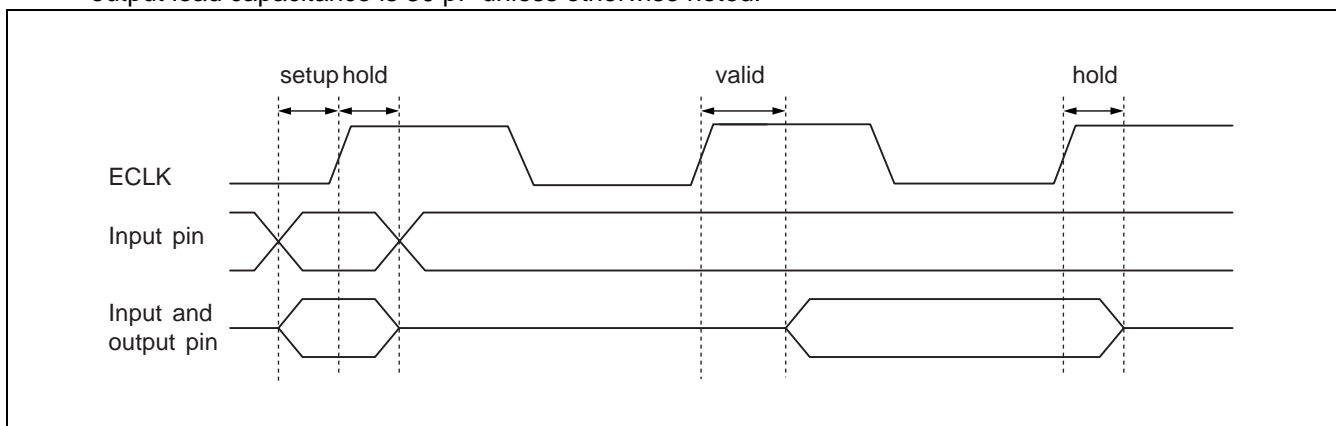
$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \text{ °C to } + 70 \text{ °C})$

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Resources input	RXD[0]/PP[6]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TXD[0]/PP[7]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	MSDIRS#/ PP[8]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	MSDIRP#/ PP[9]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RXD[1]/PP[10]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TXD[1]/PP[11]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[0]/ PP[12]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[1]/ PP[15]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[2]/ PP[18]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[3]/ PP[19]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
Each voltage value is based on the GND ($V_{SS} = 0$ V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less.
The external output load capacitance is 30 pF unless otherwise noted.

(4) ICE Interface

$(V_{DE} = 3.3\ V \pm 0.15\ V,\ V_{DD} = V_{DDP} = 1.8\ V \pm 0.1\ V,\ V_{SS} = 0\ V,\ Ta = 0\ °C\ to\ +70\ °C)$

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
ECLK output	ECLK output period		—	30	—	30	—	ns
	ECLK output high time		—	13.0	—	13.0	—	ns
	ECLK output low time		—	13.0	—	13.0	—	ns
	ECLK output rise time		—	—	2.0	—	2.0	ns
	ECLK output fall time		—	—	2.0	—	2.0	ns
ICE output	ED	Output valid delay time	ECLK rise	—	8.0	—	8.0	ns
		Output hold time	ECLK rise	0.0	—	0.0	—	ns
ICE input	ERST#	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns
	HRST#	Low pulse width	—	16	—	16	—	T_{CLKIN}
	ECV	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns
	ED	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted. Each voltage value is based on the GND ($V_{SS} = 0.0$ V) level. The timing measurement reference point is 1.5 V and the input level is 0.4 V to 2.4 V. The input rise time and fall time are 1.5 ns or less. The external output load capacitance is 30 pF unless otherwise noted.

(5) Reset

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Reset output	RSTOUT#	Output valid delay time	CLKIN rise	0	8.0	0	8.0	ns
Reset input	PRST#	Low pulse width	—	16	—	16	—	T$_{CLKIN}$
Boot input	RAMBOOT#	Low pulse width	—	16	—	16	—	T$_{CLKIN}$

(6) CPU Status

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
CPU output	CPUHOLD	Output valid delay time	CLKIN rise	0	8.0	0	8.0	ns

(7) Clocks

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Clock mode input	CMODE[3 : 0]	Input setup time	—	Must be fixed to "H" or "L"				—
		Input hold time	—	Must be fixed to "H" or "L"				—

(8) Test

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz		266 MHz		Unit
				Min	Max	Min	Max	
Test mode input	TESTMODE	Input setup time	—	Must be fixed to "L"				—
		Input hold time	—	Must be fixed to "L"				—
	TDC	Input setup time	—	Must be fixed to "L"				—
		Input hold time	—	Must be fixed to "L"				—
	MTESTMODE	Input setup time	—	Must be fixed to "L"				—
		Input hold time	—	Must be fixed to "L"				—

(9) Video Display Controller (VDC)

$(V_{DE} = 3.3$ V $\pm$ 0.15 V, $V_{DD} = V_{DDP} = 1.8$ V $\pm$ 0.1 V, $V_{SS} = 0$ V, Ta $= 0$ °C to $+ 70$ °C)

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
VDC clock input	VDPCLKIN period		—	12.5	50	ns
	VDPCLKIN high time		—	4.0	—	ns
	VDPCLKIN low time		—	4.0	—	ns
VDC I/F output	VDR [7 : 0]/VDCR [7 : 0]	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
		Output hold time	—	—	—	ns
	VDG [7 : 0]/VDY [7 : 0]/ VDX[7 : 0]	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
	VDB [7 : 0]/VDCX[7 : 0]/ VDCB [7 : 0]	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
		Output hold time	—	—	—	ns
	VDHSYNC/VDHSYNC#	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
	VDVSYNC/VDVSYNC#	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
	ENABLE/ENABLE#	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
	TOPFIELD/ TOPFIELD#	Output valid delay time	VDCLKOUT fall	−2.0	3.0	ns
	VDCLKOUT*	Output valid delay time	VDPCLKIN rise	7.0	14.0	ns
VDC I/F input	DISABLE	Input setup time	VDPCLKIN rise	2.5	—	ns
		Input hold time	VDPCLKIN rise	1.5	—	ns

* : The falling edge of VDCLKOUT is synchronous with respect to the rising edge of VDPCLKIN.

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
Each voltage value is based on the GND ($V_{SS} = 0.0$ V) level. The timing measurement reference point is 1.5 V and the input level is 0.4 V to 2.4 V.
The external output load capacitance is 30 pF.

(10) Video Capture Controller (VCC)

$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \,^{\circ}\text{C to } + 70 \,^{\circ}\text{C})$

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
VCC clock input	VCDCLKIN period		—	12.5	125	ns
	VCDCLKIN high time		—	4	—	ns
	VCDCLKIN low time		—	4	—	ns
VCC I/F input	VCR [7 : 0]/VCCR [7 : 0]	Input setup time	VCDCLKIN rise	2.5	—	ns
		Input hold time	VCDCLKIN rise	1.5	—	ns
	VCG[7 : 0]/VCY[7 : 0]/ VCX[7 : 0]	Input setup time	VCDCLKIN rise	2.5	—	ns
		Input hold time	VCDCLKIN rise	1.5	—	ns
	VCB[7 : 0]/VCCX[7 : 0]/ VCCB[7 : 0]	Input setup time	VCDCLKIN rise	2.5	—	ns
		Input hold time	VCDCLKIN rise	1.5	—	ns
	VCHSYNC/VCHSYNC#	Input setup time	VCDCLKIN rise	2.5	—	ns
		Input hold time	VCDCLKIN rise	1.5	—	ns
	VCVSYNC/VCVSYNC#	Input setup time	VCDCLKIN rise	2.5	—	ns
		Input hold time	VCDCLKIN rise	1.5	—	ns

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
Each voltage value is based on the GND ($V_{SS} = 0.0$ V) level. The timing measurement reference point is 1.5 V and the input level is 0.4 V to 2.4 V.
The external output load capacitance is 30 pF.

(11) Audio

(V$_{DE}$ = 3.3 V ± 0.15 V, V$_{DD}$ = V$_{DDP}$ = 1.8 V ± 0.1 V, V$_{SS}$ = 0 V, Ta = 0 °C to + 70 °C)

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
Audio clock input	FSCKI period		—	25	—	ns
	FSCKI high time		—	10.5	—	ns
	FSCKI low time		—	10.5	—	ns
	BCKI period		—	312.5	—	ns
	BCKI high time		—	130	—	ns
	BCKI low time		—	130	—	ns
Audio I/F output	SDO*	Output valid delay time	FSCKI rise	3.0	10.0	ns
	LRCKO*	Output valid delay time	FSCKI rise	3.0	10.0	ns
	BCKO*	Output valid delay time	FSCKI rise	3.0	10.0	ns
	LRCKI	Output valid delay time	FSCKI rise	3.0	10.0	ns
Audio I/F input	SDI	Input setup time	BCKI rise	50	—	ns
		Input hold time	BCKI rise	50	—	ns
	LRCKI	Input setup time	BCKI rise	50	—	ns
		Input hold time	BCKI rise	50	—	ns

* : LRCKO and SDO signals are generated with respect to the falling edge of BCKO (duty 50%) .

Note : Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
Each voltage value is based on the GND (V$_{SS}$ = 0.0 V) level. The timing measurement reference point is 1.5 V and the input level is 0.4 V to 2.4 V.
The external output load capacitance is 30 pF.

(12) USB Interface

$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \text{ °C to} + 70 \text{ °C})$

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
USB clock input	USCKI period		—	20	—	ns
	USCKI high time		—	8	—	ns
	USCKI low time		—	8	—	ns
USB driver	D+/D− rise time	T_{FR}	—	4	20	ns
	D+/D− fall time	T_{FF}	—	4	20	ns
	Differential rise and fall time matching		—	90	111.11	%
	Driver output resistance		—	3	19	Ω

Notes: • Frequency of USCKI is set to 48 MHz in order to carry out operation based on the standard of USB 2.0 FS. And it is necessary to put in a clock with a frequency accuracy of 2500 ppm.
• In order to fulfill the standard of USB 2.0 FS, it is necessary to add 25 to 30 Ω in-series resistance outside.
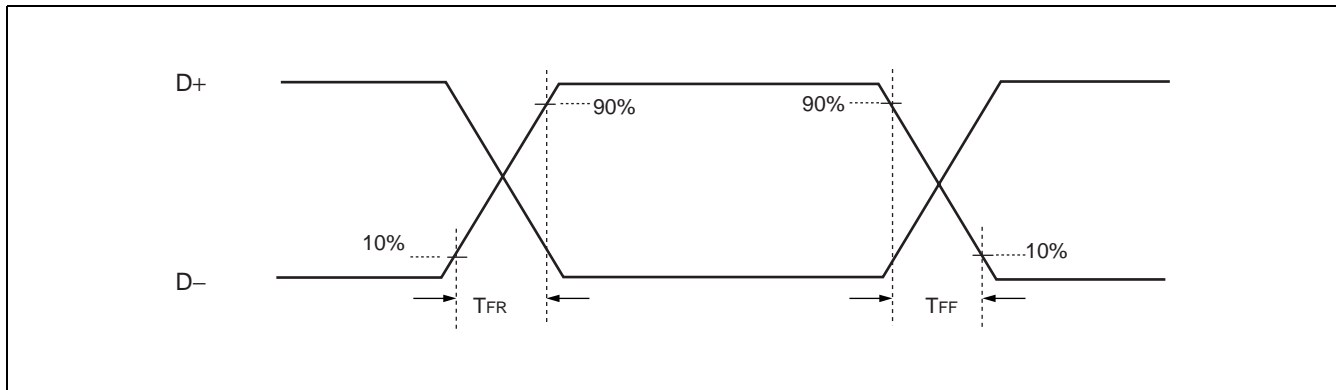
(13) I²C

$(V_{DE} = 3.3 \text{ V} \pm 0.15 \text{ V}, V_{DD} = V_{DDP} = 1.8 \text{ V} \pm 0.1 \text{ V}, V_{SS} = 0 \text{ V}, Ta = 0 \text{ °C to} + 70 \text{ °C})$

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
I²C I/F output	SCL[1 : 0]	Output fall time	—	23*	250	ns
		Output rise time	—	23*	300	ns
	SDA[1 : 0]	Output fall time	—	23*	1000	ns
		Output rise time	—	23*	300	ns

$* : 20 + 0.1 \times C$ (C = Capacitance of one bus line in pF)

Notes: • Each parameter is valid within the specified ranges of temperatures and supply voltages unless otherwise noted.
• Each voltage value is based on the GND level. The timing measurement reference point is 1.5 V and the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less.
• The external output load capacitance is 30 pF.

(14) Memory Stick Interface

   Customers are advised to consult with our sales representatives , if you use MS interface.

(15) Power Sequence

$(V_{DE} = 3.3\ V \pm 0.15\ V, V_{DD} = V_{DDP} = 1.8\ V \pm 0.1\ V, V_{SS} = 0\ V, Ta = 0\ ^{\circ}C\ to\ + 70\ ^{\circ}C)$

Item	Parameter		Reference Signal	240 MHz/266 MHz		Unit
				Min	Max	
Power-on	V_{DE} rise time	T_{RE}	—	—	30	ms
	V_{DD} rise time	T_{RD}	—	—	20	ms
	Delay time from V_{DE} rise to V_{DD} rise	T_{DRED}	—	−100	100	ms

Note : Power-off Sequence is not defined.

• Power-on Sequence
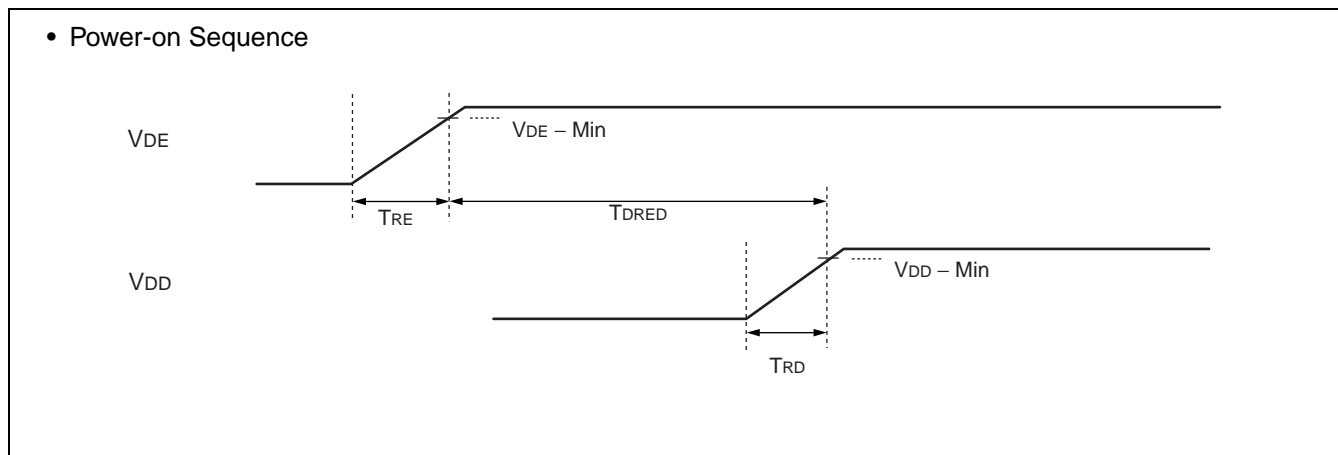
MB93423

5. Clock Setting

In this LSI, the clock signal inputted into CLKIN is multiplied by internal PLL, and it has distributed to each part in LSI.

The multiplication rate for each clock is decided using the CMODE [3 : 0] pins. Depending on this setup, the maximum frequency of CLKIN may be restricted.

The maximum frequency that can be inputted into CLKIN and the frequency of each part of LSI are shown below.

CMODE [0]to[3]				Ratio*		CLKIN frequency	Internal operating clock of this LSI				
3	2	1	0	Frequency			External bus	SDRAM	Core bus	Core	DSU
0	0	-	-	Reserved							
0	1	0	0	Ratio*			×1	×1	×1	×2	×2	×0.25
				Freq. [MHz]	MB93423BGL-GE1	60.0	60.0	60.0	120.0	120.0	15.0
					MB93423-26BGL-GE1	66.7	66.7	66.7	133.3	133.3	16.7
0	1	0	1	Ratio*			×1	×1	×2	×4	×4	×0.5
				Freq. [MHz]	MB93423BGL-GE1	30.0	30.0	60.0	120.0	120.0	15.0
					MB93423-26BGL-GE1	33.3	33.3	66.7	133.3	133.3	16.7
0	1	1	-	Reserved							
1	0	0	0	Ratio*			×1	×1	×1	×1	×2	×0.25
				Freq. [MHz]	MB93423BGL-GE1	60.0	60.0	60.0	60.0	120.0	15.0
					MB93423-26BGL-GE1	66.7	66.7	66.7	66.7	133.3	16.7
1	0	0	1	Ratio*			×1	×1	×2	×2	×4	×0.5
				Freq. [MHz]	MB93423BGL-GE1	60.0	60.0	120.0	120.0	240.0	30.0
					MB93423-26BGL-GE1	66.7	66.7	133.3	133.3	266.6	33.3
1	0	1	0	Reserved							
1	0	1	1	Ratio*			×1	×1	×4	×4	×8	×1
				Freq. [MHz]	MB93423BGL-GE1	30.0	30.0	120.0	120.0	240.0	30.0
					MB93423-26BGL-GE1	33.3	33.3	133.3	133.3	266.6	33.3
1	1	0	0	Ratio*			×1	×1	×1	×2	×4	×0.5
				Freq. [MHz]	MB93423BGL-GE1	60.0	60.0	60.0	60.0	240.0	30.0
					MB93423-26BGL-GE1	66.7	66.7	66.7	66.7	266.6	33.3
1	1	0	1	Ratio*			×1	×1	×2	×4	×8	×1
				Freq. [MHz]	MB93423BGL-GE1	30.0	30.0	60.0	120.0	240.0	30.0
					MB93423-26BGL-GE1	33.3	33.3	66.7	133.3	266.6	33.3
1	1	1	-	Reserved							

* : "×" indicates the frequency ratio for the external input clock.

Notes :
- As the setting of CMODE = 0, 1, 2, 3, 6, 7, A, E, F is not confirmed for operation guarantee, do not set them.
- By default, the operating frequency of the resource bus clock is the same as that of the external bus. When CLKC.p0 is set to "1", the operating frequency of the resource bus clock is half that of the external bus.

■ CONNECTION WITH MEMORY

1. Connection with ROM or SRAM

An example of connection between this processor and ROM or SRAM, etc. is shown below.

Connection example : when connecting 2 SRAMs (256 K × 8 bits each) to 16-bit bus (The polarity of BE is positive logic.)
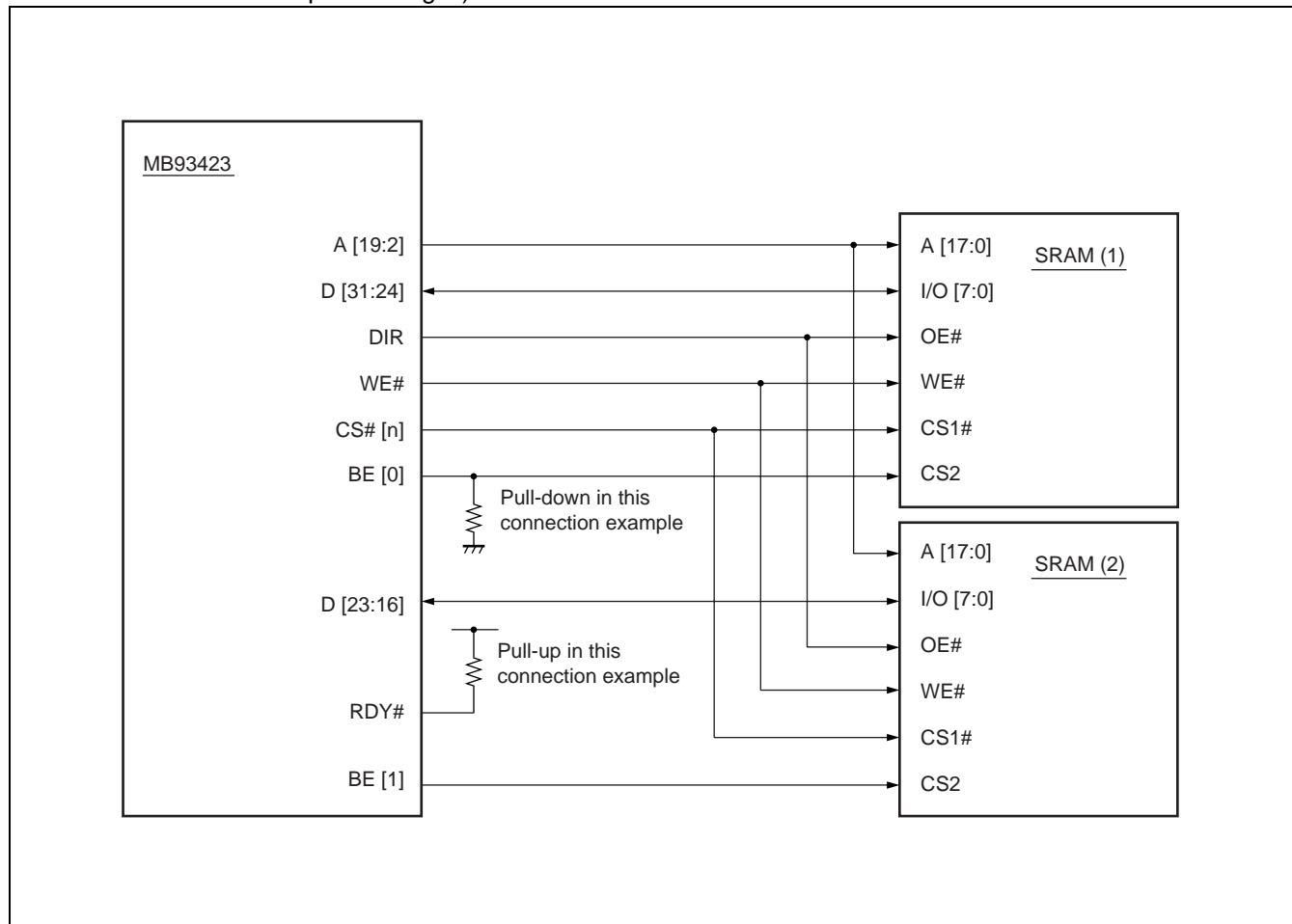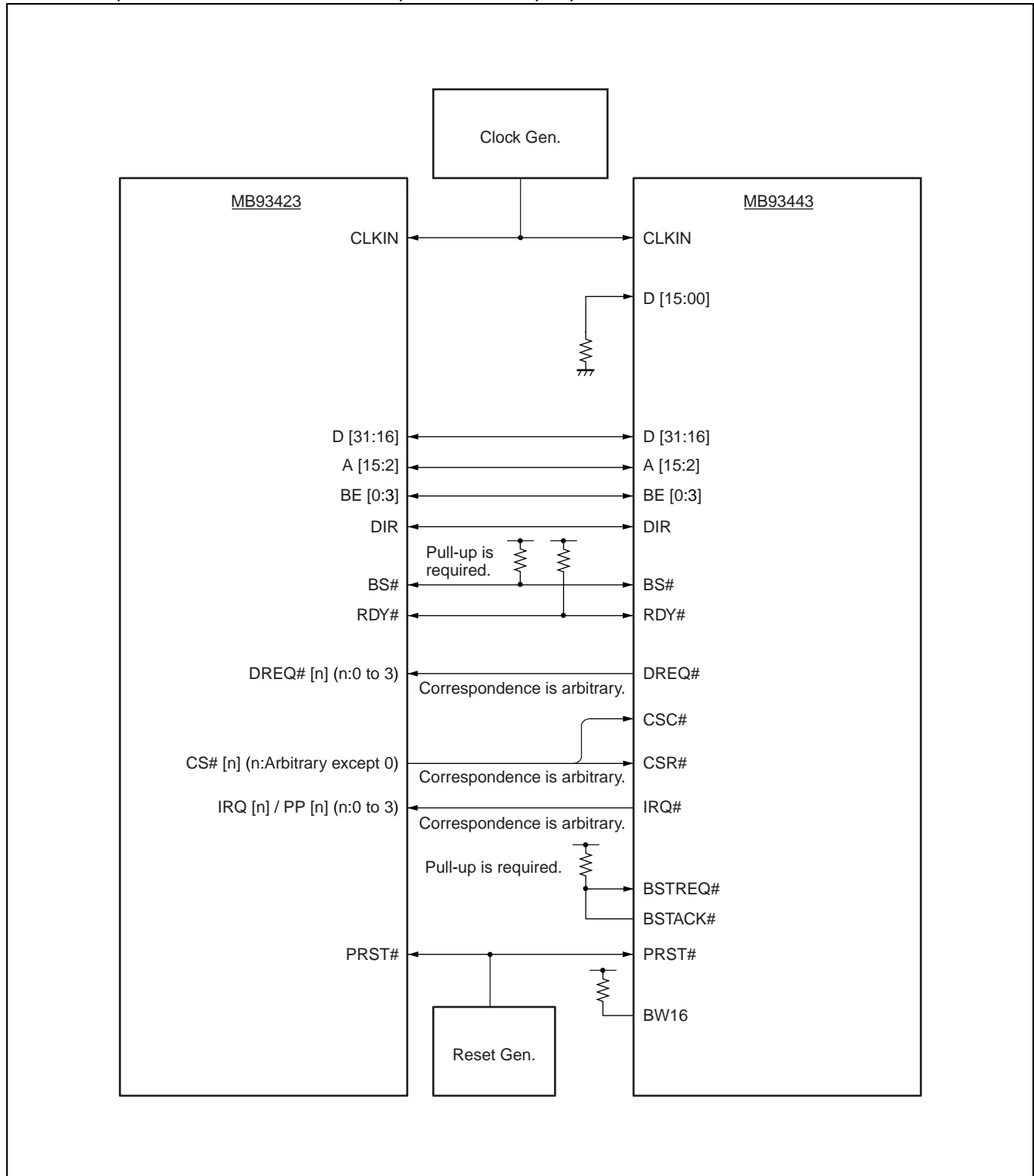
2. Connection with SDRAM

DCS#[2] and DCS#[3] are only used for connecting the 168-pin registered DIMM. Connect the 168-pin registered DIMM as follows. The DIMM must be "registered". In the registered DIMM, it is assumed that the module connected to DCS#[2] or DCS#[3] is used after DCS#, DBA, DA, DRAS#, DCAS#, DWE#, DDQM, and DCKE are latched once at the rising of DCLK signal. When using DCS#[2] or DCS#[3], the bus width must be set to the 32-bit mode.
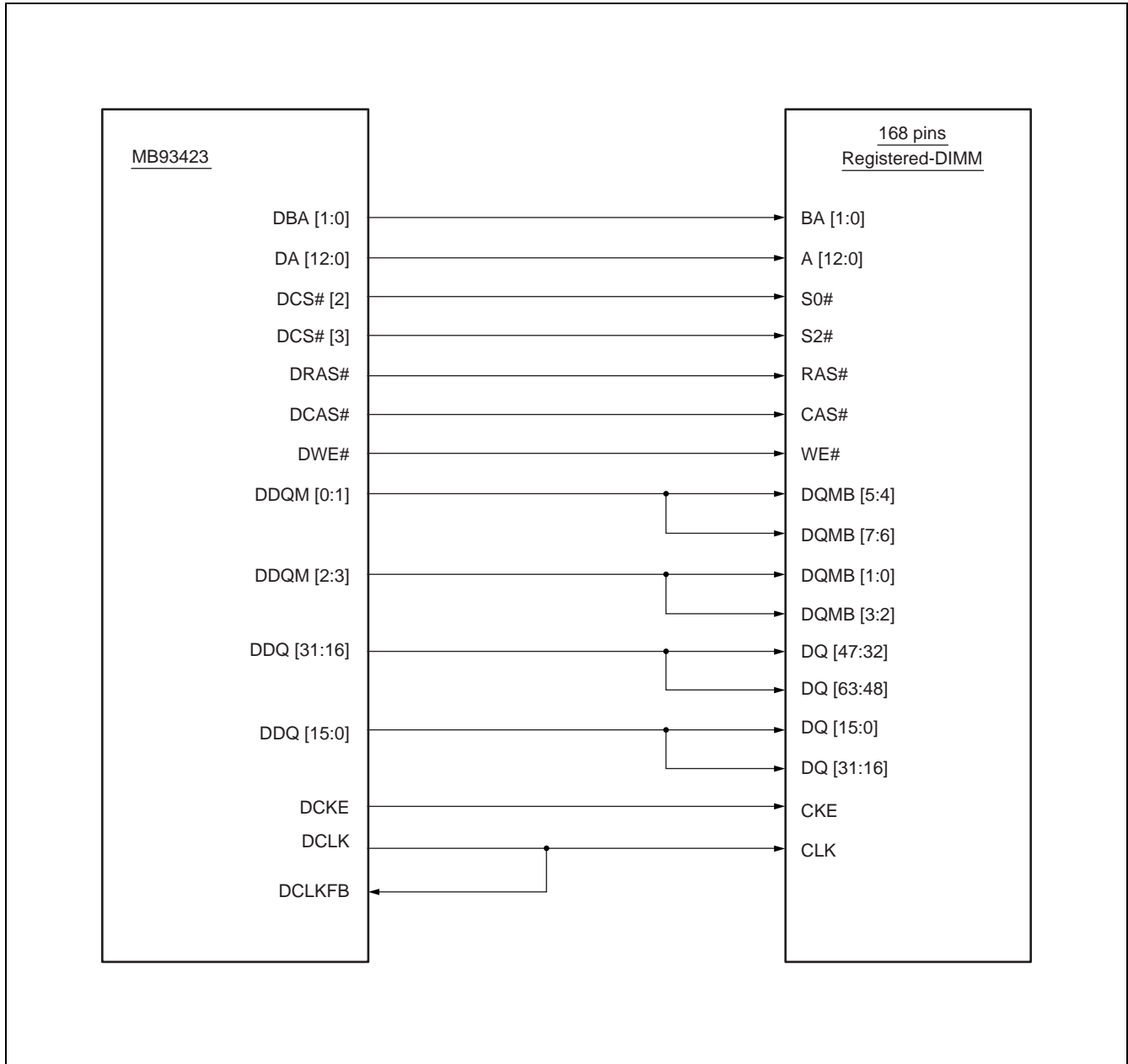
Example : Connecting Registered-DIMM to DCS#[3 : 2]

DCS#[2] and DCS#[3] are only used for connecting the 168-pin registered DIMM. Connect the 168-pin registered DIMM as follows. The DIMM must be "registered". In the registered DIMM, it is assumed that the module connected to DCS#[2] or DCS#[3] is used after DCS#, DBA, DA, DRAS#, DCAS#, DWE#, DDQM, and DCKE are latched once at the rising of DCLK signal. When using DCS#[2] or DCS#[3], the bus width must be set to the 32-bit mode.

MB93423
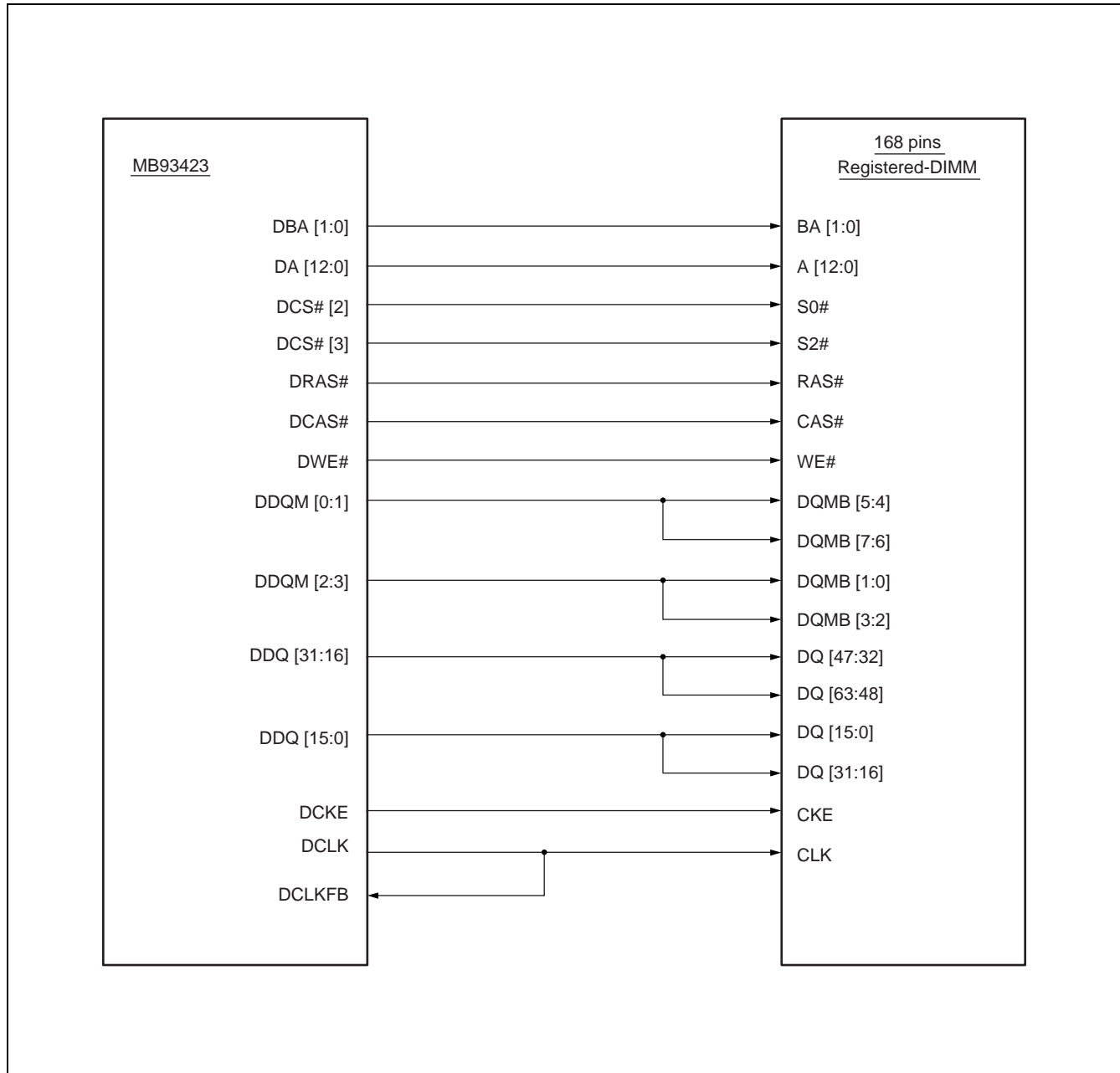
■ CONNECTION WITH PERIPHERAL DEVICE

1. Connection with MB93443 (IDE/PC-Card Host Controller)

An example of connection between this processor and peripheral device is shown below 16-bit bus.

2. Connection with MB93441 (PCI Bridge Chip)

An example of connection between this processor and peripheral device is shown below 16-bit bus.
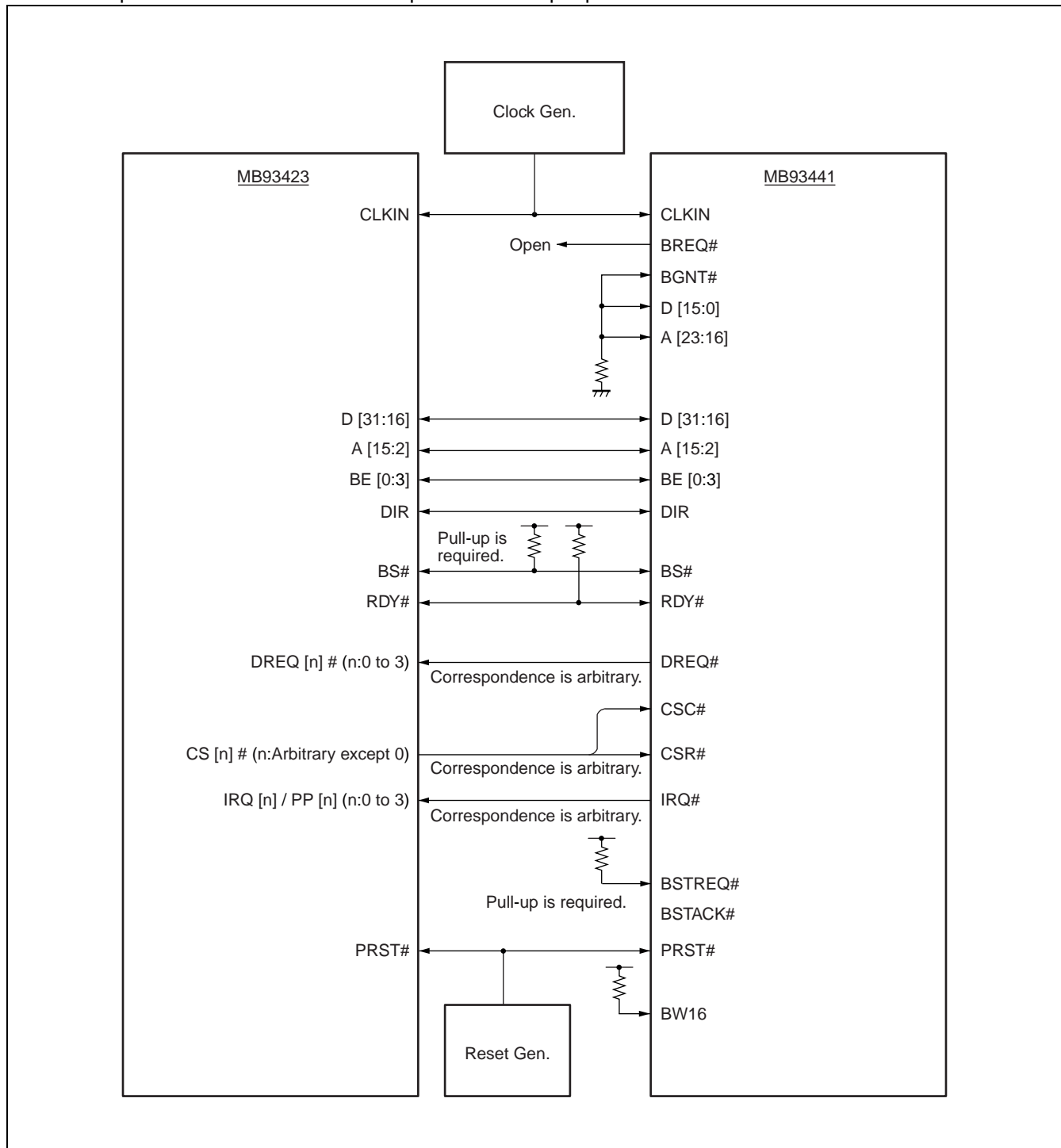
Note : Because address A[23 : 16] is connected to GND as shown in the above figure, it will be short out when MB93441 is a bus master.
However, there is no bus slave function and it is prohibited to be a bus master, therefore it will not be short out.

■ PACKAGE DIMENSION

337-ball plastic PFBGA
    (BGA-337P-M03)

13.00±0.10(.512±.004)

⊕ 0.20(.008) S B

12.00(.472)REF

B   0.50(.020)
         TYP

13.00±0.10
(.512±.004)

12.00(.472)
REF

A

0.50(.020)
TYP

3.00(.118)
REF

(INDEX AREA)

⊕ 0.20(.008) S A

AE AC AA W U   R N L   J G E C A
  AD AB Y V   T P M K   H F D B

3.00(.118)
REF

INDEX

386-ø0.30±0.10
(386-ø.012±.004)

⊕ ø0.05(.002) Ⓜ S A B

S

0.10(.004) S

0.25±0.10
(.010±.004)
(Stand off)

1.15±0.20
(.045±.008)
(Seated height)
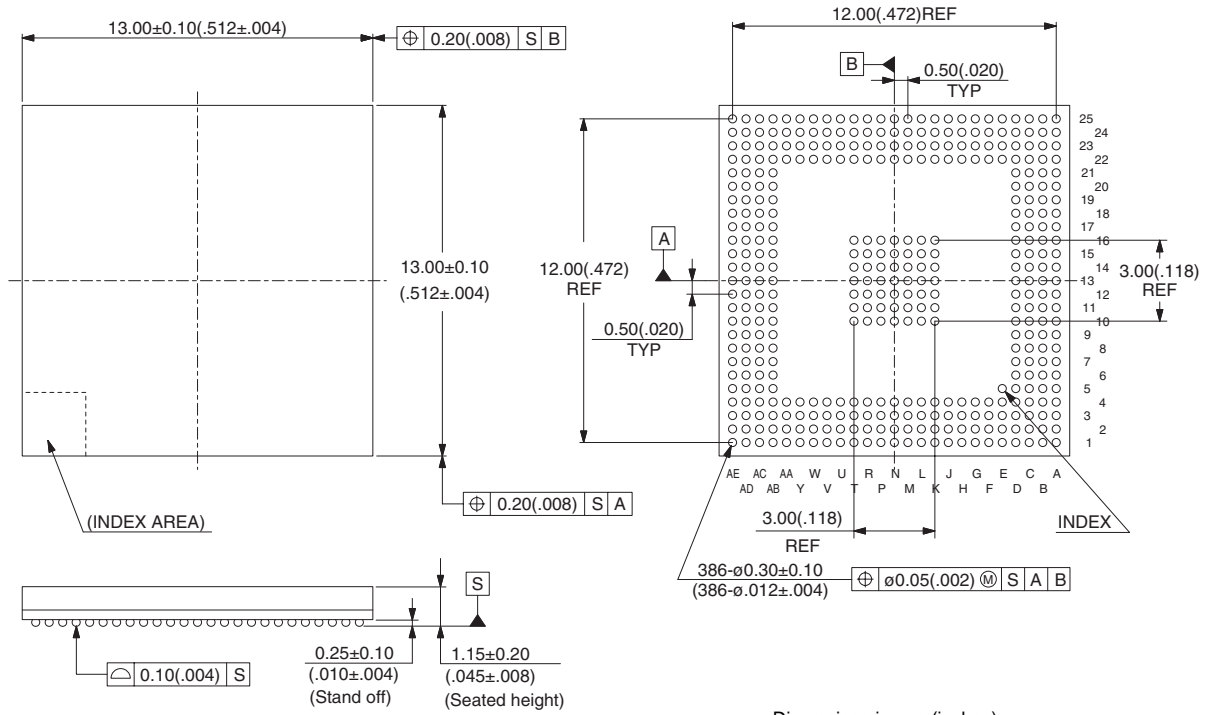
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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