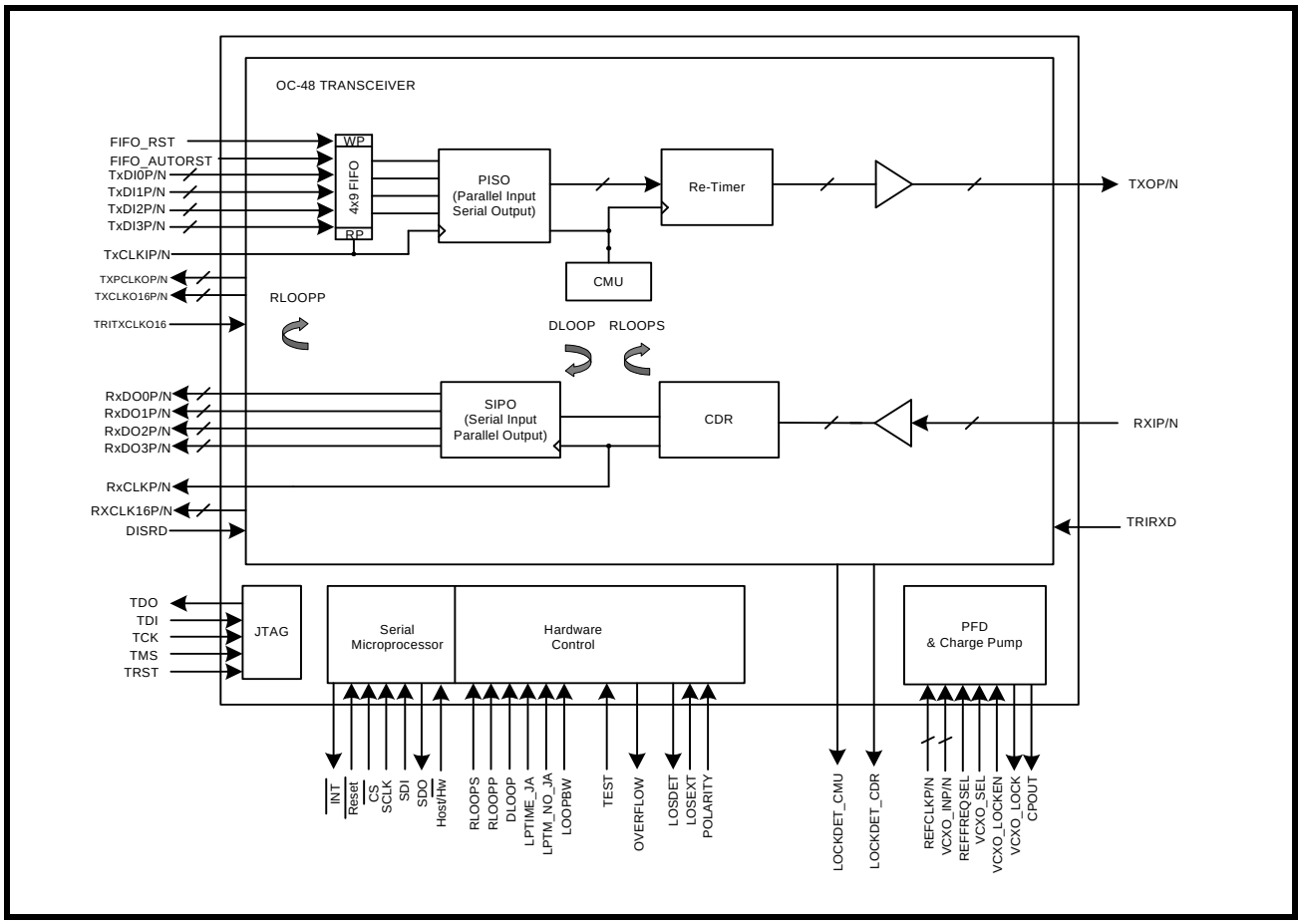
GENERAL DESCRIPTION

The XRT91L80 is a fully integrated SONET/SDH transceiver for SONET OC-48 allowing the use of Forward Error Correction (FEC) capability. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from slower external clock references. It also provides Clock and Data Recovery (CDR) functions by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The chip provides serial-to-parallel and parallel-to-serial converters and 4-bit LVDS system interfaces in both receive and transmit directions. The transmit section includes a 4x9 Elastic Buffer (FIFO) to absorb any phase differences between the transmitter input clock and the internally generated transmitter reference clock. In the event of an overflow, an internal FIFO control circuit outputs an OVERFLOW indication. The FIFO under the control of the AUTORST pin can automatically recover from an overflow condition. The operation of the device can be monitored by checking the status of the LOCKDET and LOSDET output signals. An on-chip phase/frequency detector and charge-pump offers the ability to form a de-jittering PLL with an external VCXO that can be used in loop timing mode to clean up the recovered clock in the receive section.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FIGURE 1. BLOCK DIAGRAM OF XRT91L80



FEATURES

- 2.488 / 2.666 Gbps Transceiver
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, limiting amplifier and clock data recovery (CDR) functions
- Host mode serial microprocessor interface simplifies monitor and control
- Separate reference and VCXO input ports support multiple de-jittering modes
- On-chip phase detector and charge pump for external VCXO based de-jittering PLL
- Targeted for SONET OC-48/SDH STM-16 Applications
- Selectable full duplex operation between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.666 Gbps
- 4-bit LVDS data paths at 622/666 MHz compliant with OIF SFI-4 Implimentation Agreement
- Internal FIFO decouples transmit input and output clocks
- Tx CMU and Rx CDR lock detect
- Provides Local, Remote and Split Loop-Back modes as well as Loop Timing mode
- Diagnostics features include various lock detect functions
- Meets Telcordia, ANSI and ITU-T jitter requirements
- Operates at 1.8V with 3.3V I/O
- 420mW Typical Power Dissipation
- Package: 12 x 12 mm 196-pin STBGA
- IEEE 1149.1 Compatable JTAG port

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT91L80IB	196 STBGA	-40℃ to +85℃

FIGURE 2. 196 BGA PINOUT OF THE XRT91L80 (TOP VIEW)

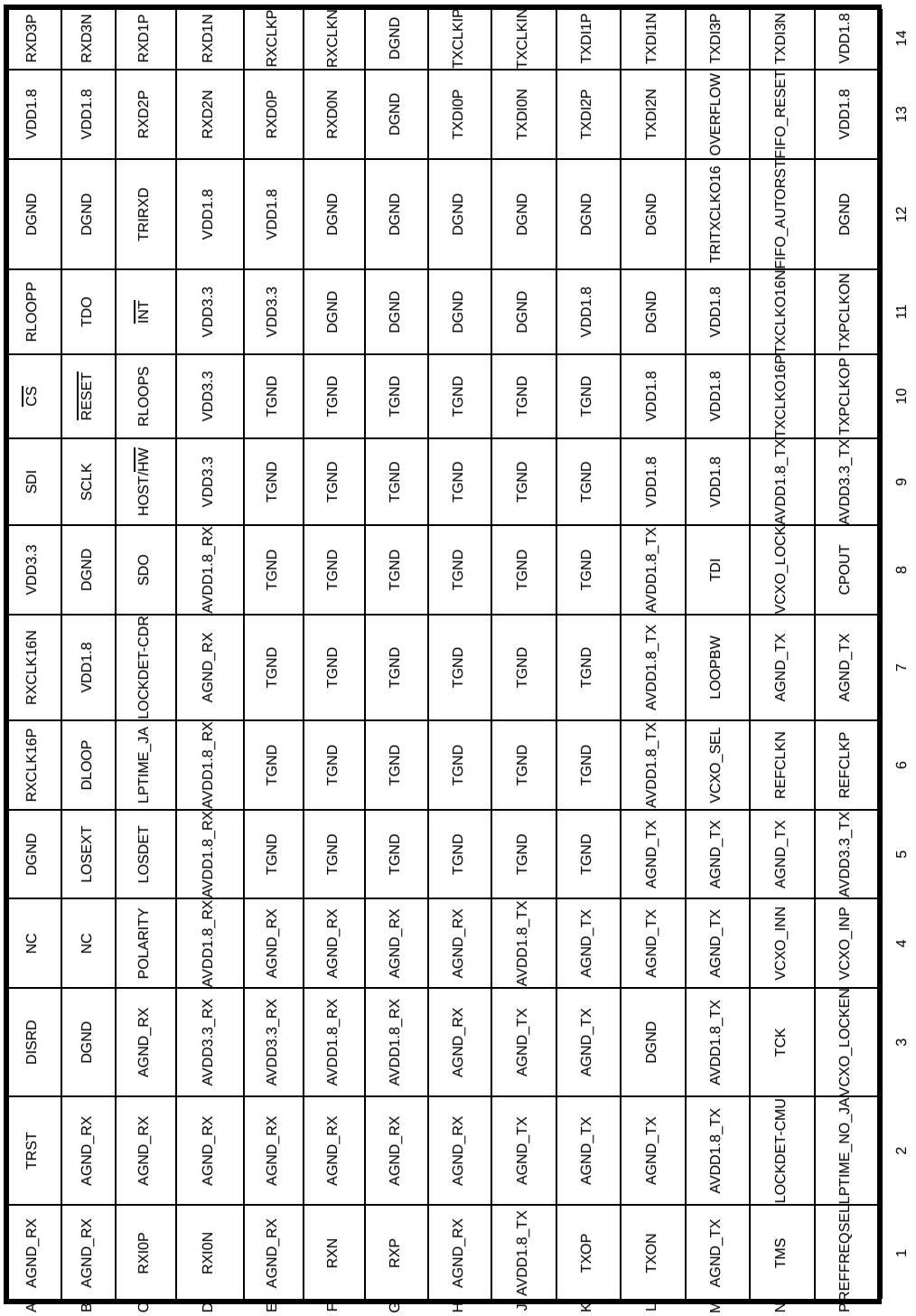


TABLE OF CONTENTS

PIN DESCRIPTIONS

SERIAL MICROPROCESSOR INTERFACE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
Host/$\overline{Hw}$	LVTTL	I	C9	**Host or Hardware Mode Select Input** The XRT91L80 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. By default, the device is configured in the Hardware mode. "Low" = Hardware Mode "High" = Host Mode This pin is provided with an internal active pull-down.
$\overline{CS}$	LVTTL	I	A10	**Chip Select Input (Host Mode Only)** Active low signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High". This pin is provided with an internal active pull-up.
SCLK	LVTTL	I	B9	**Serial Clock Input (Host Mode Only)** Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation. This pin is provided with an internal active pull-down.
SDI	LVTTL	I	A9	**Serial Data Input (Host Mode Only)** When $\overline{CS}$ is pulled "Low", the serial input data is sampled on the rising edge of SCLK. This pin is provided with an internal active pull-down.
SDO	LVTTL	O	C8	**Serial Data Output (Host Mode Only)** If a Read function is initiated, the serial output data is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16.
$\overline{INT}$	LVTTL	O	C11	**Interrupt Output (Host Mode Only)** Active low signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High".
$\overline{RESET}$	LVTTL	I	B10	**Master Reset Input** Active low signal. When this pin is pulled "Low" for more than 10µS, the internal registers are set to their default state. See the register description for the default values. This pin is provided with an internal active pull-up.

HARDWARE CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RLOOPS	LVTTL	I	C10	**Serial Remote Loopback** **Hardware Mode** The serial remote loopback mode interconnects the receive serial input data to the transmit serial output data. If serial remote loopback is enabled, the 4-bit parallel transmit input data is ignored while the 4-bit parallel receive output data is maintained. "Low" = Disabled "High" = Serial Remote Loopback Mode Enabled This pin is provided with an internal active pull-down. ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*
RLOOPP	LVTTL	I	A11	**Parallel Remote Loopback** **Hardware Mode** The parallel remote loopback mode allows the input serial data stream to pass through the clock and data recovery circuit and loopback at the parallel interface to the serial output port. The 4-bit parallel transmit input data is ignored while the 4-bit parallel receive output data is maintained. "Low" = Disabled "High" = Parallel Remote Loopback Mode Enabled This pin is provided with an internal active pull-down. ***NOTE:*** *DLOOP and RLOOPS should be **disabled** when RLOOPP is enabled.*
DLOOP	LVTTL	I	B6	**Digital Loopback** **Hardware Mode** The digital loopback mode interconnects the 4-bit parallel transmit input data and TxCLK to the 4-bit parallel receive output data and RxCLK respectively while maintaining the transmit serial output data. If digital loopback is enabled, the receive serial input data is ignored. "Low" = Disabled "High" = Digital Loopback Mode Enabled This pin is provided with an internal active pull-down. ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*
LPTIME_JA	LVTTL	I	C6	**Loop Timing Mode With Jitter Attenuation** The LPTIME_JA pin must be set "High" in order to select the recovered receive clock as the reference source for the de-jitter PLL. "Low" = Disabled "High" = Enabled This pin is provided with an internal active pull-down.
LPTIME_NO_JA	LVTTL	I	P2	**Loop Timing Mode With No Jitter Attenuation** When the loop timing mode is activated the external reference clock to the input of the CMU is replaced with the 1/16th or the 1/32nd of the high-speed recovered receive clock from the CDR. "Low" = Disabled "High" = Loop timing Activated This pin is provided with an internal active pull-down.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0P TXDI0N TXDI1P TXDI1N TXDI2P TXDI2N TXDI3P TXDI3N	LVDS	I	H13 J13 K14 L14 K13 L13 M14 N14	**Transmit Parallel Data Input** The 622Mbps 4-bit parallel transmit input data should be applied to the transmitters simultaneously referenced to the rising edge of the TXCLKI input. The 4-bit parallel interface is multiplexed into the transmit serial output interface MSB first (TXDI3P/N). ***NOTE:*** *The XRT91L80 can accept 666Mbps 4-bit parallel transmit input data for Forward Error Correction (FEC) Applications.*
TXCLKIP TXCLKIN	LVDS	I	H14 J14	**Transmit Input Clock** 622MHz input clock reference for the 4-bit parallel transmit input data TXDIP/N[3:0]. ***NOTE:*** *The XRT91L80 can accept a 666MHz transmit input clock for Forward Error Correction (FEC) Applications.*
TXOP TXON	CMLDIFF	O	K1 L1	**Transmit Serial Data Output** The transmit serial data stream is generated by multiplexing the 4-bit parallel transmit input data into a 2.488Gbps serial data stream. In Forward Error Correction, the transmit serial data stream is 2.666Gbps.
REFCLKP REFCLKN	LVPECL	I	P6 N6	**Reference Clock Input** This differential input clock reference is used for the transmit clock multiplier unit (CMU) to provide the necessary high speed clock reference for this device. Pin REFFREQSEL determines the value used as the reference. See Pin REFFREQSEL for more details.
VCXO_INP VCXO_INN	LVPECL	I	P4 N4	**Voltage Controled Oscillator Input** This differential input clock is used for the transmit PLL jitter attenuation. Pin REFFREQSEL determines the value used as the reference. See Pin REFFREQSEL for more details.
REFFREQSEL	LVTTL	I	P1	**Reference Clock Frequency Select** **Hardware Mode** This pin is used to select the frequency of the REFCLK input to the CMU. "Low" = 77.76MHz (83.5MHz for FEC) "High" = 155.52MHz (167MHz for FEC) This pin is provided with an internal active pull-down.
VCXO_SEL	LVTTL	I	M6	Selects De-Jitter VCXO Option **Hardware Mode** This pin selects either the normal REFCLK or the de-jitter VCXO as a reference clock. "Low" = Normal REFCLK Mode "High" = De-Jitter VCXO Mode This pin is provided with an internal active pull-down.
VCXO_LOCK	LVTTL	O	N8	**De-Jitter PLL Lock Detect** If the de-jitter PLL lock detect is enabled with Pin P3 and the de-jitter VCXO mode is selected by Pin M6, this pin will pull "High" when the PLL is locked. "Low" = VCXO out of Lock "High" = VCXO Locked

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
VCXO_LOCKEN	LVTTL	I	P3	**De-Jitter PLL Lock Detect Enable** **Hardware Mode** This pin enables the VCXO lock detect Pin N8 to be active. "Low" = VCXO_LOCK disabled "High" = VCXO_LOCK enabled This pin is provided with an internal active pull-down.
CPOUT	-	O	P8	**Charge Pump Output (for external VCXO)** The nominal output of the charge pump is 250µA
LOOPBW	LVTTL	I	M7	**CMU Loop Bandwidth Select** **Hardware Mode** This pin is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. "Low" = Narrow Band (1x) "High" = Wide Band (4x) This pin is provided with an internal active pull-down.
TXPCLKOP TXPCLKON	LVDS	O	P10 P11	**Transmit Clock Output (622/666 MHz)** This clock can be used for the downstream device to generate the TXDI data and TXCLK. This enables the downstream device and the OC-48 transceiver to be in synchronization.
TXCLKO16P TXCLKO16N	LVDS	O	N10 N11	**Auxillary Clock** 155.52(166)MHz auxillary clock derived from CMU output. This clock can also be used for the downstream device as a reference for generating the TXDI data and TXCLK. This enables the downstream device and the OC-48 transceiver to be in synchronization.
TRITXCLKO16	LVTTL	I	M12	**Tri-State Enable** **Hardware Mode** This pin is used to tri-state the auxillary clock. "Low" = TXCLKO16 Enabled "High" = TXCLKO16 Tri-State This pin is provided with an internal active pull-down.
LOCKDET_CMU	LVTTL	O	N2	**CMU Lock Detect** This pin is used to monitor the lock condition of the clock multiplier unit. "Low" = CMU Out of Lock "High" = CMU Locked
OVERFLOW	LVTTL	O	M13	**Transmit FIFO Overflow** This pin is used to monitor the transmit FIFO status. "Low" = Normal Status "High" = Overflow Condition

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
FIFO_RST	LVTTL	I	N13	**FIFO Control Reset** **Hardware Mode** FIFO_RST should be held "High" for 10 cycles of TXCLK during power-up in order to flush out the FIFO. Upon an interrupt indication that the FIFO has an overflow condition, this pin is used to reset or flush out the FIFO. This pin is provided with an internal active pull-down. ***NOTE:*** *To automatically reset the FIFO, see FIFO_AUTORST pin.*
FIFO_AUTORST	LVTTL	I	N12	**Automatic FIFO Reset** **Hardware Mode** If this pin is set "High", the OC-48 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by pulling FIFO_RST "High" for 10 cycles of TXCLK. "Low" = Manual FIFO reset required for overflow conditions "High" = Automatically resets FIFO upon overflow detection This pin is provided with an internal active pull-down.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXD0P RXD0N RXD1P RXD1N RXD2P RXD2N RXD3P RXD3N	LVDS	O	E13 F13 C14 D14 C13 D13 A14 B14	**Receive Parallel Data Output** 622Mbps 4-bit parallel receive output data is updated simultaneously on the rising edge of the RXCLK output. The 4-bit parallel interface is de-multiplexed from the receive serial input data MSB first (RXD3P/N). ***NOTE:*** *The XRT91L80 can output 666Mbps 4-bit parallel receive output data for Forward Error Correction (FEC) Applications.*
RXCLKP RXCLKN	LVDS	O	E14 F14	**Receive Output Clock** 622MHz output clock reference for the 4-bit parallel receive output data RXDP/N[3:0]. ***NOTE:*** *The XRT91L80 can output a 666MHz receive output clock for Forward Error Correction (FEC).*
TRIRXD	LVTTL	I	C12	**Tri-State Receive Parallel Data Output** **Hardware Mode** This pin is used to control the activity of the 4-bit parallel receive output bus and its reference clock. "Low" = Normal Mode "High" = Tri-State RXDP/N[3:0] and RXCLK This pin is provided with an internal active pull-down.
RXIP RXIN	CMLDIFF	I	C1 D1	**Receive Serial Data Input** The receive serial data stream of 2.488Gbps is applied to these input pins. In Forward Error Correction, the receive serial data stream is 2.666Gbps.
RXP RXN	-	I	G1 F1	**Biasing Resistor** These 2 pins should be connected by a 402Ω resistor

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXCLK16P RXCLK16N	LVDS	O	A6 A7	**155.52 (166) MHz Reference Clock** This output clock reference is derived from the recovered clock from the receive path.
LOCKDET_CDR	LVTTL	O	C7	**CDR Lock Detect** This pin is used to monitor the lock condition of the clock and data recovery unit. "Low" = CDR Out of Lock "High" = CDR Locked
LOSEXT	LVTTL	I	B5	**LOS or SD input from optical module** This pin is provided with an internal active pull-down.
POLARITY	LVTTL	I	C4	**Polarity for LOS input** **Hardware Mode** LOSEXT and POLARITY signals will be Exclusive NORed internally to generate the correct polarity. This pin is provided with an internal active pull-down.
LOSDET	LVTTL	O	C5	**LOS Detect** Flags LOS condition based on LOS/SD signal from optical module. "Low" = No Alarm "High" = A LOS condition is present
DISRD	LVTTL	I	A3	**Disable Receive Output Data Upon LOS** **Hardware Mode** If this pin is pulled "High", the receive output data will automically pull "Low" when a LOS condition occurs. "Low" = Disabled "High" = Mute Data Upon LOS This pin is provided with an internal active pull-down.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
VDDD3.3	PWR	A8, D9, D10, D11, E11	**Digital 3.3V Power Supply** VDDD3.3 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDDD3.3 power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_Rx	PWR	D3, E3	**Analog 3.3V Receiver Power Supply** AVDD3.3_Rx should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD3.3_Rx power supply pins should have bypass capacitors to the nearest ground.
AVDD3.3_Tx	PWR	P5, P9	**Analog 3.3V Transmitter Power Supply** AVDD3.3_Tx should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The TVDD3.3_Tx power supply pins should have bypass capacitors to the nearest ground.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
VDD1.8	PWR	A13, B7, B13, D12, E12, K11, L9, L10, M9, M10, M11, P13, P14	**Digital 1.8V Power Supply** VDDD1.8 should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDDD1.8 power supply pins should have bypass capacitors to the nearest ground.
AVDD1.8_Rx	PWR	D4, D5, D6, D8, F3, G3	**Analog 1.8V Receiver Power Supply** AVDD1.8_Rx should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_Rx power supply pins should have bypass capacitors to the nearest ground.
AVDD1.8_Tx	PWR	J1, J4, L6, L7, L8, M3, N9, M2	**Analog 1.8V Transmitter Power Supply** AVDD1.8_Tx should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD1.8_Tx power supply pins should have bypass capacitors to the nearest ground.
DGND	GND	A5, A12, B3, B8, B12, F11, F12, G11, G12, G13, G14, H11, H12, J11, J12, K12, L3, L11, L12, P12	**Digital Ground for 3.3V / 1.8V Digital Power Supplies** It is recommended that all ground pins of this device be tied together.
AGND_Rx	GND	A1, B1, B2, C2, C3, D2, D7, E1, E2, E4, F2, F4, G2, G4, H1, H2, H3, H4	**Receiver Analog Ground for 3.3V / 1.8V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
AGND_Tx	GND	J2, J3, K2, K3, K4, L2, L4, L5, M1, M4, M5, N5, N7, P7	**Transmitter Analog Ground for 3.3V / 1.8V Analog Power Supplies** It is recommended that all ground pins of this device be tied together.
TGND	GND	E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K5, K6, K7, K8, K9, K10	**Thermal Ground** It is recommended that all ground pins of this device be tied together.

NO CONNECTS

NAME	LEVEL	TYPE	PIN	DESCRIPTION
NC		NC	A4 B4	**No Connect** This pin can be left floating or tied to ground.

JTAG

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	N3	I	**Test clock:** Boundary Scan clock input. ***Note**: This input pin should be pulled "Low" for normal operation*
TMS	N1	I	**Test Mode Select:** Boundary Scan Mode Select input. JTAG is disabled by default. This pin is provided with an internal active pull-up. ***Note**: This input pin should be pulled "Low" for normal operation*
TDI	M8	I	**Test Data In:** Boundary Scan Test data input. This pin is provided with an internal active pull-up. ***Note**: This input pin should be pulled "Low" for normal operation*
TDO	B11	O	**Test Data Out:** Boundary Scan Test data output
TRST	A2	I	**JTAG Test Reset Input** This pin is provided with an internal active pull-up.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L80 Transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The Transceiver converts 4-bit parallel data at 622/666 MHz to a serial CML bit stream at 2.488/2.666Gbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), limiting amplifier and receive clock and data recovery (CDR) unit. The Transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 Hardware Mode vs. Host Mode

Functionality of the OC-48 Transceiver can be configured by using either Host mode or Hardware mode. If Hardware mode is selected by pulling Host/HW "Low" or leaving this pin unconnected, the functionality is controlled by the hardware pins described in the Hardware Pin Descriptions. However, if Host mode is selected by pulling Host/HW "High", the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Whether using Host or Hardware mode, the functionality remains the same. Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and the Register Bit Descriptions concentrate on configuring the device.

1.2 Input Clock Reference

The XRT91L80 can accept either a 77.76/83.3MHz or 155.52/166MHz input clock at REFCLKP/N as its internal timing reference for generating higher speed clocks. The reference clock can be provided with one of two frequencies chosen by REFCLKSEL. The reference frequency options for the XRT91L80 are listed in Table 1.

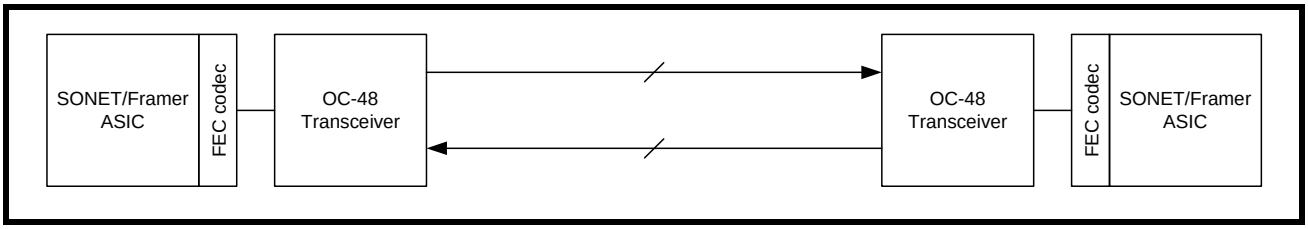
TABLE 1: REFERENCE FREQUENCY OPTIONS (NORMALMODE/FEC)

REFCLKSEL	REFERENCE CLOCK FREQUENCY	OUTPUT CLOCK FREQUENCY	OPERATING MODE
0	77.76/83.3 MHz	2.488/2.666 GHz	OC-48/STM-16
1	155.52/166 MHz	2.488/2.666 GHz	OC-48/STM-16

1.3 Forward Error Correction (FEC)

Forward Error Correction is used to control errors along a one-way path of communication. FEC sends extra information along with data which can be used by a receiver to check and correct the data without requesting re-transmission of the original information. It does so by introducing a known structure into a data sequence prior to transmission. The most common methods are to replace a 14-bit data packet with a 15-bit codeword structure, or to replace a 17-bit data packet with an 18-bit codeword structure. To maintain original bandwidth, a higher speed clock reference, derived by the ratio of 15/14 or 18/17 referenced to 77.76MHz or 155.52MHz is applied to the OC-48 transceiver using an external crystal. The XRT91L80 supports FEC by accepting an input clock reference up to 83.3MHz or 166MHz. This allows the Transmit 4-bit Parallel Input Data to be applied to the OC-48 transceiver at 666Mpbs which is converted to a 2.666Gbps serial output stream to an optical module. A simplified block diagram of FEC is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF FORWARD ERROR CORRECTION



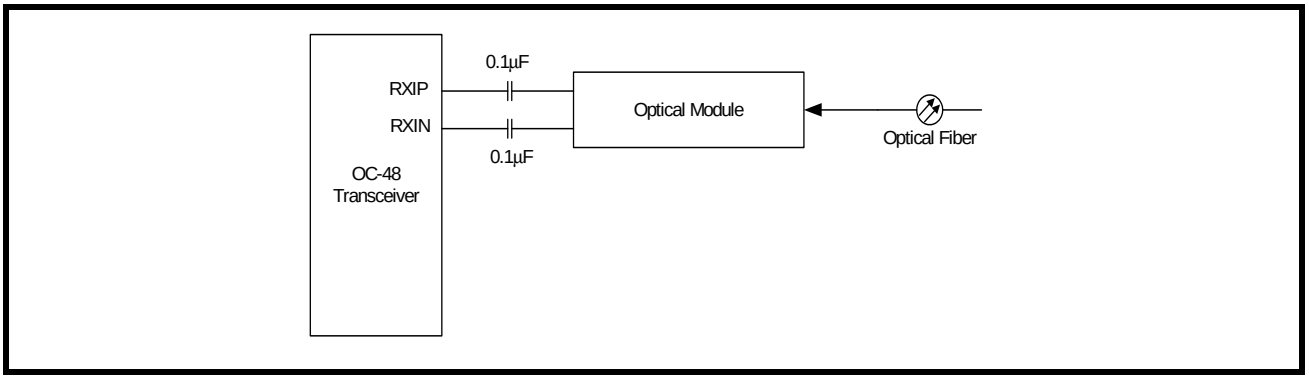
2.0 RECEIVE SECTION

The receive section of XRT91L80 includes the differential limiting amplifier inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high speed Non-Return to Zero (NRZ) serial data at 2.488/2.666 Gbps through the differential limiting amplifier input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into 4-bit-wide 622.08/666 Mbps parallel data and presented to the RXD[3:0]P/N LVDS parallel interface. A divide-by-4 version of the high-speed recovered clock RXCLKP/N, is used to synchronize the transfer of the 4-bit RXD[3:0]P/N data with the receive portion of the upstream device. Upon initialization or loss of signal or loss of lock the 155.52/77.76 MHz (166/83.3 MHz) external reference clock is used to start-up the clock recovery phase-locked loop for proper operation. A special loop-back feature can be configured when RLOOPP is used in conjunction with de-jittered loop-time mode that allows the re-transmitted data to comply with ITU and Bellcore jitter generation specifications.

2.1 Receive Serial Input

The receive serial inputs are applied to RXIP/N. The receive serial inputs should be AC coupled to an optical module or an electrical interface. A simplified block diagram is shown in Figure 4.

FIGURE 4. RECEIVE SERIAL INPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

2.2 Receive Clock and Data Recovery

The clock and data recovery unit accepts the high speed NRZ serial data from the differential CML receiver and generates a clock that is the same frequency as the incoming data. The clock recovery utilizes the REFCLKP/N to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the reference clock. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately 500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. When this condition occurs the PLL will declare Loss of Lock and the LOCKDET_CDR signal will be pulled low. A Loss of Lock condition will also be declared when the external LOSEXT is asserted. Whenever a Loss of Lock/Loss of Signal event occurs, the CDR will continue to supply a receive clock (based on the local reference) to the upstream framer device. When the DISRD control is enabled, receive parallel output data will be forced to an all zeroes condition for the entire duration that a LOS condition is detected. This acts as a receive data mute upon LOS function to prevent random noise from being misinterpreted as valid incoming data. When the LOSEXT becomes inactive and the recovered clock is determined to be within 500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch and lock back onto the incoming receive data stream and the lock detect output (LOCKDET_CDR) will go active.

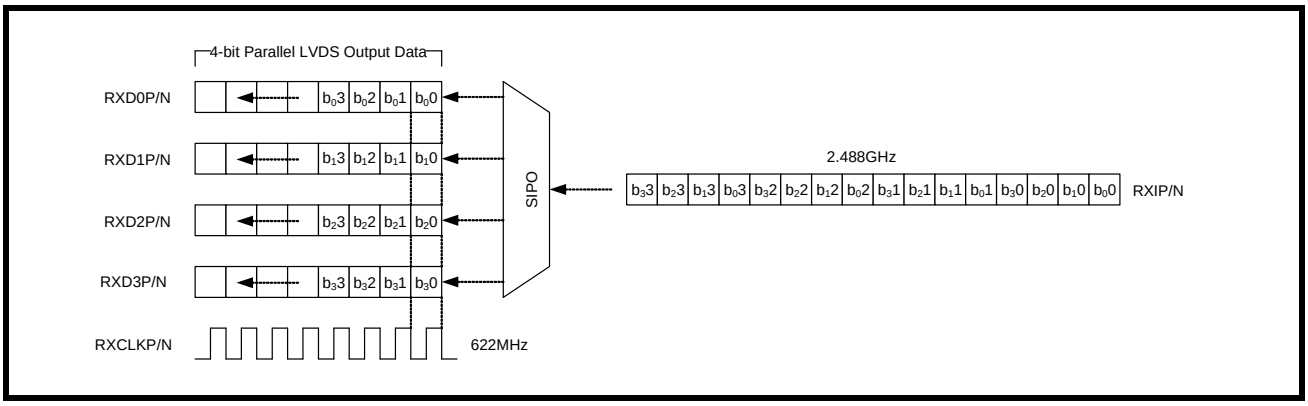
2.3 Loss Of Signal

XRT91L80 supports external Loss of Signal detection (LOS). The external LOS function is supported by the LOSEXT input. The TTL input is coming from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices the polarity of this signal can be either active low or active high. The LOSEXT and POLARITY inputs are Exclusive NOR’ed to generate the external loss control signal with the correct polarity. Whenever an external LOS is detected, the XRT91L80 will automatically output a high level signal on the LOSDET output pin as well as update the control registers whenever the host mode serial microprocessor interface feature is active.

2.4 Receive Serial Input to Parallel Output (SIPO)

The SIPO is used to convert the 2.488/2.666GHz serial input data to 622/666MHz parallel output data which can interface to a SONET Framer/ASIC. The SIPO bit de-interleaves the serial input data into a 4-bit parallel output to RXD3P/N. A simplified block diagram is shown in Figure 5.

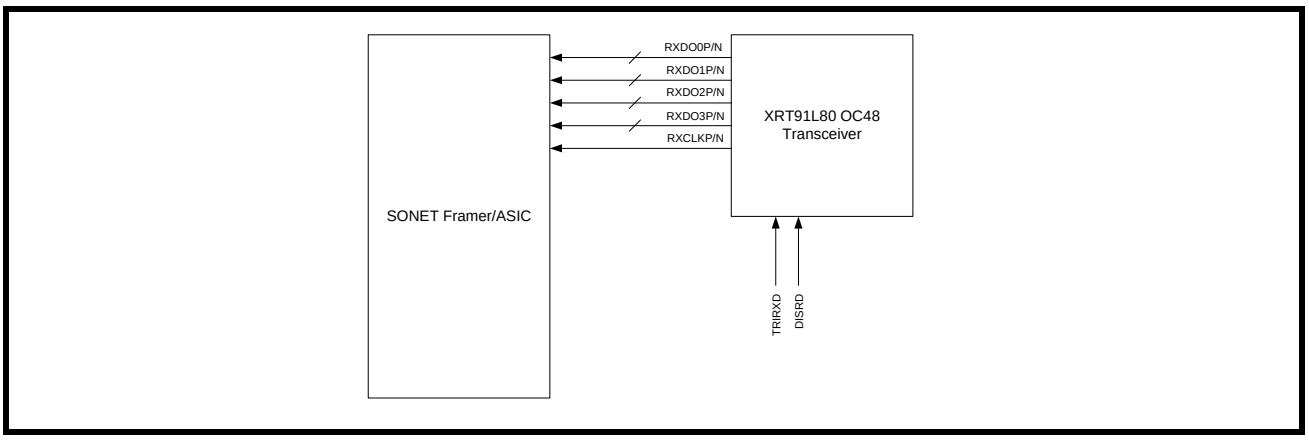
FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.5 Receive Parallel Output Interface

The 4-bit LVDS 622/666MHz parallel output data of the receive path is used to interface to a SONET Framer/ ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 6.

FIGURE 6. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.6 Receive Parallel Output Data Timing

The receive parallel output data from the OC-48 receiver will adhere to the setup and hold times shown in Figure 7 and Table 2.

FIGURE 7. RECEIVE PARALLEL OUTPUT TIMING

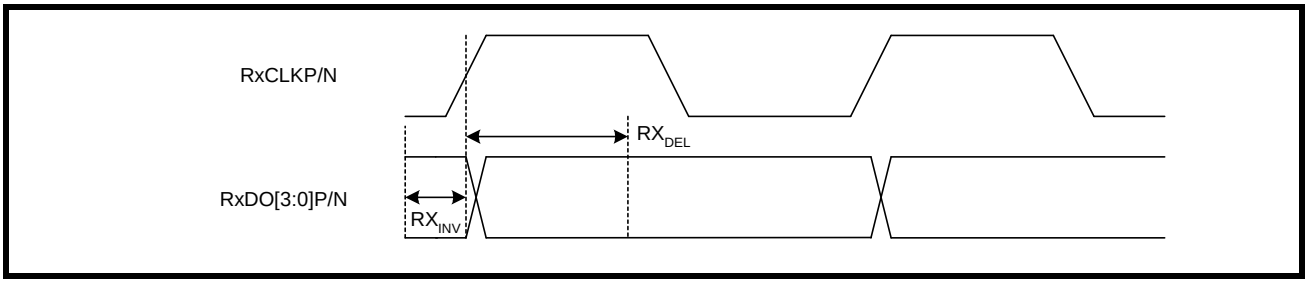


TABLE 2: RECEIVE PARALLEL OUTPUT DATA TIMING SPECIFICATIONS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
RX_{INV}	RxCLKP/N "High" to data invalid window			200	pS	
RX_{DEL}	RxCLKP/N "High" to data delay			200	pS	
RX_{DTY}	RxCLKP/N Duty Cycle		50		%	

2.7 Disable Receive Output Data Upon LOS

The Receiver outputs can automatically be pulled "Low" during a LOS condition to prevent data chattering. By pulling DISRD "High", the Receiver outputs will pull "Low" any time a LOS condition occurs.

2.8 Tri-State Receive Output Data

Unlike DISRD, TRIRXD is used to tri-state the Receiver outputs regardless of the input data stream. By pulling TRIRXD "High", the Receiver outputs will automically tri-state.

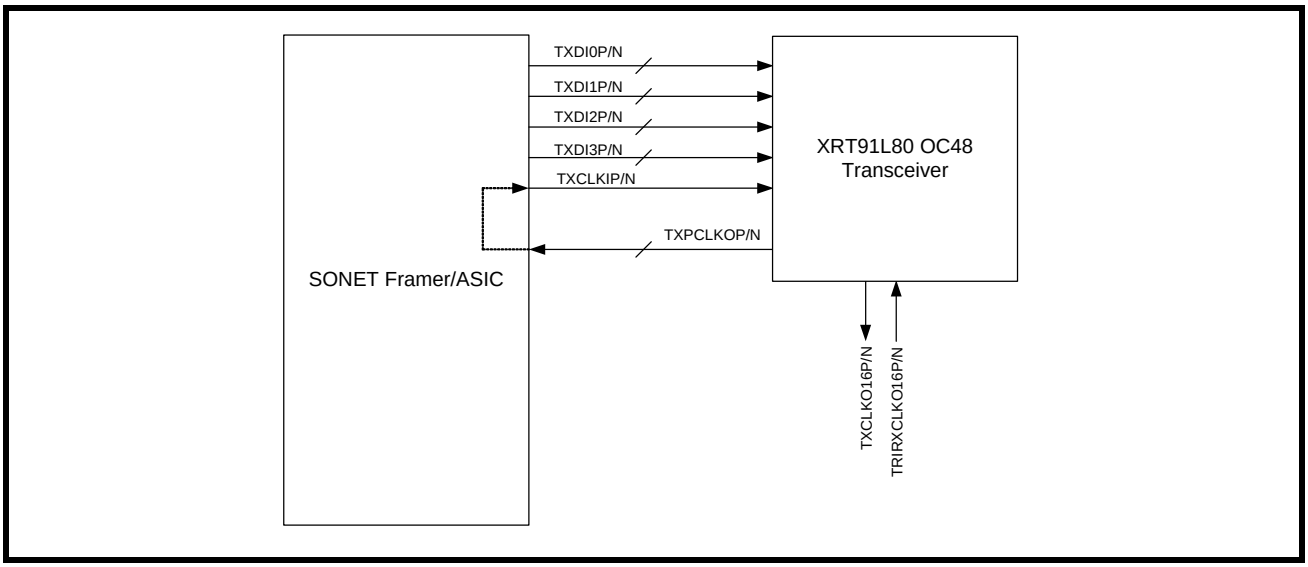
3.0 TRANSMIT SECTION

The transmit section of the XRT91L80 accepts 4-bit parallel LVDS data and converts it to serial CML output data intented to interface to an optical module. It consists of a 4-bit parallel LVDS interface, a 4x9 FIFO, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Current Mode Logic (CML) differential line driver, and Loop Timing modes. The CML serial output data rate is 2.488/2.666Gbps for OC-48 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 2.488/2.666GHz serial output clock is divided by four and the 622/666MHz clock is presented to the upstream device to be used as its timing source.

3.1 Transmit Parallel Interface

The parallel data from an upstream device is presented to the XRT91L80 through a 4-bit LVDS parallel bus interface TXDI[3:0]. The data is latched into a parallel input register on the rising edge of TXPCLKIP/N. If the SONET Framer/ASIC is synchronized to the same timing source as the XRT91L80, the transmit input data and clock can directly interface to the OC-48 transceiver. However, if the SONET Framer/ASIC is synchronized to a separate crystal, the XRT91L80 has two output clock references that can be used to synchronize the SONET Framer/ASIC. TXPCLKOP/N is a 622/666MHz LVDS output clock source that is derived from the input clock reference of the transceiver. TXCLKO16P/N is a 155.52/166MHz LVDS auxillary output clock source that is also derived from the input clock reference. Either of these two output clock sources can be used to synchronize the SONET Framer/ASIC to the XRT91L80. If the auxillary clock source is not used, it can be tri-stated by pulling TRIRXCLKO16 "High". A simplified block diagram of the parallel interface is shown in Figure 8.

FIGURE 8. TRANSMIT PARALLEL INPUT INTERFACE BLOCK



3.2 Transmit Parallel Input Data Timing

When applying parallel input data to the transmitter, the setup and hold times should be followed as shown in Figure 9 and Table 3.

FIGURE 9. TRANSMIT PARALLEL INPUT TIMING

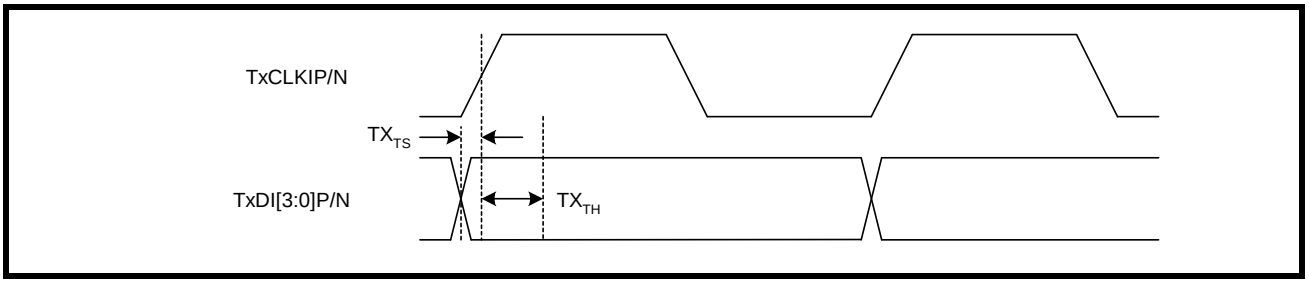


TABLE 3: TRANSMIT PARALLEL INPUT DATA TIMING SPECIFICATIONS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified						
SYMBOL	**PARAMETER**	**MIN.**	**TYP.**	**MAX.**	**UNITS**	**CONDITIONS**
TX_{TS}	TxCLKIP/N "High" to data setup time	300			pS	
TX_{TH}	TxCLKIP/N "High" to data hold time	300			pS	
TX_{DTY}	TxCLKIP/N Duty Cycle	40		60	%	

3.3 Transmit FIFO

The Parallel Interface also includes a 4x9 FIFO that can be used to eliminate difficult timing issues between the input transmit clock and the clock derived from the CMU. The use of the FIFO permits the system to tolerate an arbitrary amount of delay and jitter between TXCLKOP/N and TXCLKIP/N. The FIFO can be initialized when FIFO_RESET is asserted and held "High" for 10 cycles of the TXCLKO clock. Once the FIFO is centered, the delay between TXCLKO and TXCLKI can decrease or increase up to two periods of the low-speed clock (TXCLKO). Should the delay exceed this amount, the read and write pointers will point to the same word in the FIFO resulting in a loss of transmitted data (FIFO overflow). In the event of a FIFO overflow the FIFO control logic will initiate an OVERFLOW signal that can be used by an external controller to issue a RESET signal. The chip under the control of the FIFO_AUTORST pin can automatically recover from an overflow condition. When the FIFO_AUTORST input is set to a "High" level, once an overflow condition is detected, the chip will set the OVERFLOW pin to a high level and will automatically reset and center the FIFO.

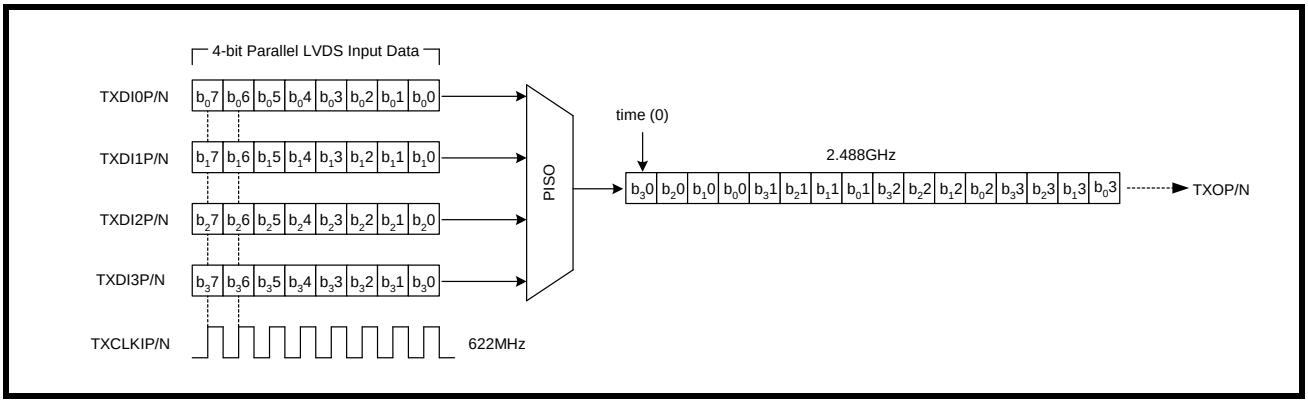
3.4 FIFO Calibration Upon Power Up

It is required that the FIFO_RST pin be pulled "High" for 10 TXCLK cycles to flush out the FIFO after the device is powered on. If the FIFO experiences an Overflow condition, FIFO_RST can be used to manually reset the FIFO. However, the OC-48 transceiver has an automatic reset pin that will allow the FIFO to automatically reset upon an Overflow condition. FIFO_AUTORST should be pulled "High" to enable the automatic FIFO reset function.

3.5 Transmit Parallel Input to Serial Output (PISO)

The PISO is used to convert 622/666MHz parallel input data to 2.488/2.666GHz serial output data which can interface to an optical module. The PISO bit interleaves parallel input data into a serial bit stream taking the first bit from TXDI3P/N, then the first bit from TXDI2P/N, and so on as shown in Figure 10.

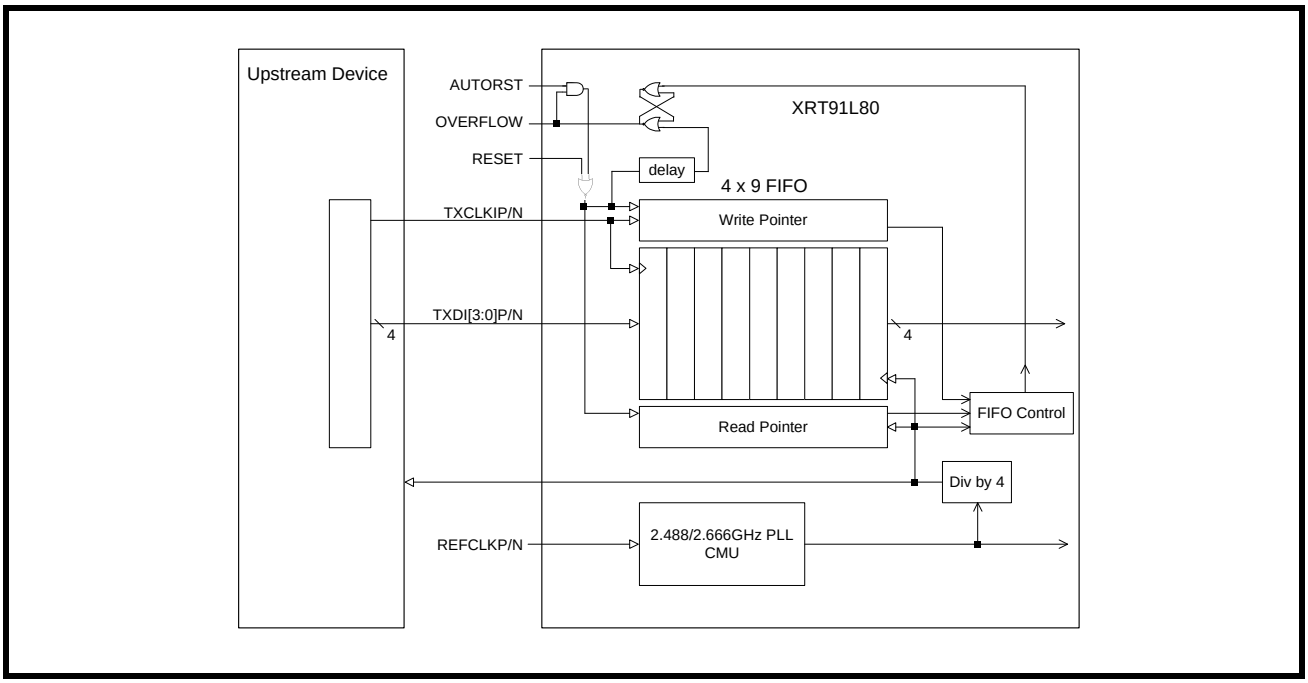
FIGURE 10. SIMPLIFIED BLOCK DIAGRAM OF PISO



3.6 Clock Multiplier Unit (CMU) and Re-Timer

The high-speed serial clock synthesized by the CMU is divided by 4, and the TXPCLKOP/N clock is presented to an upstream device. The upstream device should use TXPCLKOP/N as its timing source. The Upstream device then generates the TXCLKIP/N clock that is phase aligned with the transmit data and provides it to the parallel interface of the transmitter. The data must meet setup and hold times with respect to TXCLKIP/N. The XRT91L80 will latch TXDI[3:0]P/N on the rising edge of TXCLKIP/N. The clock synthesizer uses a PLL to lock to the differential input reference clock. It can also be driven by an optional external VCXO for loop timed or local reference de-jitter applications. As an example the REFCLKP/N input can accept a clock from a LVPECL crystal oscillator that has a frequency accuracy better than 20ppm in order for the TXCLKOP/N frequency to have the accuracy required for SONET systems. The other input, VCXO_INP/N can be connected to the output of a VCXO that can be configured to clean up the recovered received clock in loop timing mode before being applied to the input of the transmit CMU as a reference clock. In addition, the internal phase/frequency detector and charge pump, combined with an external VCXO can alternately be used as a jitter attenuator to de-jitter a noisy system reference clock prior to it being used to time the CMU. Figure 11 provides a detailed overview of the transmit FIFO in a system interface.

FIGURE 11. TRANSMIT FIFO AND SYSTEM INTERFACE



3.7 Loop Timing and clock control

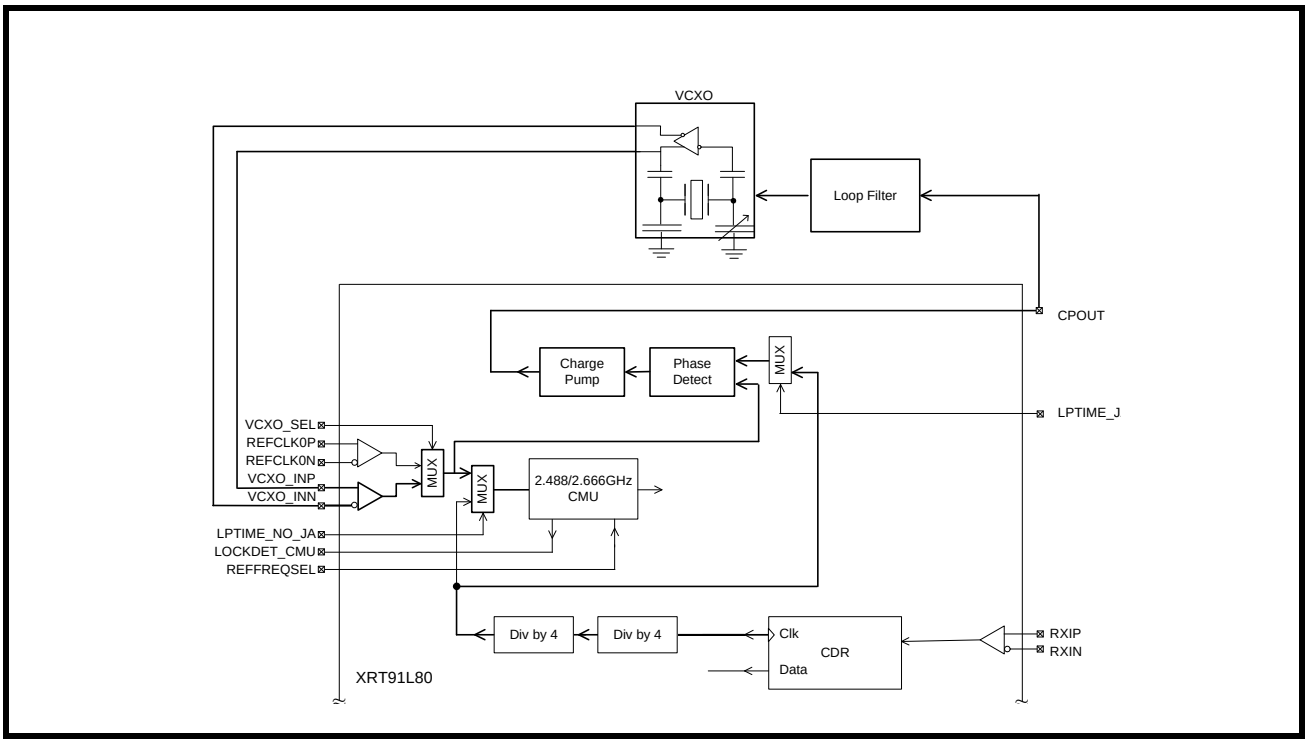
Two types of loop timing are possible in the XRT91L80. In the regular loop timing mode (without an external VCXO), the loop timing is controlled by the LPTIME_NO_JA pin. This mode is selected by asserting the LPTIME_NO_JA signal to a high level. When the loop timing mode is activated the external reference clock to the input of the CMU is replaced with the 1/16th or the 1/32nd of the high-speed recovered receive clock from the CDR. Under this condition both the transmit and receive sections are synchronized to the recovered receive clock. The normal looptime mode directly locks the CMU to the recovered receive clock with no external de-jittering.

In cases when the jitter of the recovered receive clock does not satisfy the strict ITU and Bellcore jitter generation requirements, an external VCXO-based PLL can be used to clean up the jitter of the recovered receive clock. In this case the VCXO_SEL pin should be set high. By doing so, the CMU receives its reference clock signal from an external VCXO connected to the VCXO_INP/N inputs. The LPTIME_JA pin must also be set high in order to select the recovered receive clock as the reference source for the de-jitter PLL. In this state, the VCXO will be phase locked to the recovered receive clock through a narrowband loop filter. The use of the on-chip phase/frequency detector with charge pump and an external VCXO to remove the transmit jitter due to jitter in the recovered clock is shown in Figure 11. The on-chip phase/frequency detector can also be used to remove the jitter from a noisy reference signal that is applied to the REFCLKP/N inputs. In this case the LPTIME_NO_JA pin should be set "Low", the VCXO_SEL set "High", and the LPTIME_JA pin set "Low". In this configuration, the REFCLKP/N signal is used as the reference to the de-jitter PLL and the de-jittered output of the phase locked VCXO is used as the timing reference to the CMU. Table 4 provides configuration for selecting the loop timing and reference de-jitter modes.

TABLE 4: LOOP TIMING AND REFERENCE DE-JITTER CONFIGURATIONS

VCXO_SEL	LPTIME_JA	LPTIME_NO_JA	ACTION
0	0	0	Normal mode
0	0	1	Loop timing without de-jitter
1	0	0	Reference de-jitter
1	1	0	Loop timing with de-jitter

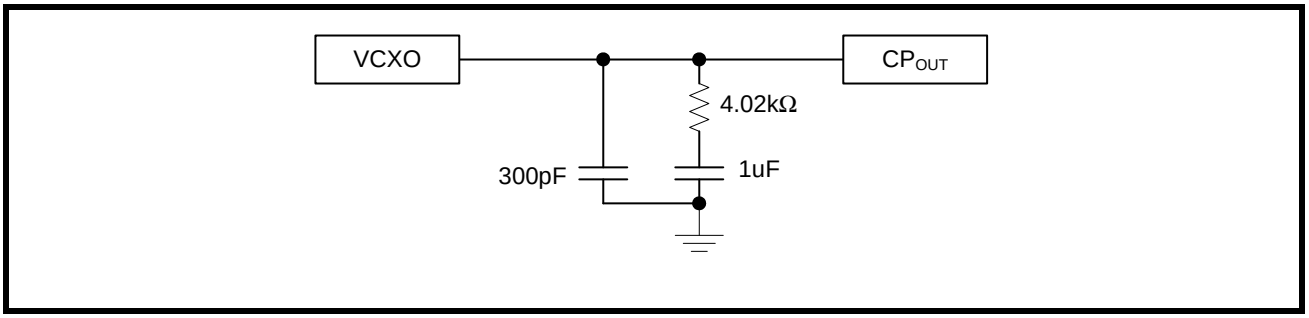
FIGURE 12. LOOP TIMING MODE USING AN EXTERNAL CLEANUP VCXO



3.8 External Loop Filter

As shown in Figure 12, there is an internal charge pump used to drive an external loop filter and external VCXO. The charge pump current is fixed at 250uA. Figure 13 is a simplified block diagram of the external loop filter and recommended values.

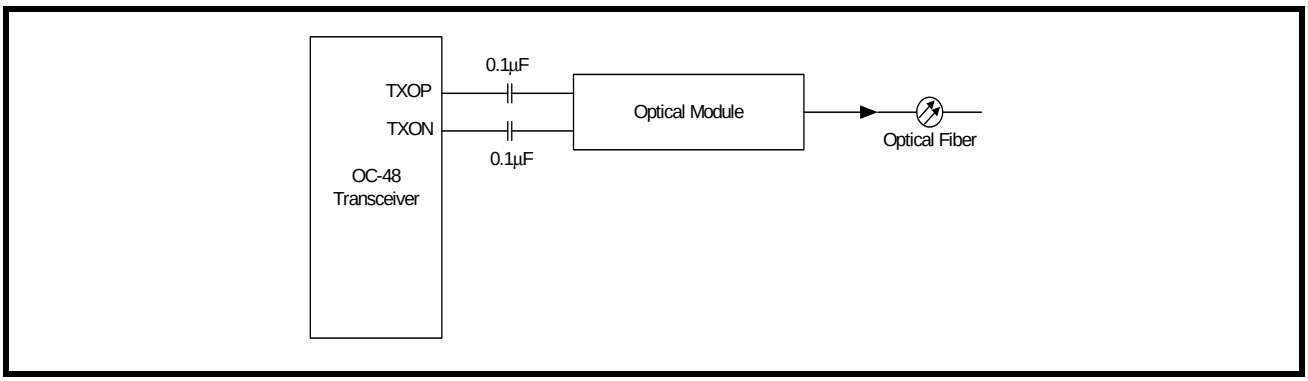
FIGURE 13. SIMPLIFIED DIAGRAM OF THE EXTERNAL LOOP FILTER



3.9 Transmit Serial Output Control

The 2.488/2.666GHz transmit serial output is avaliable on TXOP/N pins. The transmit serial output should be AC coupled to an optical module or electrical interface. A simplified block diagram is shown in Figure 14.

FIGURE 14. TRANSMIT SERIAL OUTPUT INTERFACE BLOCK



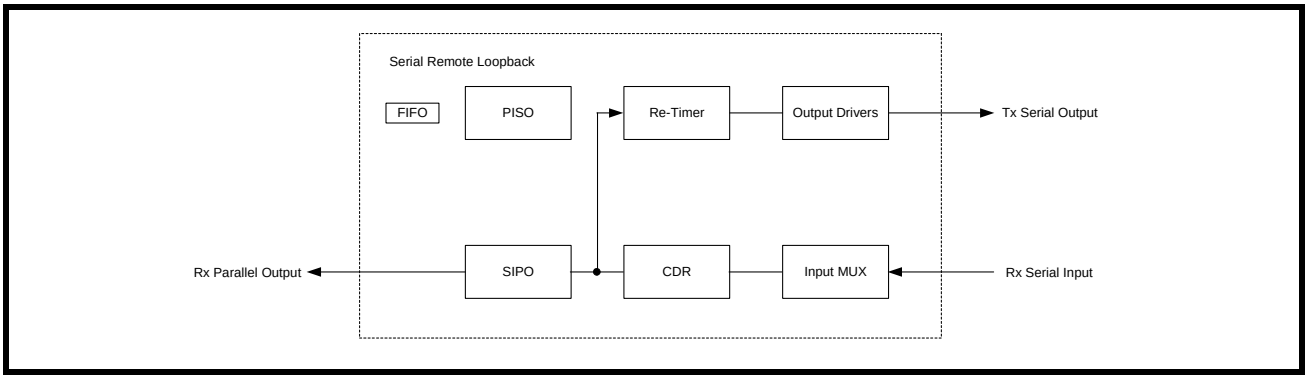
NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

4.0 DIAGNOSTIC FEATURES

4.1 Serial Remote Loopback

The serial remote loopback function is activated by setting RLOOPS "High". When serial remote loopback is activated, the high-speed serial receive data from RXIP/N is presented at the high speed transmit output TXOP/N, and the high-speed recovered clock is selected and presented to the high-speed transmit clock output TXCLKP/N. During serial remote loopback, the high-speed receive data (RXIP/N) is also converted to parallel data and presented at the low-speed receive parallel interface RXD[3:0]P/N. The recovered receive clock is also divided by 4 and presented at the low-speed clock output RXCLKP/N to synchronize the transfer of the 4-bit received parallel data. A simplified block diagram of serial remote loopback is shown in Figure 15.

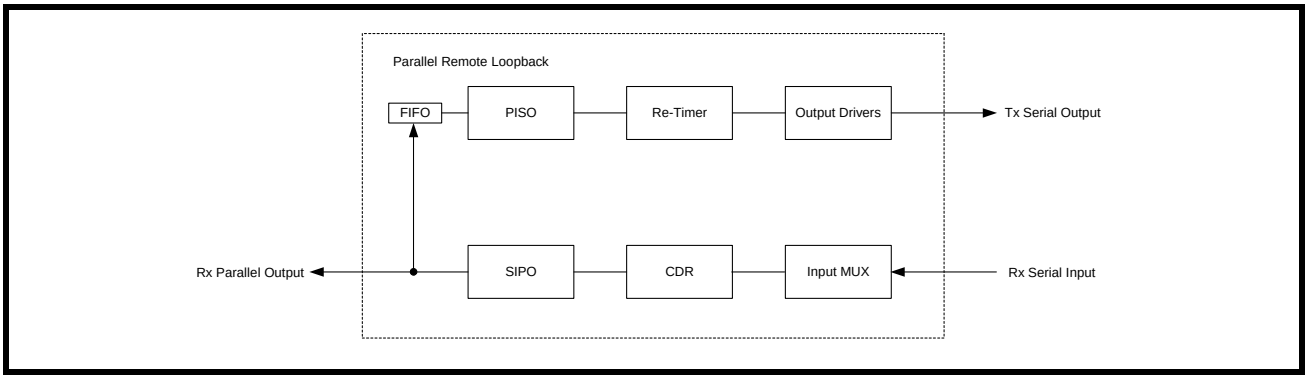
FIGURE 15. SERIAL REMOTE LOOPBACK



4.2 Parallel Remote Loopback

RLOOPP controls a more comprehensive version of remote loop-back that can also be used in conjunction with the de-jitter PLL that is phase locked to the recovered receive clock. In this mode, the received signal traverses the limiting amplifier, is processed by the CDR, and is sent through the serial to parallel converter. At this point, the 4-bit parallel data and clock are looped back to the transmit FIFO. Concurrently, if receive clock jitter attenuation is also employed, the received clock is divided down in frequency and presented to the input of the integrated phase/frequency detector and is compared to the frequency of a VCXO that is connected to the VCXO_INP/N inputs. With the LPTIME_JA configured to use the recovered receive clock as the reference and VCXO_SEL asserted, the VCXO is phase locked to the recovered receive clock. The de-jittered clock is then used to retime the transmitter, resulting in the re-transmission of the de-jittered received data out of TXOP/N. A simplified block diagram of parallel remote loopback is shown in Figure 16.

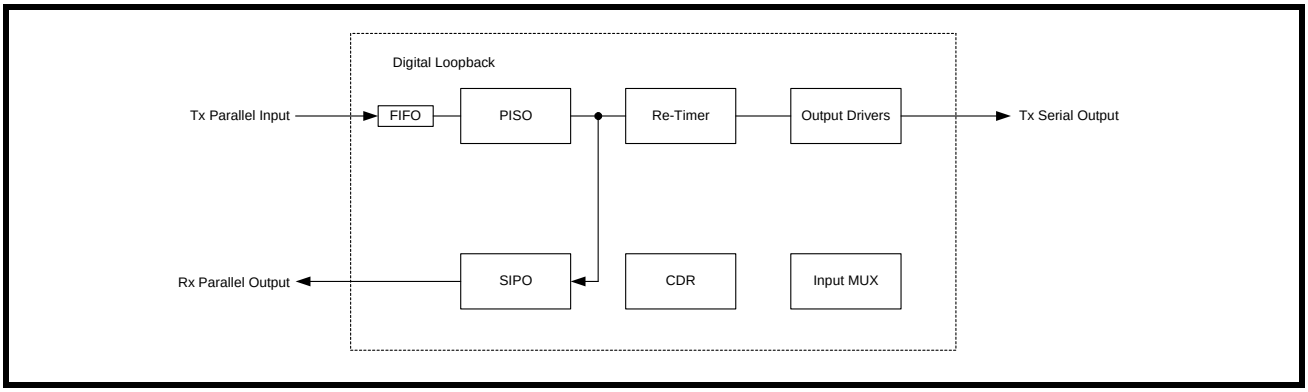
FIGURE 16. PARALLEL REMOTE LOOPBACK



4.3 Digital Local Loopback

The digital local loopback is activated when the DLOOP signal is set high. When digital local loopback is activated, the high-speed data from the output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The CMU output is also looped back to the receive section and is used to synchronize the transfer of the data through the receiver. In Digital loopback mode the transmit data from the transmit parallel interface TXDI[3:0]P/N is serialized and presented to the high-speed transmit output TXOP/N along with the high-speed transmit clock which is generated from the clock multiplier unit and presented to the TXO2P/N pins. A simplified block diagram of digital loopback is shown in Figure 17.

FIGURE 17. DIGITAL LOOPBACK



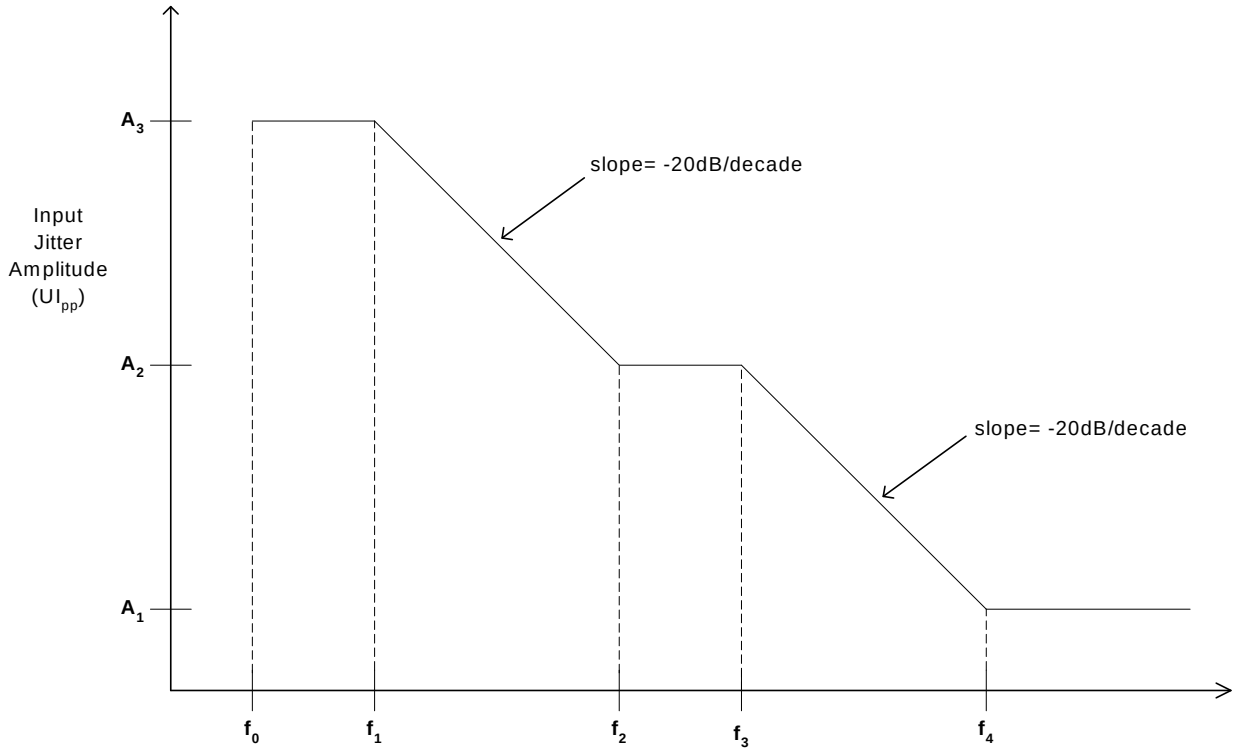
4.4 SONET Jitter Requirements

SONET equipment jitter requirements are specified for the following three types of jitter. The definitions of each of these types of jitter are given below. SONET equipment jitter requirements are specified for the following three types of jitter.

4.4.1 Jitter Tolerance:

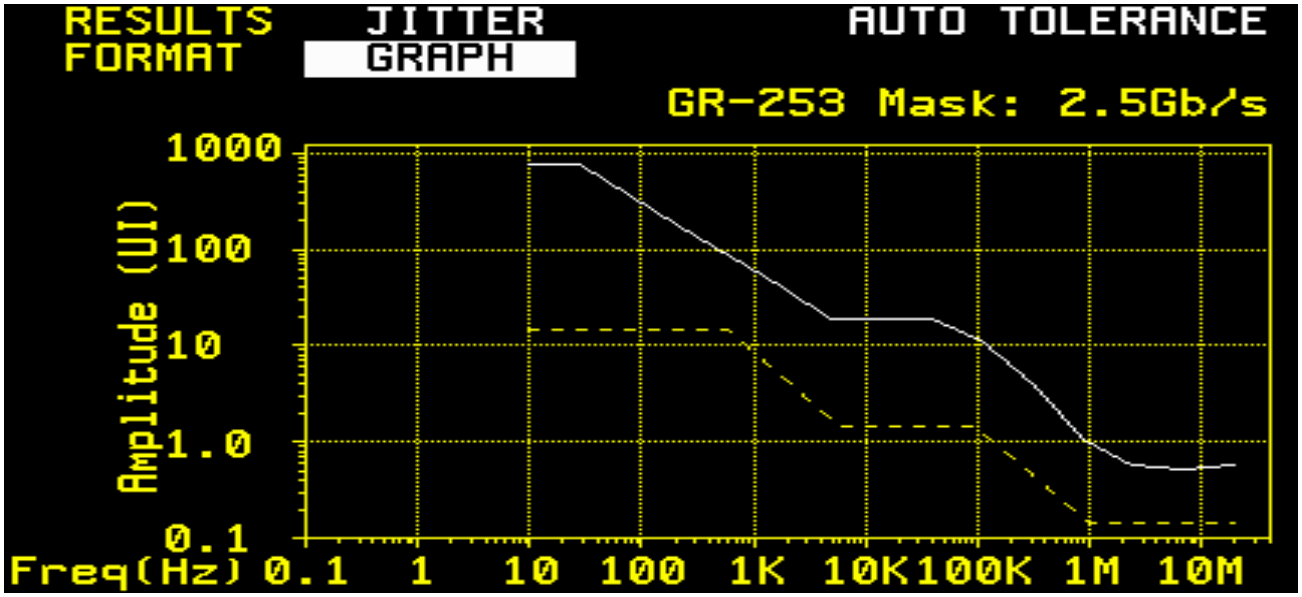
Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N equipment interface that causes an equivalent 1dB optical power penalty. OC-1/STS-1, OC-3/STS-3, OC-12 and OC-48 category II SONET interfaces should tolerate, the input jitter applied according to the mask of Figure 18, with the corresponding parameters specified in the figure.

FIGURE 18. JITTER TOLERANCE MASK



OC-N/STS-N LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
1	10	30	300	2K	20K	0.15	1.5	15
3	10	30	300	6.5K	65K	0.15	1.5	15
12	10	30	300	25K	250K	0.15	1.5	15
48	10	600	6000	100K	1000K	0.15	1.5	15

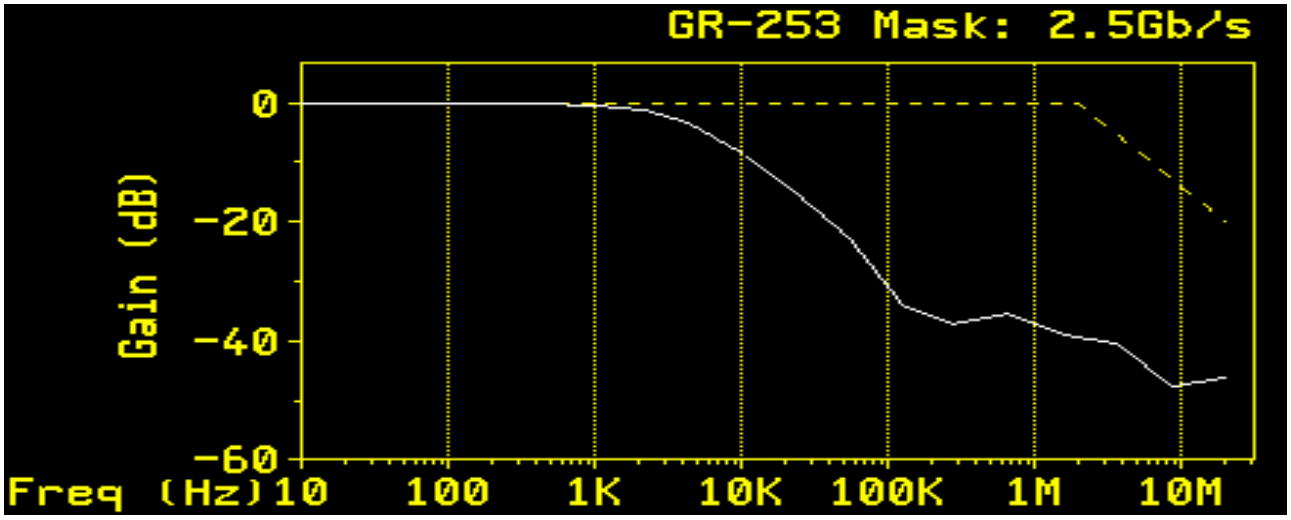
FIGURE 19. MEASURED JITTER TOLERANCE WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING.



4.4.2 Jitter Transfer

Jitter transfer is defined as the ratio of the jitter on the output of OC-N to the jitter applied on the input of OC-N versus frequency. Jitter transfer is important in applications where the system is utilized in the loop-timed mode, where the recovered clock is used as the source of the transmit clock.

FIGURE 20. MEASURED JITTER TRANSFER WITH EXTERNAL JITTER ATTENUATION ENABLED IN LOOPTIMING.

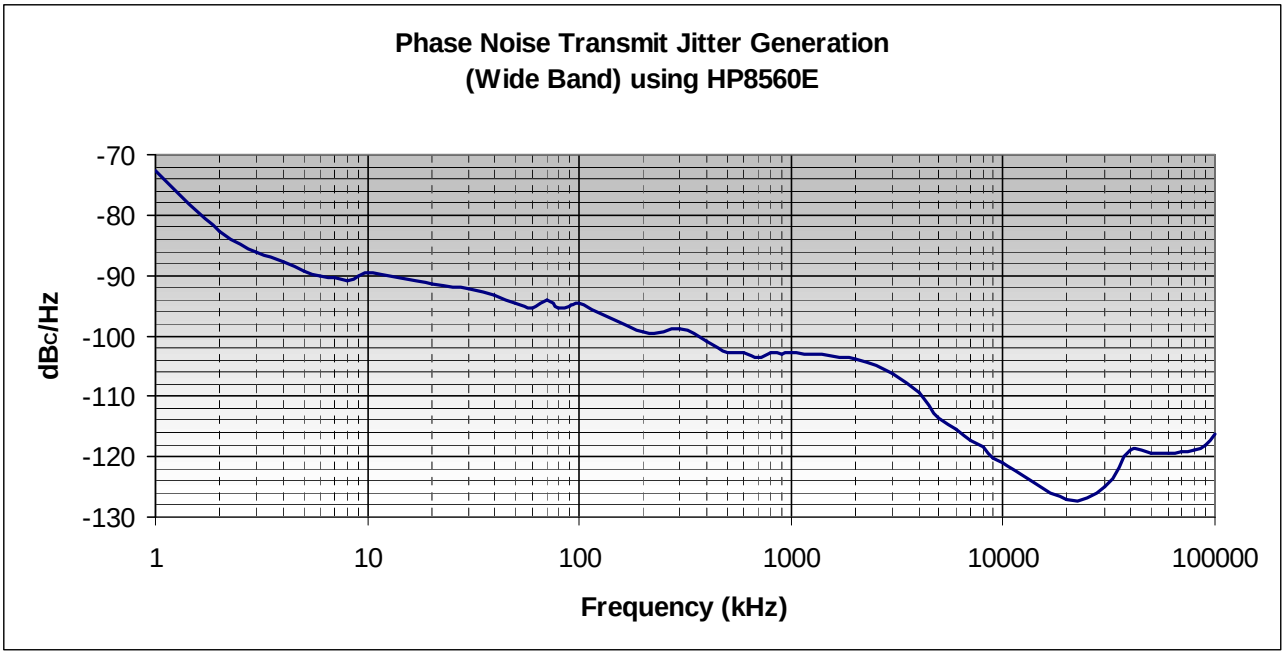


4.4.3 Jitter Generation

Jitter generation is defined as the amount of jitter at the OC-N output in the absence of applied input jitter. The Bellcore and ITU requirement for this type jitter is 0.01UI rms measured with a specific band-pass filter.

FIGURE 21. MEASURED PHASE NOISE TRANSMIT JITTER GENERATION AT 2.5 GBPS

Wide-band filter used in this test case.

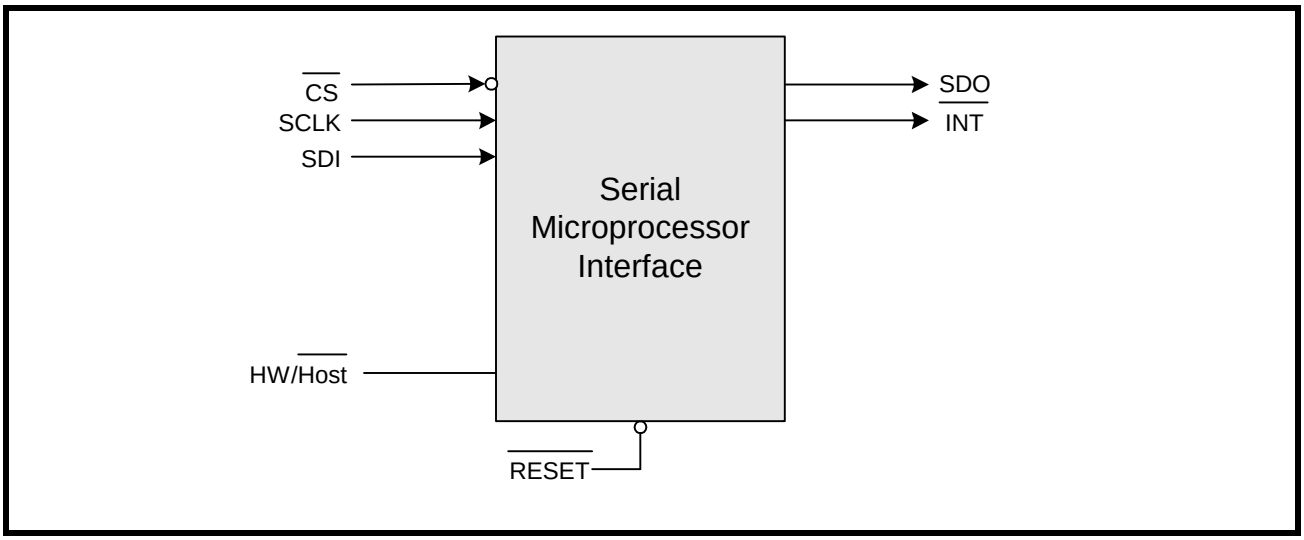


For more information on these specifications refer to Bellcore TR-NWT-000253 sections 5.6.2-5 and GR-253-CORE section 5.6.

5.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the transceiver. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the transceiver via an interrupt pin, and reset the transceiver to its default configuration by pulling reset "Low" for more than 10mS. A simplified block diagram of the Serial Microprocessor is shown in Figure 22.

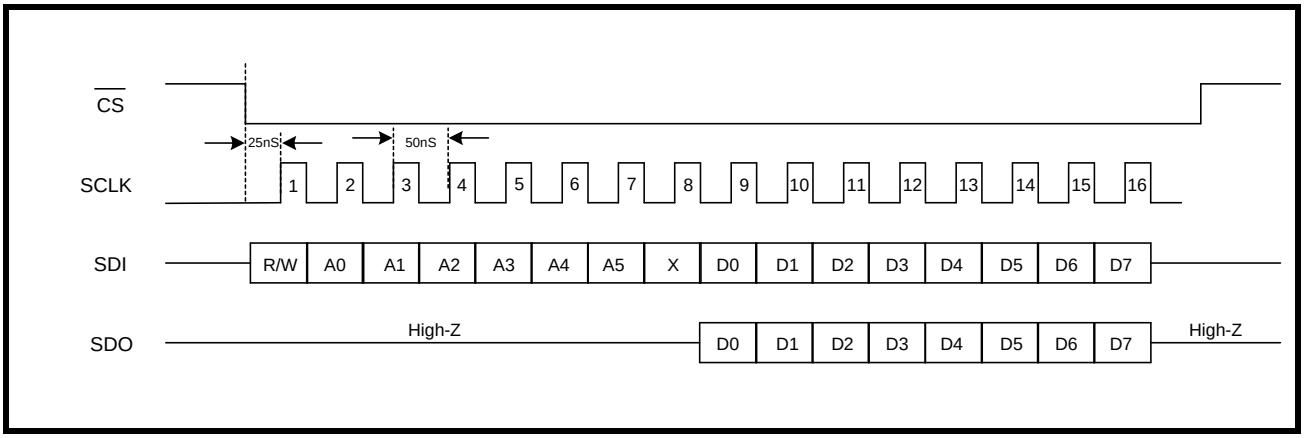
FIGURE 22. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



5.1 SERIAL TIMING INFORMATION

The serial port requires 16 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 16 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in Figure 23.

FIGURE 23. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: *The serial microprocessor interface does **NOT** support "burst write" or "burst read" operations. Chip Select (active "Low") **must be de-asserted** at the end of every single write or single read operation.*

5.2 16-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the transceiver LSB first. The 16 bits of serial data are described below.

5.2.1 R/W (SCLK1)

The first serial bit applied to the transceiver informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to “0”, the microprocessor is configured for a Write operation. If the R/W bit is set to “1”, the microprocessor is configured for a Read operation.

5.2.2 A[5:0] (SCLK2 - SCLK7)

The next 6 SCLK cycles are used to provide the address to which a Read or Write operation will occur. A0 (LSB) must be sent to the transceiver first followed by A1 and so forth until all 6 address bits have been sampled by SCLK.

5.2.3 X (Dummy Bit SCLK8)

The dummy bit sampled by SCLK8 is used to allow sufficient time for the serial data output pin to update data if the readback mode is selected by setting R/W = “1”. Therefore, the state of this bit is ignored and can hold either “0” or “1” during both Read and Write operations.

5.2.4 D[7:0] (SCLK9 - SCLK16)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. D0 (LSB) must be sent to the transceiver first followed by D1 and so forth until all 8 data bits have been sampled by SCLK. Once 16 SCLK cycles have been complete, the transceiver holds the data until $\overline{CS}$ is pulled “High” whereby, the serial microprocessor latches the data into the selected internal register.

5.3 8-BIT SERIAL DATA OUTPUT DESCRIPTION

The serial data output is updated on the falling edge of SCLK9 - SCLK16 if R/W is set to “1”. D0 (LSB) is provided on SCLK9 to the SDO pin first followed by D1 and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

6.0 REGISTER MAP AND BIT DESCRIPTIONS

TABLE 5: MICROPROCESSOR REGISTER MAP

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Channel 0 Control Register (0x00h - 0x05h)										
0	0x00	R/W	Reserved	Reserved	Reserved	VCXOIE	LOSIE	CDRIE	CMUIE	FIFOIE
1	0x01	RUR	Reserved	Reserved	Reserved	VCXOIS	LOSIS	CDRIS	CMUIS	FIFOIS
2	0x02	RO	Reserved	Reserved	Reserved	VCXOD	LOSD	CDRD	CMUD	FIFOD
3	0x03	R/W	Reserved	REFREQSEL	Reserved	LOOPBW	VCXOSEL	TRITXCLK016	AUTORST	FIFORST
4	0x04	R/W	Reserved	POLARITY	LOOPTM	LPTIMJADIS	DISRD	TRIRXD	Reserved	VCXOLKEN
5	0x05	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	DLOOP	RLOOPS	RLOOPP
0x06 - 0x3D		R/W	**Reserved**							
62	0x3E	RO	**Device ID (See Bit Description)**							
63	0x3F	RO	**Revision ID (See Bit Description)**							

TABLE 6: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X00H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOIE	**Voltage Controlled External Oscillator Lock Interrupt Enable** "0" = Masks the VCXO Lock interrupt generation "1" = Enables Interrupt generation ***NOTE:*** *VCXOLKEN must be enabled for this bit to be functional.*	R/W	0
D3	LOSIE	**Loss of Signal Interrupt Enable** "0" = Masks the LOS interrupt generation "1" = Enables Interrupt generation	R/W	0
D2	CDRIE	**Clock and Data Recovery Lock Interrupt Enable** "0" = Masks the CDR Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D1	CMUIE	**Clock Multiplier Unit Lock Interrupt Enable** "0" = Masks the CMU Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D0	FIFOIE	**FIFO Overflow Interrupt Enable** "0" = Masks the FIFO Overflow interrupt generation "1" = Enables Interrupt generation	R/W	0

TABLE 7: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X01H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOIS	**Voltage Controlled External Oscillator Lock Interrupt Status** An external interrupt will not occur unless the VCXOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in VCXO Lock Status Occurred ***NOTE:*** *VCXOLKEN must be enabled for this bit to be functional.*	RUR	0
D3	LOSIS	**Loss of Signal Interrupt Status** An external interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in LOS Status Occurred	RUR	0
D2	CDRIS	**Clock and Data Recovery Lock Interrupt Status** An external interrupt will not occur unless the CDRIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CDR Lock Status Occurred	RUR	0
D1	CMUIS	**Clock Multiplier Unit Lock Interrupt Status** An external interrupt will not occur unless the CMUIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CMU Lock Status Occurred	RUR	0
D0	FIFOIS	**FIFO Overflow Interrupt Status** An external interrupt will not occur unless the FIFOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in FIFO Overflow Status Occurred	RUR	0

TABLE 8: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X

CHANNEL 0 CONTROL REGISTER (0X02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D5	Reserved	This Register Bit is Not Used	X	X
D4	VCXOD	**Voltage Controlled External Oscillator Lock Detection** The VCXOD is used to indicate whether the internal clock reference is locked to an external VCO. "0" = VCXO currently not Locked "1" = VCXO Locked ***NOTE:*** *VCXOLKEN must be enabled for this bit to be functional.*	RO	0
D3	LOSD	**Loss of Signal Detection** The LOSD indicates the LOS activity. "0" = No Alarm "1" = A LOS condition is present	RO	0
D2	CDRD	**Clock and Data Recovery Lock Detection** The CDRD is used to indicate that the CDR is locked. "0" = CDR Out of Lock "1" = CDR Locked	RO	0
D1	CMUD	**Clock Multiplier Unit Lock Detection** The CMUD is used to indicate that the CMU is locked. "0" = CMU Out of Lock "1" = CMU Locked	RO	0
D0	FIFOD	**FIFO Overflow Detection** The FIFOD indicates that the FIFO is experiencing an overflow condition. "0" = No Alarm "1" = A FIFO Overflow condition is present	RO	0

TABLE 9: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X03H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	Reserved - Set to 0	R/W	0
D6	REFREQSEL	**Input Reference Frequency Select** This bit is used to select the input clock reference. "0" = 77.76/83.3 MHz "1"= 155.52/166 MHz	R/W	0
D5	Reserved	Reserved - Set to 0	R/W	0
D4	LOOPBW	**CMU Loop Band Width Select** This bit is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. "0" = Narrow Band (1x) "1" = Wide Band (4x)	R/W	0

TABLE 9: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X03H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	VCXOSEL	**VCXO De-Jitter Select** This bit selects either the normal REFCLK or the de-jitter VCXO as a reference clock. "0" = Normal REFCLK Mode "1" = De-Jitter VCXO Mode	R/W	0
D2	TRITXCLKO16	**Auxillary Output Clock Tri-State** This bit is used to tri-state the auxillary clock. "0" = TXCLKO16 Enabled "1" = TXCLKO16 Tri-State	R/W	0
D1	AUTORST	**Automatic FIFO Overflow Reset** If this bit is set to "1", the OC-48 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by setting FIFO_RST to "1" for 10 cycles of TXCLK. "0" = Manual FIFO reset required for overflow conditions "1" = Automatically resets FIFO upon overflow detection	R/W	0
D0	FIFORST	**Manual FIFO Reset** FIFORST should be set to "1" for 10 cycles of TXCLK during power-up in order to flush out the FIFO. Upon an interrupt indication that the FIFO has an overflow condition, this bit is used to reset or flush out the FIFO. "0" = Normal Operation "1" = Manual FIFO Reset ***NOTE:*** *To automatically reset the FIFO, see the AUTORST bit.*	R/W	0

TABLE 10: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X04H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	POLARITY	**Polarity for LOS Input Select** LOSEXT and POLARITY bits will be Exlussive NORed internally to generate the correct polarity.	R/W	0
D5	LOOPTM_JA	**Loop Timing With Jitter Attenuation** The LOOPTM_JA bit must be set to "1" in order to select the recovered receive clock as the reference source for the de-jitter PLL. "0" = Disabled "1" = Enabled	R/W	0

CHANNEL 0 CONTROL REGISTER (0X04H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D4	LPTIMJADIS	**Loop Timing With No Jitter Attenuation** When the loop timing mode is activated the external reference clock to the input of the CMU is replaced with the 1/16th or the 1/32nd of the high-speed recovered receive clock from the CDR. "0" = Disabled "1" = Loop timing Activated	R/W	0
D3	DISRD	**Receive Output Disable Upon LOS** If this bit is set to "1", the receive output data will automically pull "Low" when a LOS condition occurs. "0" = Disabled "1" = Mute Data Upon LOS	R/W	0
D2	TRIRXD	**Receive Output Tri-State** This bit is used to control the activity of the 4-bit parallel receive output bus and its reference clock. "0" = Normal Mode "1" = Tri-State RXDP/N[3:0] and RXCLK	R/W	0
D1	Reserved	Reserved - Set to 0	R/W	0
D0	VCXOLKEN	**De-Jitter PLL Lock Detect Enable** This bit enables the VCXO lock detect Pin N8 to be active. "0" = VCXO_LOCK disabled "1" = VCXO_LOCK enabled	R/W	0

TABLE 11: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

CHANNEL 0 CONTROL REGISTER (0X05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	Reserved	This Register Bit is Not Used	X	X
D3	Reserved	This Register Bit is Not Used	X	X
D2	DLOOP	**Digital Loopback** Digital loopback allows the Transmit input pins to be looped back to the Receive output pins for local diagnostics. The Transmit serial output data is valid during the digital loopback. "0" = Disabled "1" = Enable DLOOP ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*	R/W	0

CHANNEL 0 CONTROL REGISTER (0X05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	RLOOPS	**Serial Remote Loopback** Serial remote loopback allows the Receive serial input pins to be looped back to the Transmit serial output pins for remote diagnostics. The Receive output data is valid during a serial remote loopback. "0" = Disabled "1" = Enable RLOOPS ***NOTE:*** *DLOOP and RLOOPS can be enabled simultaneously to achieve a dual loopback diagnostic feature.*	R/W	0
D0	RLOOPP	**Parallel Remote Loopback** Parallel remote loopback has the same affect as the serial remote loopback, except that the input data is allowed to pass through the SIPO before it's looped back to the Transmit path, wherein it passes through the Transmit FIFO, through the PISO, and back out the Transmit serial output. The Receive output data is valid during a serial remote loopback. "0" = Disabled "1" = Enable RLOOPP ***NOTE:*** *DLOOP and RLOOPS should be **disabled** when RLOOPP is enabled.*	R/W	0

TABLE 12: MICROPROCESSOR REGISTER 0X3EH BIT DESCRIPTION

DEVICE "ID" REGISTER (0X3EH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6 D5 D4 D3 D2 D1 D0	Device "ID"	The device "ID" of the XRT91L80 LIU is 0xC0h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1 1 0 0 0 0 0 0

TABLE 13: MICROPROCESSOR REGISTER 0X3FH BIT DESCRIPTION

REVISION "ID" REGISTER (0X3FH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6 D5 D4 D3 D2 D1 D0	Revision "ID"	The revision "ID" of the XRT91L80 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon (Revision A) will be 0x01h.	RO	This byte shows the revision of the device.

7.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply..... -0.5V to +3.465V	Power Dissipation STBGA Package..... TBD
Storage Temperature .....-65℃ to 150℃	Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40℃ t o 85℃	ESD Protection (HBM)..... .....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V	Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25℃, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{DD}		Power Supply Current		TBD		mA	
I_{LL}		Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{HL}	TTL	Input High Voltage	2.0			V	
V_{IL}	TTL	Input Low Voltage			0.8	V	
V_{IDIFF}	Analog	Input Differential Voltage	0.2		1	V	AC Coupled
V_{COMM}	Analog	Common Mode Voltage	1		2	V	
V_{ICOMM}	LVDS	Input LVDS Common Mode Voltage	0.5		2	V	
V_{IAMP}	LVDS	Input LVD Voltage	0.1			V	
V_{ICOMM}	PECL	Input PECL Common Mode Voltage	1.5		2	V	Terminate with 50Ω to V_{CC}-2
V_{IAMP}	PECL	Input PECL Voltage	0.2			V	Terminate with 50Ω to V_{CC}-2
V_{OH}	TTL	Output High Voltage	2			V	
V_{OL}	TTL	Output Low Voltage			0.8	V	
V_{OH}	LVDS	Output LVDS High Voltage	1.35			V	Differential Termination, 100Ω
V_{OL}	LVDS	Output LVDS Low Voltage			1.15	V	Differential Termination, 100Ω
V_{OAMP}	CML	Output Common Mode Logic Voltage	0.4		0.6	V	AC Coupled, 50Ω to GND

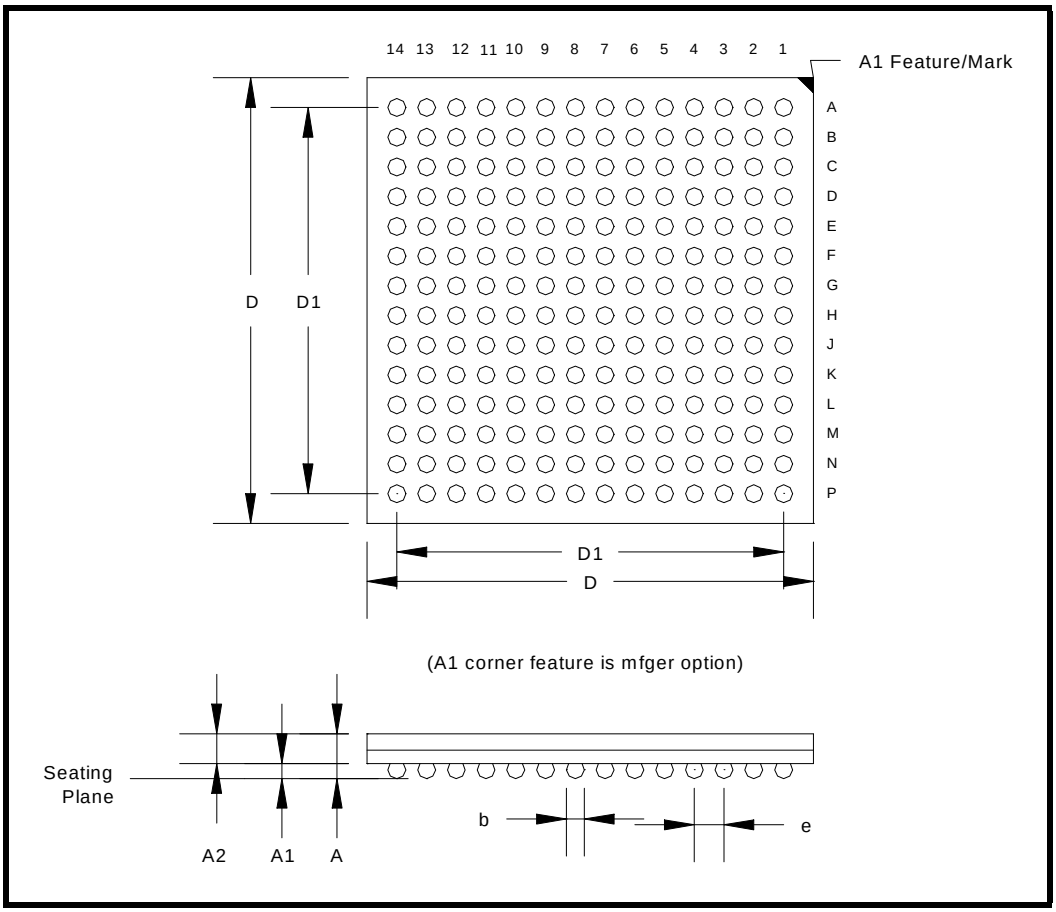
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L80IB	196 Shrink Thin Ball Grid Array (12.0 mm x 12.0 mm, STBGA)	-40°C to +85°C

196 SHRINK THIN BALL GRID ARRAY

(12.0 MM X 12.0 MM, STBGA)

REV. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.067	1.35	1.70
A1	0.010	0.022	0.25	0.55
A2	0.033	0.052	0.85	1.31
D	0.465	0.480	11.80	12.20
D1	0.409 BSC		10.40 BSC	
b	0.018	0.022	0.45	0.55
e	0.031 BSC		0.80 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	October 2004	1st release of the XRT91L80 product brief
P1.0.1	October 2004	Fixed typos throughout document
P1.0.2	October 2004	Fixed typos throughout document
P1.0.3	January 2005	Added jitter transfer and tolerance mask test results and phase noise transmit jitter generation results, added $\overline{CS}$ de-assertion note on section 5.1, fixed register 0x02, 0x04, 0x05 microprocessor bit descriptions, updated pin descriptions, corrected 'falling edge' typo in section 3.7 to 'rising edge', and enhanced receive and transmit interface block diagrams.
P1.0.4	March 2005	Remove 'RXSEL' reference on the RXIP/N pin description. Minor edit in receive section 2.0. FIFO_RST corrected for active High in section 3.4. Removed unsupported note for transparent mode FIFO operation in section 3.3.