

SOT-23 Formed SMD Package

CSC2712

SILICON PLANAR EPITAXIAL TRANSISTOR

N-P-N transistor

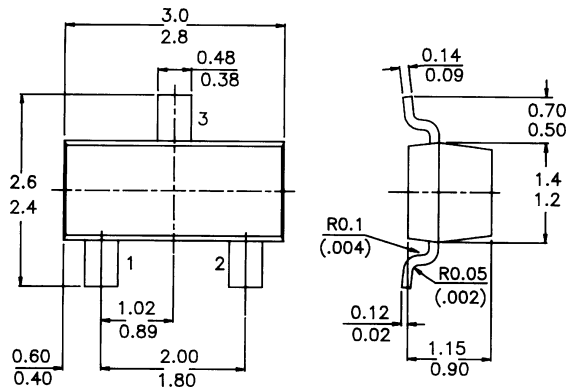
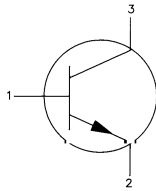
Marking

CSC2712Y=1E
CSC2712GR(G)=1F
CSC2712BL(L)=1G

PACKAGE OUTLINE DETAILS
ALL DIMENSIONS IN mm

Pin configuration

1 = BASE
2 = EMITTER
3 = COLLECTOR



ABSOLUTE MAXIMUM RATINGS

Collector-base voltage (open emitter)	V_{CBO}	max.	60 V
Collector-emitter voltage (open base)	V_{CEO}	max.	50 V
Emitter-base voltage (open collector)	V_{EBO}	max.	5 V
Collector current (peak value)	I_C	max.	150 mA
Total power dissipation at $T_{amb} = 25^\circ C$	P_{tot}	max.	150 mW
Junction temperature	T_j	max.	150 °C
D.C. current gain	h_{FE}	min.	70
		max.	700
Transition frequency	f_T	min.	80 MHz
$I_C = 1 \text{ mA}; V_{CE} = 10 \text{ V}$			
Noise figure at $R_S = 10 \text{ K}\Omega$	F	max.	10 dB
$I_C = 0.1 \text{ mA}; V_{CE} = 6 \text{ V};$			
$f = 1 \text{ kHz}$			

RATINGS (at $T_A = 25^\circ\text{C}$ unless otherwise specified)*Limiting values*

Collector-base voltage (open emitter)	V_{CB0}	max.	60 V
Collector-emitter voltage (open base)	V_{CEO}	max.	50 V
Emitter-base voltage (open collector)	V_{EBO}	max.	5 V
Collector current (d.c.)	I_C	max.	150 mA
Base current	I_B	max.	30 mA
Total power dissipation at $T_{amb} = 25^\circ\text{C}$	P_{tot}	max.	150 mW
Junction temperature	T_j	max.	150 °C
Storage temperature	T_{stg}		-50 to +150 °C

CHARACTERISTICS (at $T_A = 25^\circ\text{C}$ unless otherwise specified)*Collector cut-off current*

$I_E = 0; V_{CB} = 60\text{ V}$	I_{CBO}	max.	100 nA
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Emitter cut-off current

$I_C = 0; V_{EB} = 5\text{ V}$	I_{EBO}	max.	100 nA
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Saturation voltage

$I_C = 100\text{ mA}; I_B = 10\text{ mA}$	V_{CEsat}	max.	250 mV
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D.C. current gain

$I_C = 2\text{ mA}; V_{CE} = 6\text{ V}$	h_{FE}	min.	70
		max.	700
	Y	min.	120
		max.	240
	$GR(G)$	min.	200
		max.	400
	$BL(L)$	min.	350
		max.	700

Transition frequency

$I_C = 1\text{ mA}; V_{CE} = 10\text{ V}$	f_T	min.	80 MHz
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Noise figure at $R_g = 10\text{ k}\Omega$

$V_{CE} = 6\text{ V}; I_C = 0.1\text{ mA}$	N_F	max.	10 dB
$f = 1\text{ kHz}$			

Notes

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Discrete Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished on the CDIL Web Site/ CD is believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Discrete Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

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