

IS42S8800/IS42S8800L

IS42S16400/IS42S16400L



2(1)M Words x 8(16) Bits x 4 Banks (64-MBIT)
SYNCHRONOUS DYNAMIC RAM

FEATURES

- Single 3.3V ($\pm 0.3V$) power supply
- High speed clock cycle time -7: 133MHz<3-3-3>, -8: 100MHz<2-2-2>
- Fully synchronous operation referenced to clock rising edge
- Possible to assert random column access in every cycle
- Quad internal banks controlled by A12 & A13 (Bank Select)
- Byte control by LDQM and UDQM for IS42S16400
- Programmable Wrap sequence (Sequential / Interleave)
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable /CAS latency (2 and 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- X8, X16 organization
- LVTTL compatible inputs and outputs
- 4,096 refresh cycles / 64ms
- Burst termination by Burst stop and Precharge command
- Package 400mil 54-pin TSOP-2

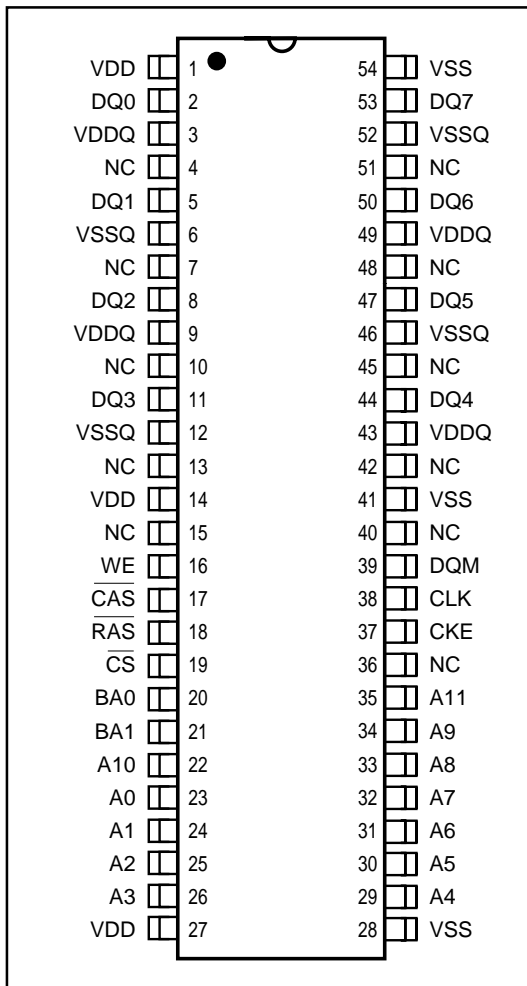
DESCRIPTION

The IS42S8800 and IS42S16400 are high-speed 67, 108,864-bit synchronous dynamic random-access memories, organized as 2,097,152 x 8 x 4 and 1,048,576 x 16 x 4 (word x bit x bank), respectively.

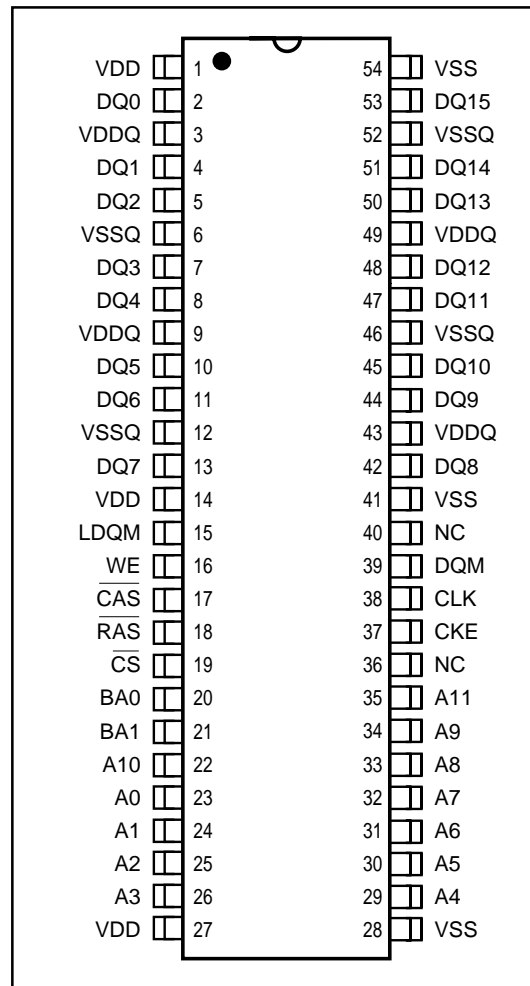
The synchronous DRAMs achieved high-speed data transfer using the pipeline architecture and clock frequency up to 133MHz for -7. All input and outputs are synchronized with the positive edge of the clock. The synchronous DRAMs are compatible with Low Voltage TTL (LVTTL). These products are packaged in 54-pin TSOP-2.

PIN CONFIGURATIONS

54-Pin TSOP-2 (IS42S8800)



54-Pin TSOP-2 (IS42S16400)

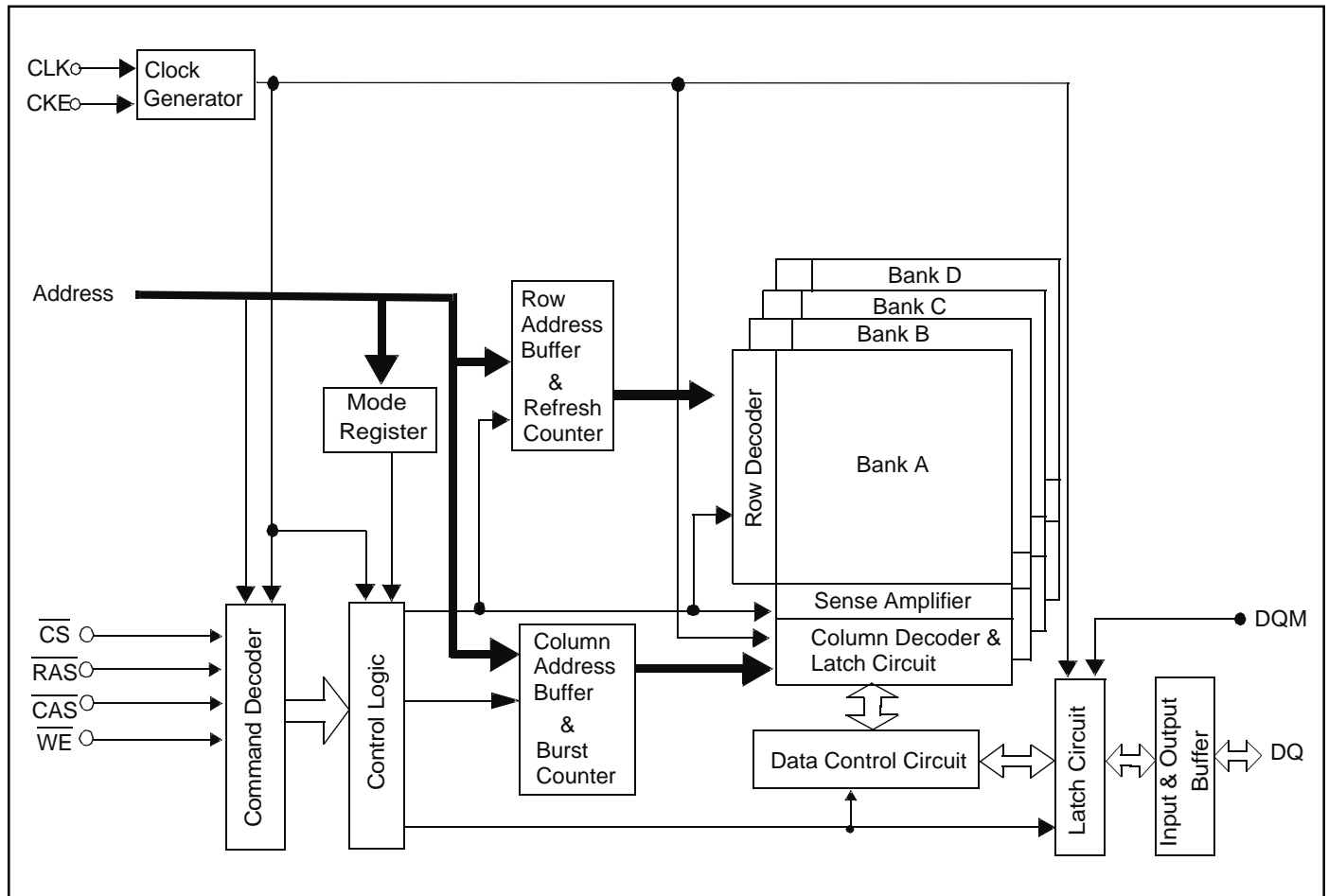


PIN DESCRIPTIONS

| | |
|------------|-----------------------|
| CLK | Master Clock |
| CKE | Clock Enable |
| CS | Chip Select |
| RAS | Row Address Strobe |
| CAS | Column Address Strobe |
| WE | Write Enable |
| DQ0 ~ DQ15 | Data I/O |

| | |
|-------|---------------------|
| DQM | DQ Mask Enable |
| A0-11 | Address Input |
| BA0,1 | Bank Address |
| VDD | Power Supply |
| VDDQ | Power Supply for DQ |
| VSS | Ground |
| VSSQ | Ground for DQ |

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

| Symbol | Type | Function (In Detail) |
|-------------------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK | Input Pin | Maste Clock: Other inputs signals are referenedc to the CLK rising edge |
| CKE | Input Pin | Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals,device input buffers and output drivers. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). |
| \overline{CS} | Input Pin | Chip Select: \overline{CS} enables (registered LOW) and disables (registered HIGH) the com-mand decoder. All commands are masked when \overline{CS} is registered HIGH. \overline{CS} provides for external bank selection on systems with multiple banks. \overline{CS} is considered part of the command code. |
| \overline{RAS} , \overline{CAS} , \overline{WE} | Input Pin | Command Inputs: \overline{RAS} , \overline{CAS} and \overline{WE} (along with \overline{CS}) define the command being entered. |
| A0-A11 | Input Pin | Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one loca-tion out of the memory array in the respec-tive bank. The row address is specified by A0-A11. The column address is specified by A0-A8 (IS42S8800) / A0-A7 (IS42S16400) |
| BA0,BA1 | Input Pin | Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. |
| DQM, UDQM ,LDQM | Input Pin | Address Inputs: Provide the row address for ACTIVE commands (row address A0-A10), and the column address and AUTO PRECHARGE bit for READ/WRITE com-mands (column address A0-A7 with A10 defining AUTO PRECHARGE), to select one location out of the memory array in the respective bank. |
| DQ0 to DQ15 | I/O Pin | IData Input / Output: Data bus. |
| V_{DD} , V_{SS} | Power Supply Pin | Power Supply for the memory array and peripheral circuitry. |
| V_{DDQ} , V_{SSQ} | Power Supply Pin | Power Supply are supplied to the output buffers only. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameters | Rating | Unit |
|------------------|---------------------------------------------------------------|-------------------------------|------|
| V _{DD} | Supply Voltage (with respect to V _{SS}) | -0.5 to +4.6 | V |
| V _{DDQ} | Supply Voltage for Output (with respect to V _{SSQ}) | -0.5 to +4.6 | V |
| V _I | Input Voltage (with respect to V _{SS}) | -0.5 to V _{DD} +0.5 | V |
| V _O | Output Voltage (with respect to V _{SSQ}) | -1.0 to V _{DDQ} +0.5 | V |
| I _O | Short circuit output current | 50 | mA |
| P _D | Power Dissipation (T _A = 25 °C) | 1 | W |
| T _{OPT} | Operating Temperature | 0 to +70 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

Notes:

1. Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC RECOMMENDED OPERATING CONDITIONS

(At T_A = 0 to +70°C unless otherwise noted)

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------------|------|------|-----------------------|------|
| V _{DD} | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{DDQ} | Supply Voltage for DQ | 0 | 0 | 0 | V |
| V _{SS} | Ground | 3.0 | 3.3 | 3.6 | V |
| V _{SSQ} | Ground for DQ | 0 | 0 | 0 | V |
| V _{IH} | High Level Input Voltage (all Inputs) | 2.0 | — | V _{DD} + 0.3 | V |
| V _{IL} | Low Level Input Voltage (all Inputs) | -0.3 | — | +0.8 | V |

CAPACITANCE CHARACTERISTICS

(At T_A = 0 ~ 70°C, V_{DD} = V_{DDQ} = 3.3 ± 0.3V, V_{SS} = V_{SSQ} = 0V, unless otherwise noted)

| Symbol | Parameter | Min. | Max. | Unit |
|------------------|------------------------------------------|------|------|------|
| C _{IN} | Input Capacitance, address & control pin | 2.5 | 3.8 | pF |
| C _{CLK} | Input Capacitance, CLK pin | 2.5 | 3.5 | pF |
| C _{I/O} | Data Input/Output Capacitance | 4.0 | 6.5 | pF |

DC ELECTRICAL CHARACTERISTICS

(At $T_A = 0 \sim 70^\circ\text{C}$, $V_{DD} = V_{DDQ} = 3.3 \pm 0.3\text{V}$, $V_{SS} = V_{SSQ} = 0\text{V}$, unless otherwise noted)

| Symbol | Parameter | Test Condition | Speed | Min. | Max. | Unit |
|------------------------------------|-------------------------------------------------------|------------------------------------------------------------------------------------|--------------|------|------|------|
| I _{CC1} ⁽¹⁾ | Operating Current | One Bank active, $\overline{\text{CAS}}$ latency = 3 | -7(42S8800) | — | 75 | mA |
| | | Burst Length=1 | -7(42S16400) | — | 70 | mA |
| | | t _{RC} = t _{RC} (min.) | -8(42S8800) | — | 85 | mA |
| | | t _{CLK} = t _{CLK} (min.) | -8(42S16400) | — | 80 | mA |
| I _{CC2P} | Precharge Standby Current (In Power-Down Mode) | CKE ≤ V _{IL} (MAX) t _{CK} = 15 ns | -7 | — | 2 | mA |
| | | | -8 | — | 2 | mA |
| I _{CC2PS} | | CKE ≤ V _{IL} (MAX) CLK ≤ V _{IL} (MAX) | -7 | — | 1 | mA |
| | | | -8 | — | 1 | mA |
| I _{CC2N} ⁽²⁾ | Precharge Standby Current (In Non Power-Down Mode) | CS ≥ V _{CC} -0.2V t _{CK} = 15 ns | -7 | — | 20 | mA |
| | | CKE ≥ V _{IH} (MIN) | -8 | — | 20 | mA |
| I _{CC2NS} | | CS ≥ V _{CC} -0.2V CKE ≤ V _{IL} (MAX) | -7 | — | 15 | mA |
| | | CKE ≥ V _{IH} (MIN) All input signals are stable. | -8 | — | 15 | mA |
| I _{CC3P} | Active Standby Current (In Power-Down Mode) | CKE ≤ V _{IL} (MAX) t _{CK} = 10 ns | -7 | — | 7 | mA |
| | | | -8 | — | 7 | mA |
| I _{CC3PS} | | CKE ≤ V _{IL} (MAX) CLK ≤ V _{IL} (MAX) | -7 | — | 5 | mA |
| | | | -8 | — | 5 | mA |
| I _{CC3N} ⁽²⁾ | Active Standby Current (In Non Power-Down Mode) | CS ≥ V _{CC} -0.2V t _{CK} = 15 ns | -7 | — | 30 | mA |
| | | CKE ≥ V _{IH} (MIN) | -8 | — | 30 | mA |
| I _{CC3NS} | | CS ≥ V _{CC} -0.2V CKE ≤ V _{IL} (MAX) | -7 | — | 25 | mA |
| | | CKE ≥ V _{IH} (MIN) All input signals are stable. | -8 | — | 25 | mA |
| I _{CC4} | Operating Current (In Burst Mode) | All Banks active $\overline{\text{CAS}}$ latency = 3 | -7(42S8800) | — | 90 | mA |
| | | Burst Length=1 | -7(42S16400) | — | 70 | mA |
| | | t _{CK} = t _{CK} (MIN) | -8(42S8800) | — | 100 | mA |
| | | | -8(42S16400) | — | 80 | mA |
| I _{CC5} | Auto-Refresh Current | t _{RC} = t _{RC} (MIN) | -7 | — | 130 | mA |
| | | t _{CLK} = t _{CLK} (MIN) | -8 | — | 110 | mA |
| I _{CC6} ^(3, 4) | Self-Refresh Current | CKE ≤ 0.2V | -7 | — | 1 | mA |
| | | | -8 | — | 1 | mA |
| | | | -7L | — | 0.5 | mA |
| | | | -8L | — | 0.5 | mA |
| I _{IL} | Input Leakage Current (Inputs) | 0V ≤ V _{IN} ≤ V _{DD} (MAX) Pins not under test = 0V | | -5 | 5 | μA |
| I _{OL} | Output Leakage Current (I/O pins) | Output is disabled DQ# in H - Z., 0V ≤ V _{OUT} ≤ V _{DD} (MAX) | | -5 | 5 | μA |
| V _{OH} | High Level Output Voltage | I _{OUT} = -2 mA | | 2.4 | — | V |
| V _{OL} | Low Level Output Voltage | I _{OUT} = +2 mA | | — | 0.4 | V |

Notes:

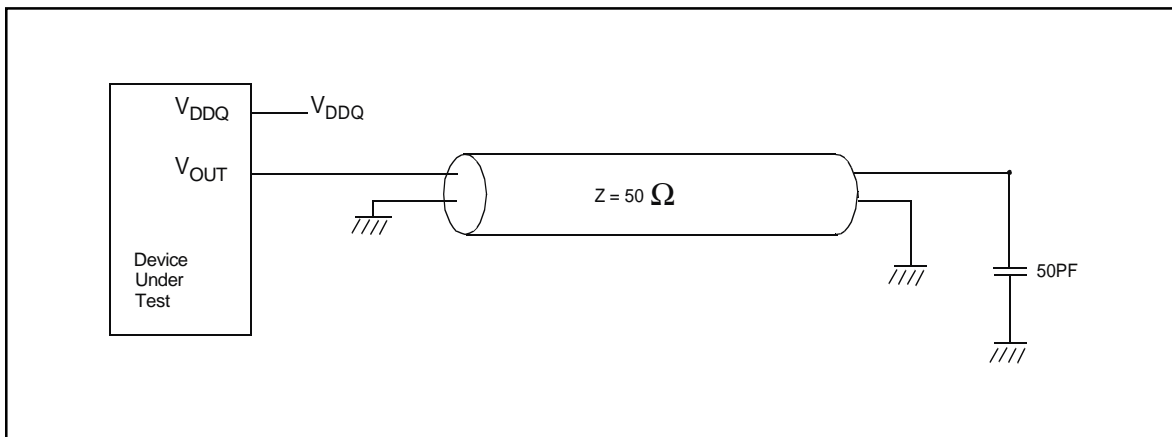
1. I_{CC}(max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.
3. Normal version: IS42S8800/IS42S16400
4. Low power version: IS42S8800L/IS42S16400L

AC TEST CONDITIONS

(At $T_A = 0 \sim 70^\circ\text{C}$, $V_{DD} = V_{DDQ} = 3.3 \pm 0.3\text{V}$, $V_{SS} = V_{SSQ} = 0\text{V}$, unless otherwise noted)

| Parameter | Rating | Unit |
|-------------------------------------------------------------|-----------|------|
| AC input Levels (V_{IH} / V_{IL}) | 2.0 / 0.8 | V |
| Input timing reference level /Output timing reference level | 1.4 | V |
| Input rise and fall time | 1 | ns |
| Output load condition | 50 | pF |

Output Load Conditions



AC ELECTRICAL CHARACTERISTICS

(At $T_A = 0 \sim 70^\circ\text{C}$, $V_{DD} = V_{DDQ} = 3.3 \pm 0.3\text{V}$, $V_{SS} = V_{SSQ} = 0\text{V}$, unless otherwise noted)

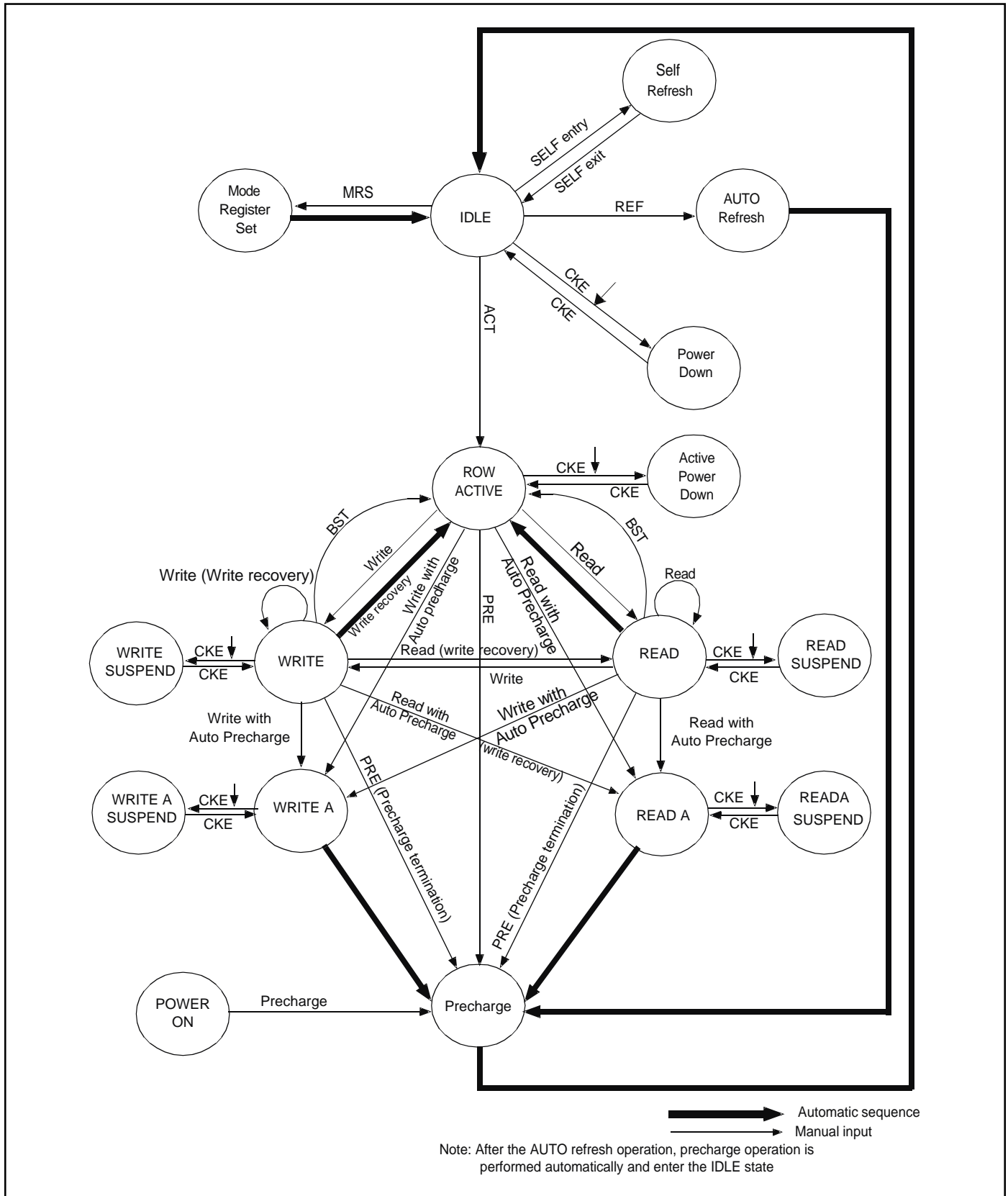
| Symbol | Parameter | | -7 | | -8 | | Units |
|------------------|----------------------------------------------------------|-------------------------------------|------|---------|------|---------|-------|
| | | | Min. | Max. | Min. | Max. | |
| t _{ck3} | CLK Cycle Time | $\overline{\text{CAS}}$ Latency = 3 | 7.5 | — | 10 | — | ns |
| t _{ck2} | | $\overline{\text{CAS}}$ Latency = 2 | 10 | — | 10 | — | ns |
| t _{ac3} | CLK to valid output delay ⁽¹⁾ | $\overline{\text{CAS}}$ Latency = 3 | — | 5.4 | — | 6 | ns |
| t _{ac2} | | $\overline{\text{CAS}}$ Latency = 2 | — | 6 | — | 6 | ns |
| t _{ch} | CLK high pulse width | | 2.5 | — | 3 | — | ns |
| t _{cl} | CLK low pulse width | | 2.5 | — | 2.5 | — | ns |
| t _{cke} | CKE setup time | | 1.5 | — | 2 | — | ns |
| t _{ckh} | CKE hold time | | 0.8 | — | 1 | — | ns |
| t _{as} | Address setup time | | 1.5 | — | 2 | — | ns |
| t _{ah} | Address hold time | | 0.8 | — | 1 | — | ns |
| t _{cms} | Command setup time | | 1.5 | — | 2 | — | ns |
| t _{cmh} | Command hold time | | 0.8 | — | 1 | — | ns |
| t _{ds} | Data input setup time | | 1.5 | — | 2 | — | ns |
| t _{dH} | Data input hold time | | 0.8 | — | 1 | — | ns |
| t _{oh3} | Output data hold time ⁽¹⁾ | $\overline{\text{CAS}}$ Latency = 3 | 2.7 | — | 3 | — | ns |
| t _{oh2} | | $\overline{\text{CAS}}$ Latency = 2 | 3 | — | 3 | — | ns |
| t _{lZ} | CLK to output in low - Z | | 0 | — | 0 | — | ns |
| t _{hZ} | CLK to output in H - Z | | 2.7 | 5.4 | 3 | 6 | ns |
| t _{rc} | ROW cycle time | | 67.5 | — | 70 | — | ns |
| t _{ras} | ROW active time | | 45 | 100,000 | 50 | 100,000 | ns |
| t _{rCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay | | 20 | — | 20 | — | ns |
| t _{rp} | Row precharge time | | 20 | — | 20 | — | ns |
| t _{rrd} | Row active to active delay | | 15 | — | 20 | — | ns |
| t _{dPL} | Data in to precharge | | 15 | — | 20 | — | ns |
| t _t | Transition time | | 1 | 10 | 1 | 10 | ns |
| t _{rsc} | Mode reg. set cycle | | 10 | — | 10 | — | ns |
| t _{pDE} | Power down exit setup time | | 7.5 | — | 10 | — | ns |
| t _{srx} | Self refresh exit time | | 7.5 | — | 10 | — | ns |
| t _{ref} | Refresh Time | | — | 64 | — | 64 | ms |

Notes:

1. if clock rising time is longer than 1ns, (tr/2-0.5ns) should be added to the parameter.

Basic Features and Function Description

Simplified State Diagram



COMMAND TRUTH TABLE

| Symbol | Command | CKE | | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | BA | A10 | A11 |
|--------|---------------------------|-----|---|-----------------|------------------|------------------|-----------------|----|-----|-------|
| | | n-1 | n | | | | | | | A9-A0 |
| DESL | Device deselect | H | X | H | X | X | X | X | X | X |
| NOP | No operation | H | X | L | H | H | H | X | X | X |
| MRS | Mode register set | H | X | L | L | L | L | L | L | V |
| ACT | Bank activate | H | X | L | L | H | H | V | V | V |
| READ | Read | H | X | L | H | L | H | V | L | V |
| READA | Read with auto precharge | H | X | L | H | L | H | V | H | V |
| WRIT | Write | H | X | L | H | L | L | V | L | V |
| WRITA | Write with auto precharge | H | X | L | H | L | L | V | H | V |
| PRE | Precharge select bank | H | X | L | L | H | L | V | L | X |
| PALL | Precharge all banks | H | X | L | L | H | L | X | H | X |
| BST | Burst stop | H | X | L | H | H | L | X | X | X |
| REF | CBR (Auto) refresh | H | H | L | L | L | H | X | X | X |
| SELF | Self refresh | H | L | L | L | L | H | X | X | X |

Notes:

H : High level

L : Low level

X : High or Low level (Don't care)

V : Valid Data input

DQM TRUTH TABLE

| Symbol | Command | CKE | | DQM |
|--------|----------------------------|-----|---|-----|
| | | n-1 | n | |
| ENB | Data Write / Output Enable | H | X | L |
| MASK | Data Mask / Output Disable | H | X | H |

CKE TRUTH TABLE

| Symbol | Command | Current State | CKE | | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Address |
|--------|--------------------------|---------------|-----|---|-----------------|------------------|------------------|-----------------|---------|
| | | | n-1 | n | | | | | |
| – | Clock suspend mode entry | Activating | H | L | X | X | X | X | X |
| – | Clock suspend | Any | L | L | X | X | X | X | X |
| – | Clock suspend mode exit | Clock suspend | L | H | X | X | X | X | X |
| REF | CBR refresh command | Idle | H | H | L | L | L | H | X |
| SELF | Self refresh entry | Idle | H | L | L | L | L | H | X |
| – | Self refresh exit | Self refresh | L | H | L | H | H | H | X |
| – | Power down entry | Idle | H | L | X | X | X | X | X |
| – | Power down exit | Power down | L | H | X | X | X | X | X |

OPERATION COMMAND TABLE⁽¹⁾

| Current State | Command | Operation | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Address |
|---------------------------------|--------------|---------------------------------------------------------|-----------------|------------------|------------------|-----------------|-------------|
| Idle | DESL | NOP or Power-Down ⁽²⁾ | H | X | X | X | X |
| | NOP or BST | NOP or Power-Down ⁽²⁾ | L | H | H | X | X |
| | READ / READA | Illegal ⁽³⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ⁽³⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Row Active | L | L | H | H | BR, RA |
| | PRE/PALL | NOP | L | L | H | L | BA, A10 |
| | REF/SELF | Refresh or Self-Refresh ⁽⁴⁾ | L | L | L | H | X |
| | MRS | Mode Register Set | L | L | L | L | Op-Code |
| Row Active | DESL | NOP | H | X | X | X | X |
| | NOP or BST | NOP | L | H | H | H | X |
| | READ/READA | Begin read : Determine AP ⁽⁵⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Begin write : Determine AP ⁽⁵⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Precharge ⁽⁶⁾ | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |
| Read | DESL | Continue burst to -> end Row active | H | X | X | X | X |
| | NOP | Continue burst to -> end Row active | L | H | H | H | X |
| | BST | Burst stop -> Row active | L | H | H | L | X |
| | READ/READA | Term burst, new read : Determine AP ⁽⁷⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Term burst, start write : Determine AP ^(7,8) | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Term burst, precharging | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| MRS | Illegal | L | L | L | L | Op-Code | |
| Write | DESL | Continue burst to end -> write recovering | H | X | X | X | X |
| | NOP | Continue burst to end -> write recovering | L | H | H | H | X |
| | BST | Burst stop -> Row active | L | H | H | L | X |
| | READ/READA | Term burst, start read : Determine AP ^(7,8) | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Term burst, new write : Determine AP ⁽⁷⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Term burst, precharging ⁽⁹⁾ | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| MRS | Illegal | L | L | L | L | Op-Code | |
| Read With Auto- Precharge | DESL | Continue burst to end -> Precharging | H | X | X | X | X |
| | NOP | Continue burst to end -> Precharging | L | H | H | H | X |
| | BST | Illegal | L | H | H | L | X |
| | READ/READA | Illegal ⁽¹¹⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ⁽¹¹⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Illegal ⁽¹¹⁾ | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| MRS | Illegal | L | L | L | L | Op-Code | |

OPERATION COMMAND TABLE^(continue)

| Current State | Command | Operation | \overline{CS} | \overline{RAS} | \overline{CAS} | \overline{WE} | Address |
|---------------------------|--------------|---------------------------------------------------------------|-----------------|------------------|------------------|-----------------|-------------|
| Write with auto precharge | DESL | Continue burst to end -> write recovering with auto precharge | H | X | X | X | X |
| | NOP | Continue burst to end -> write recovering with auto precharge | L | H | H | H | X |
| | BST | Illegal | L | H | H | L | X |
| | READ / READA | Illegal ⁽¹¹⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ⁽¹¹⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ^(3, 11) | L | L | H | H | BR, RA |
| | PRE/PALL | Illegal ^(3, 11) | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |
| Precharging | DESL | Nop -> Enter idle after tRP | H | X | X | X | X |
| | NOP | Nop -> Enter idle after tRP | L | H | H | H | X |
| | BST | Nop -> Enter idle after tRP | L | H | H | L | X |
| | READ/READA | Illegal ⁽³⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ⁽³⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Nop -> Enter idle after tRP | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |
| Row activating | DESL | Nop -> Enter row active after tRCD | H | X | X | X | X |
| | NOP | Nop -> Enter row active after tRCD | L | H | H | H | X |
| | BST | Nop -> Enter row active after tRCD | L | H | H | L | X |
| | READ/READA | Illegal ⁽³⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ⁽³⁾ | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ^(3, 9) | L | L | H | H | BR, RA |
| | PRE/PALL | Illegal ⁽³⁾ | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |
| Write recovering | DESL | Nop -> Enter row active after tDPL | H | X | X | X | X |
| | NOP | Nop -> Enter row active after tDPL | L | H | H | H | X |
| | BST | Nop -> Enter row active after tDPL | L | H | H | L | X |
| | READ/READA | Start read, Determine AP ⁽⁸⁾ | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | New write, Determine AP | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ⁽³⁾ | L | L | H | H | BR, RA |
| | PRE/PALL | Illegal ⁽³⁾ | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |

OPERATION COMMAND TABLE^(continue)

| Current State | Command | Operation | \overline{CS} | RAS | \overline{CAS} | WE | Address |
|-----------------------------------------------|---------------|--------------------------------------|-----------------|-----|------------------|----|-------------|
| Write recovering with auto precharge | DESL | Nop -> Enter precharge after tDPL | H | X | X | X | X |
| | NOP | Nop -> Enter precharge after tDPL | L | H | H | H | X |
| | BST | Nop -> Enter precharge after tDPL | L | H | H | L | X |
| | READ/READA | Illegal ^(3, 8, 11) | L | H | L | H | BA, CA, A10 |
| | WRIT/WRITA | Illegal ^(3,11) | L | H | L | L | BA, CA, A10 |
| | ACT | Illegal ^(3, 11) | L | L | H | H | BR, RA |
| | PRE/PALL | Illegal ^(3, 11) | L | L | H | L | BA, A10 |
| | REF/SELF | Illegal | L | L | L | H | X |
| | MRS | Illegal | L | L | L | L | Op-Code |
| Auto | DESL | Nop Enter idle after t _{rc} | H | X | X | X | X |
| Refreshing | NOP/BST | Nop Enter idle after t _{rc} | L | H | H | X | X |
| | READ/WRIT | Illegal | L | H | L | X | X |
| | ACT/PRE/PALL | Illegal | L | L | H | X | X |
| | REF/SELF/MRS | Illegal | L | L | L | X | X |
| Mode | DESL | Nop -> Enter idle after 2 Clocks | H | X | X | X | X |
| register | NOP | Nop -> Enter idle after 2 Clocks | L | H | H | H | X |
| setting | BST | Illegal | L | H | H | L | X |
| | READ/WRIT | Illegal | L | H | L | X | X |
| | ACT/PRE/PALL/ | Illegal | L | L | X | X | X |
| | REF/SELF/MRS | | | | | | |

Notes:

1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power downmode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by BankAddress(BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data which don't satisfy t_{DPL}.
10. Illegal if t_{RRD} is not satisfied.
11. Illegal for single bank, but legal for other banks in multi-bank devices.

CKE RELATED COMMAND TRUTH TABLE⁽¹⁾

| Current State | Operation | CKE | | \overline{CS} | RAS | \overline{CAS} | WE | Address |
|-----------------------------------|------------------------------------------------|-----|---|-----------------|-----|------------------|----|-----------|
| | | n-1 | n | | | | | |
| Self-Refresh (S.R.) | INVALID, CLK (n - 1) would exit S.R. | H | X | X | X | X | X | X |
| | Self-Refresh Recovery ⁽²⁾ | L | H | H | X | X | X | X |
| | Self-Refresh Recovery ⁽²⁾ | L | H | L | H | H | X | X |
| | Illegal | L | H | L | H | L | X | X |
| | Illegal | L | H | L | L | X | X | X |
| | Maintain S.R. | L | L | X | X | X | X | X |
| Self-Refresh Recovery | Idle After t _{RC} | H | H | H | X | X | X | X |
| | Idle After t _{RC} | H | H | L | H | H | X | X |
| | Illegal | H | H | L | H | L | X | X |
| | Illegal | H | H | L | L | X | X | X |
| | Begin clock suspend next cycle ⁽⁵⁾ | H | L | H | X | X | X | X |
| | Begin clock suspend next cycle ⁽⁵⁾ | H | L | L | H | H | X | X |
| | Illegal | H | L | L | H | L | X | X |
| | Illegal | H | L | L | L | X | X | X |
| | Exit clock suspend next cycle ⁽²⁾ | L | H | X | X | X | X | X |
| | Maintain clock suspend | L | L | X | X | X | X | X |
| Power-Down (P.D.) | INVALID, CLK (n - 1) would exit P.D. | H | X | X | X | X | X | — |
| | EXIT P.D. -> Idle ⁽²⁾ | L | H | X | X | X | X | X |
| | Maintain power down mode | L | L | X | X | X | X | X |
| Both Banks Idle | Refer to operations in Operative Command Table | H | H | H | X | X | X | — |
| | Refer to operations in Operative Command Table | H | H | L | H | X | X | — |
| | Refer to operations in Operative Command Table | H | H | L | L | H | X | — |
| | Auto-Refresh | H | H | L | L | L | H | X |
| | Refer to operations in Operative Command Table | H | H | L | L | L | L | Op - Code |
| | Refer to operations in Operative Command Table | H | L | H | X | X | X | — |
| | Refer to operations in Operative Command Table | H | L | L | H | X | X | — |
| | Refer to operations in Operative Command Table | H | L | L | L | H | X | — |
| | Self-Refresh ⁽³⁾ | H | L | L | L | L | H | X |
| | Refer to operations in Operative Command Table | H | L | L | L | L | L | Op - Code |
| Power-Down ⁽³⁾ | L | X | X | X | X | X | X | |
| Any state other than listed above | Refer to operations in Operative Command Table | H | H | X | X | X | X | X |
| | Begin clock suspend next cycle ⁽⁴⁾ | H | L | X | X | X | X | X |
| | Exit clock suspend next cycle | L | H | X | X | X | X | X |
| | Maintain clock suspend | L | L | X | X | X | X | X |

Notes:

1. H : High level, L : low level, X : High or low level (Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5. Illegal if t_{SREX} is not satisfied.

Initialization

Before starting normal operation, the following power on sequence is necessary to prevent SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high , DQN high and NOP condition at the inputs.
2. Maintain stable power, table clock , and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all bank. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is in idle state and ready for normal operation.

Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A13 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields;

Options : A13 through A7
CAS latency : A6 through A4
Wrap type : A3
Burst length : A2 through A0

Following mode register programming, no command can be asserted before at least two clock cycles have elapsed.

CAS Latency

CAS latency is the most critical parameter being set. It tells the device how many clocks must elapse before the data will be available.

The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

MODE REGISTER

| | | | | | | | | | | | | | |
|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | | |

JEDEC Standard Test Set

| | | | | | | | | | | | | | |
|----|----|----|----|---|---|---|--------|---|----|----|---|---|---|
| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x | x | x | x | 1 | 0 | 0 | LTMODE | | WT | BL | | | |

Burst Read and Single Write (for Write Through Cache)

| | | | | | | | | | | | | | |
|----|----|----|----|---|---|---|--------|---|----|----|---|---|---|
| 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | LTMODE | | WT | BL | | | |

Burst Read and Burst Write

X = Don't care

| | | | |
|--------------|-----------|--------|--------|
| Burst length | Bits2 - 0 | WT = 0 | WT = 1 |
| | 000 | 1 | 1 |
| | 001 | 2 | 2 |
| | 010 | 4 | 4 |
| | 011 | 8 | 8 |
| | 100 | R | R |
| | 101 | R | R |
| | 110 | R | R |
| 111 | Fullpage | R | |

| | | |
|-----------|---|------------|
| Wrap type | 0 | Sequential |
| | 1 | Interleave |

| | | |
|--------------|----------|-------------|
| Latency mode | Bits 6-4 | CAS latency |
| | 000 | R |
| | 001 | R |
| | 010 | 2 |
| | 011 | 3 |
| | 100 | R |
| | 101 | R |
| | 110 | R |
| 111 | R | |

Remark R : Reserved

Burst Length and Sequence

Burst of Two

| Starting Address (column address A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence (decimal) |
|-------------------------------------------------|---------------------------------------------|---------------------------------------------|
| 0 | 0, 1 | 0, 1 |
| 1 | 1, 0 | 1, 0 |

Burst of Four

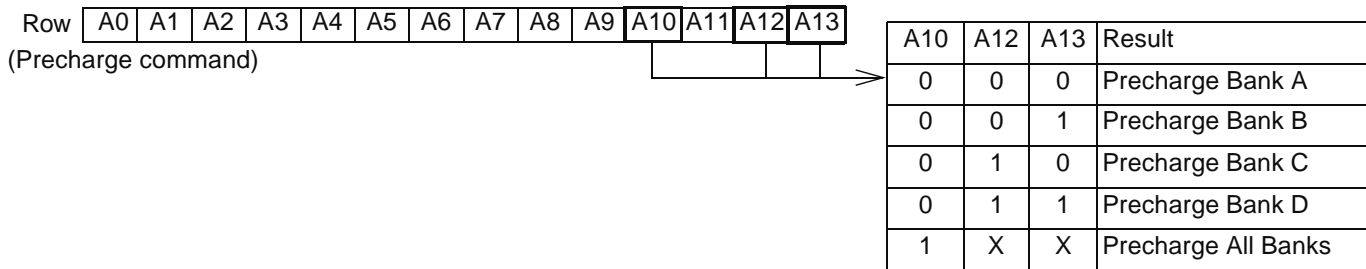
| Starting Address (column address A1 - A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence (decimal) |
|------------------------------------------------------|---------------------------------------------|---------------------------------------------|
| 00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| 01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| 10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| 11 | 3, 0, 1, 2 | 3, 2, 1, 0 |

Burst of Eight

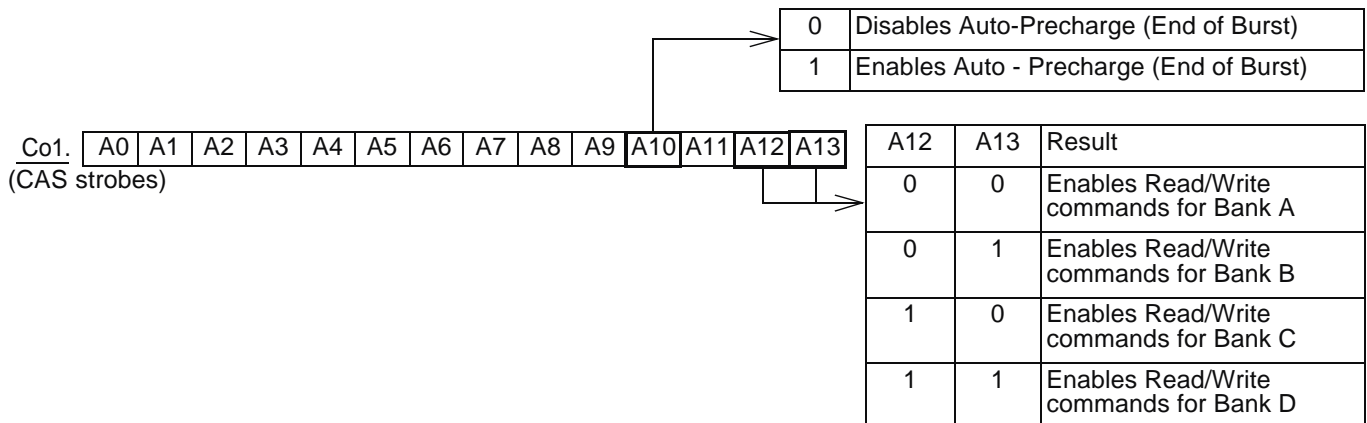
| Starting Address (column address A2 - A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence (decimal) |
|------------------------------------------------------|---------------------------------------------|---------------------------------------------|
| 000 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| 001 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| 010 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| 011 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| 100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| 101 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| 110 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| 111 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |

Full page burst is an extension of the above tables of sequential addressing, with the length being 512 (for 8M x 8) and 256 (for 4Mx16).

Address Bits of Bank-Select and Precharge



X: Don't care

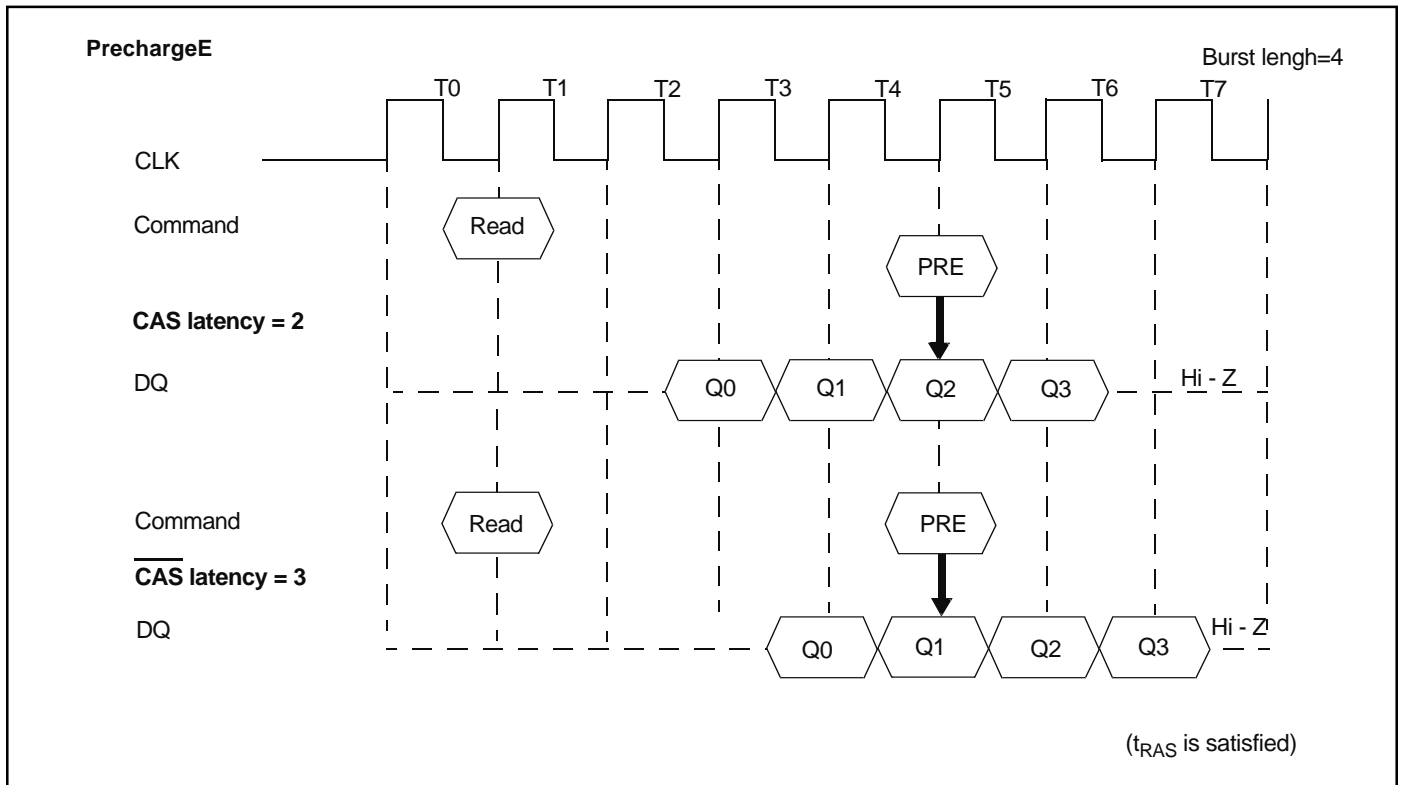


Precharge

The precharge command can be asserted anytime after $t_{RAS}(\text{min.})$ is satisfied.

Soon after the precharge command is asserted, the precharge operation is performed and the synchronous DRAM enters the idle state after $t_{RP}(\text{min.})$ is satisfied. The parameter t_{RP} is the time required to perform the precharge.

The earliest timing in a read cycle that a precharge command can be asserted without losing any data in the burst is as follows.



In order to write all data to the memory cell correctly, the asynchronous parameter t_{DPL} must be satisfied. The $t_{DPL}(\text{min.})$ specification defines the earliest time that a precharge command can be asserted. The minimum number of clocks can be calculated by dividing $t_{DPL}(\text{min.})$ with the clock cycle time.

In summary, the precharge command can be asserted relative to the reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

| CAS latency | Read | Write |
|-------------|------|--------------------------|
| 2 | -1 | + $t_{DPL}(\text{min.})$ |
| 3 | -2 | + $t_{DPL}(\text{min.})$ |

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high in the read or write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically.

In the write cycle, $t_{DAL}(\text{min.})$ must be satisfied before asserting the next activate command to the bank being precharged. When using auto precharge in the read cycle, knowing when the precharge starts is important because the next activate command to the bank being precharged cannot be executed until the precharge cycle ends. Once auto precharge has started, an activate command to the bank can be asserted after t_{RP} has been satisfied.

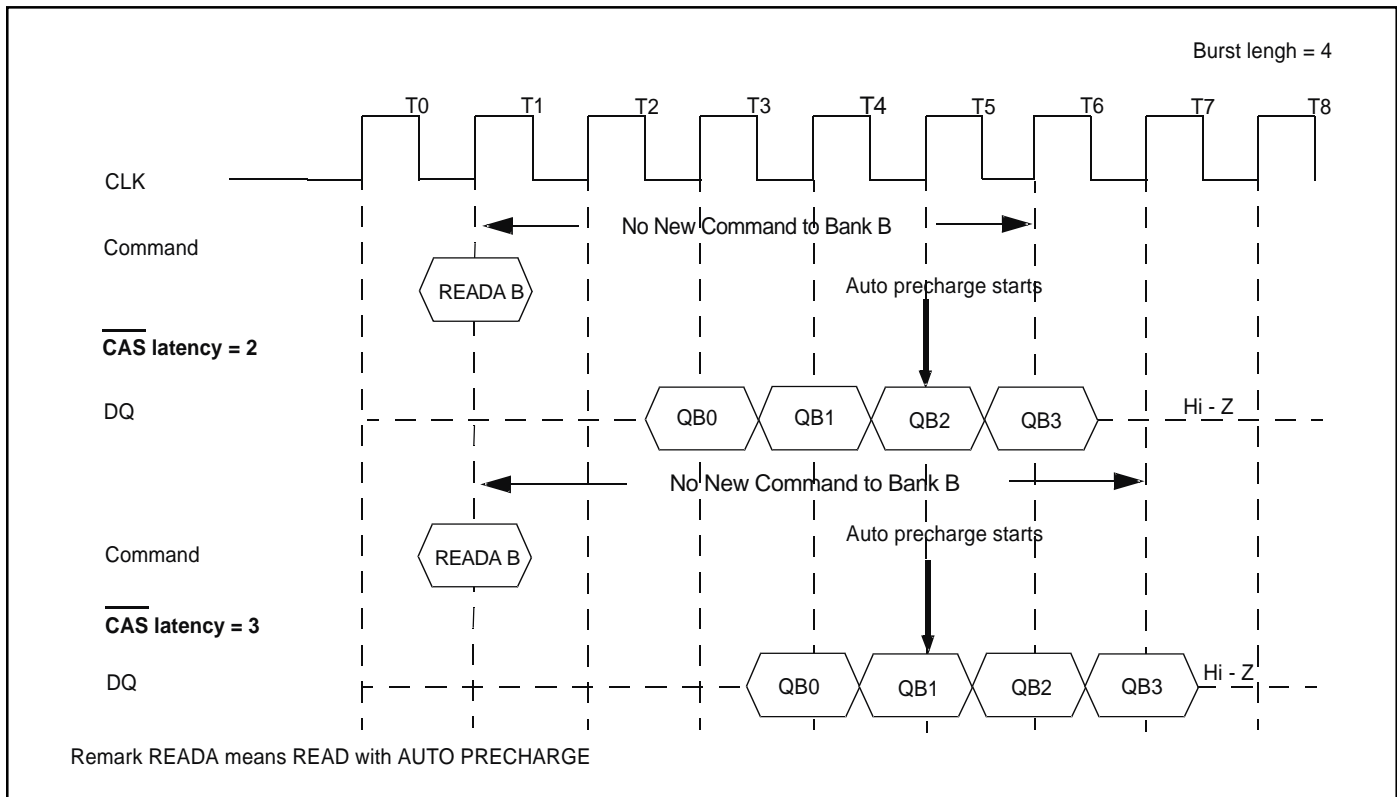
A Read or Write command without auto - precharge can be terminated in the midst of a burst operation. However, a Read or Write command with auto - precharge can not be interrupted by the same bank commands before the entire burst operation is completed. Therefore use of the same bank Read, Write, Precharge or Burst Stop command is prohibited during a read or write cycle with auto - precharge. It should be noted that the device will not respond to the Auto - Precharge command if the device is programmed for full page burst read or write cycles.

The timing when the auto precharge cycle begins depends both on both the $\overline{\text{CAS}}$ latency programmed into the mode register and whether the cycle is read or write.

Read with Auto Precharge

During a READA cycle, the auto precharge begins one clock earlier ($\text{CL} = 2$) or two clocks earlier ($\text{CL} = 3$) than the last word output.

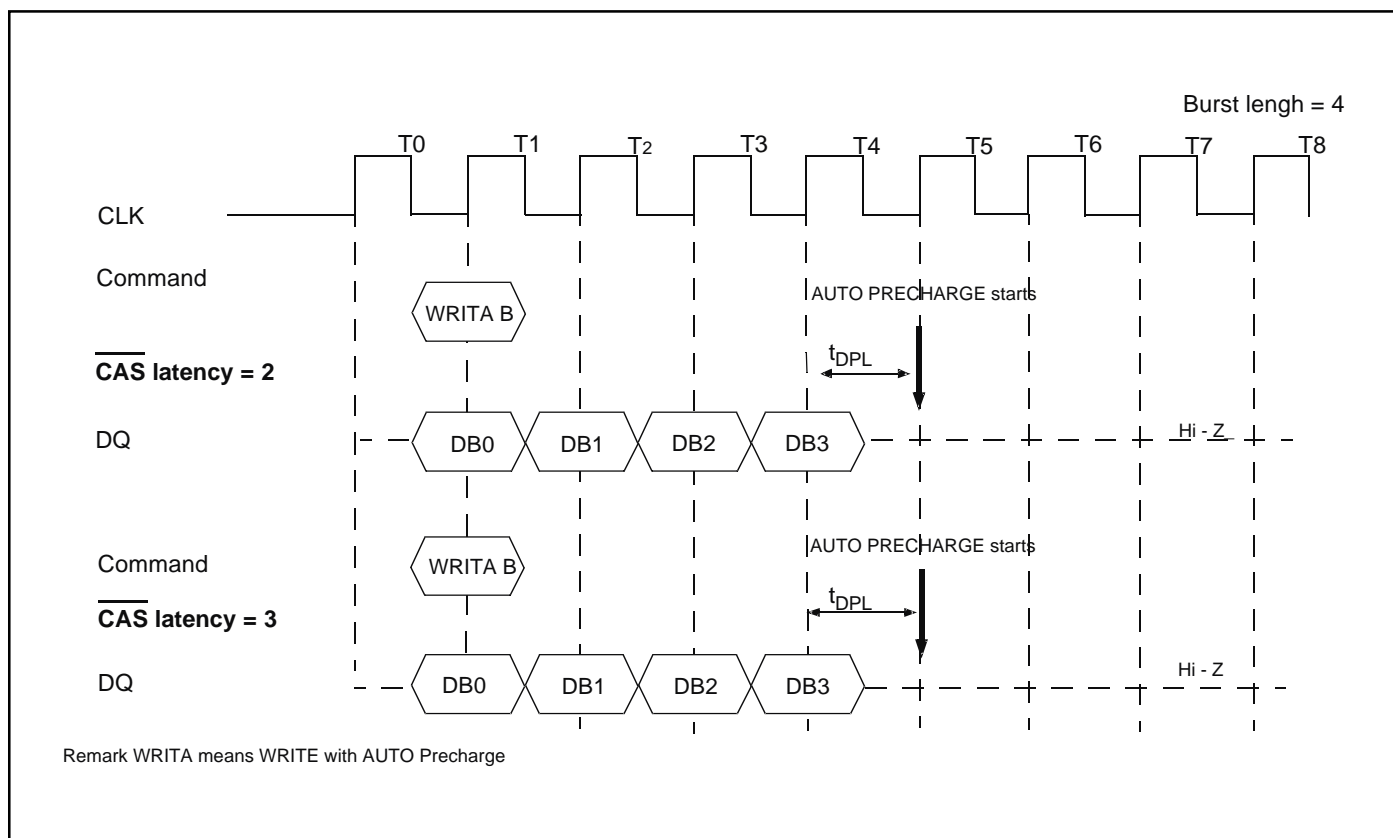
READ with AUTO PRECHARGE



Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing that is equal to the value of $t_{DPL}(\text{min.})$ after the last data word input to the device.

WRITE with AUTO PRECHARGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid. In the table below, minus means clocks before the reference; plus means clocks after the reference.

| CAS latency | Read | Write |
|-------------|------|--------------------------|
| 2 | -1 | + $t_{DPL}(\text{min.})$ |
| 3 | -2 | + $t_{DPL}(\text{min.})$ |

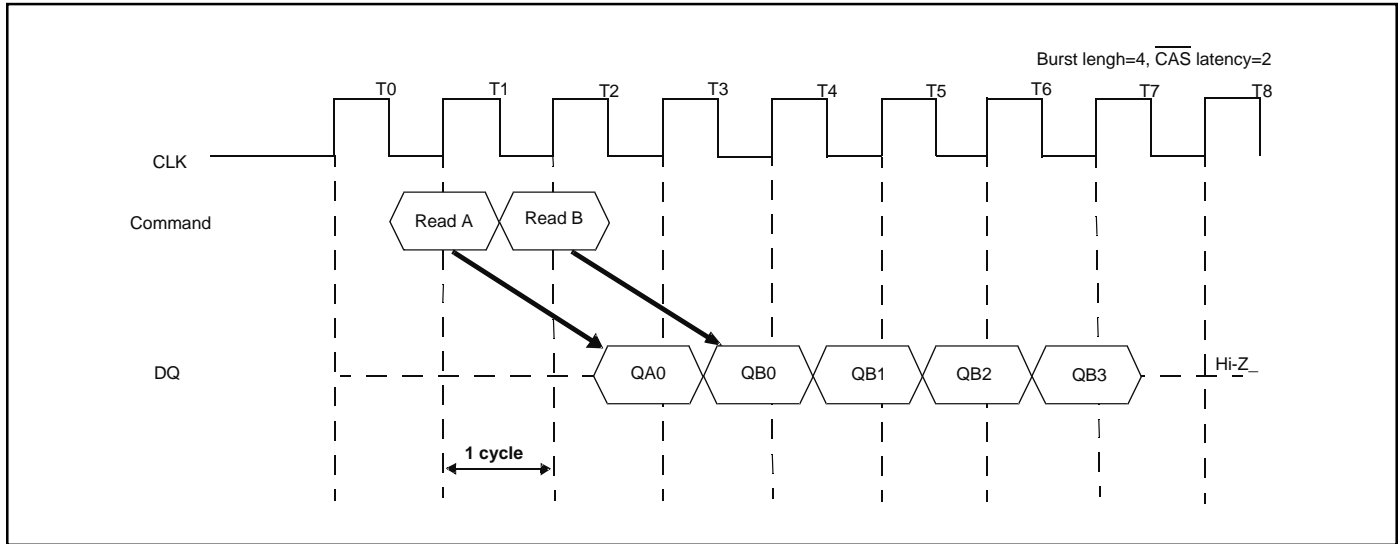
Read / Write Command Interval

Read to Read Command Interval

During a read cycle when a new read command is asserted, it will be effective after the CAS latency, even if the previous read operation has not completed. READ will be interrupted by another READ.

Each read command can be asserted in every clock without any restriction.

READ to READ Command Interval

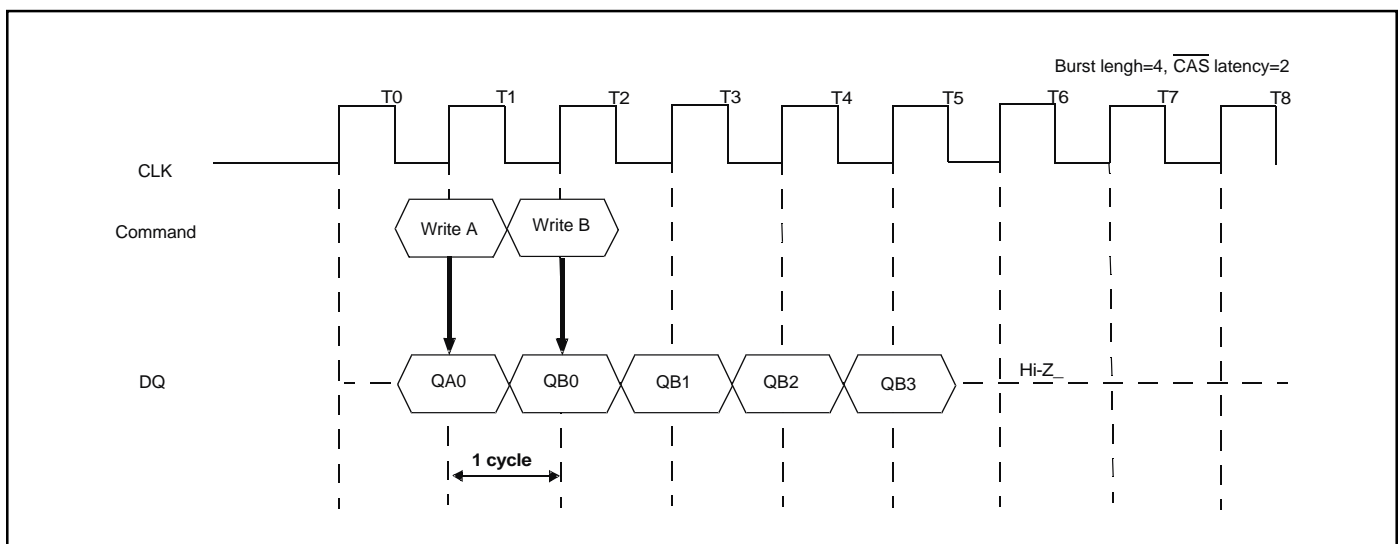


Write to Write Command Interval

During a write cycle, when a new Write command is asserted, the previous burst will be terminated and the new burst will begin with a new write command. WRITE will be interrupted by another WRITE.

Each write command can be asserted in every clock without any restriction.

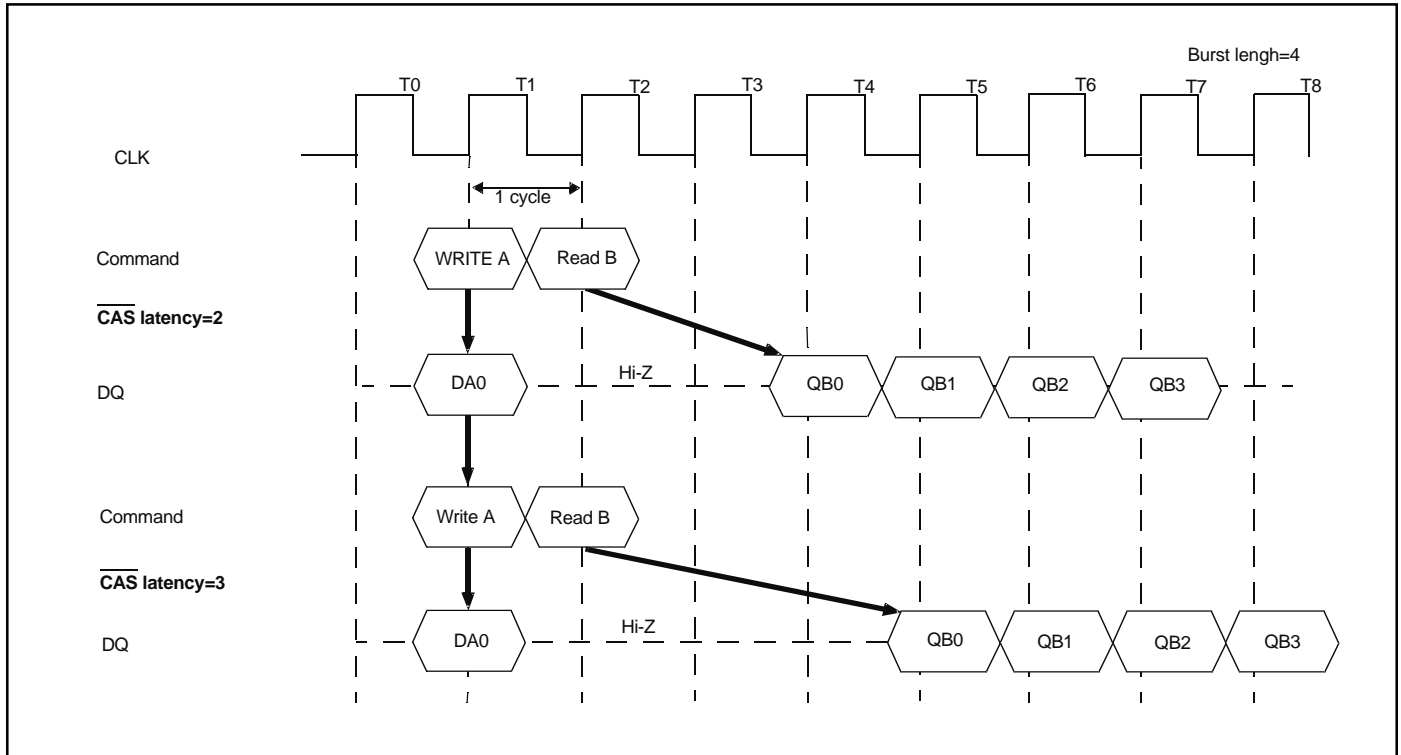
WRITE to WRITE Command Interval



Write to Read Command Interval

The write command to read command interval is also a minimum of 1 cycle. Only the write data before the read command will be written. The data bus must be Hi-Z at least one cycle prior to the first DOUT.

WRITE to READ Command Interval

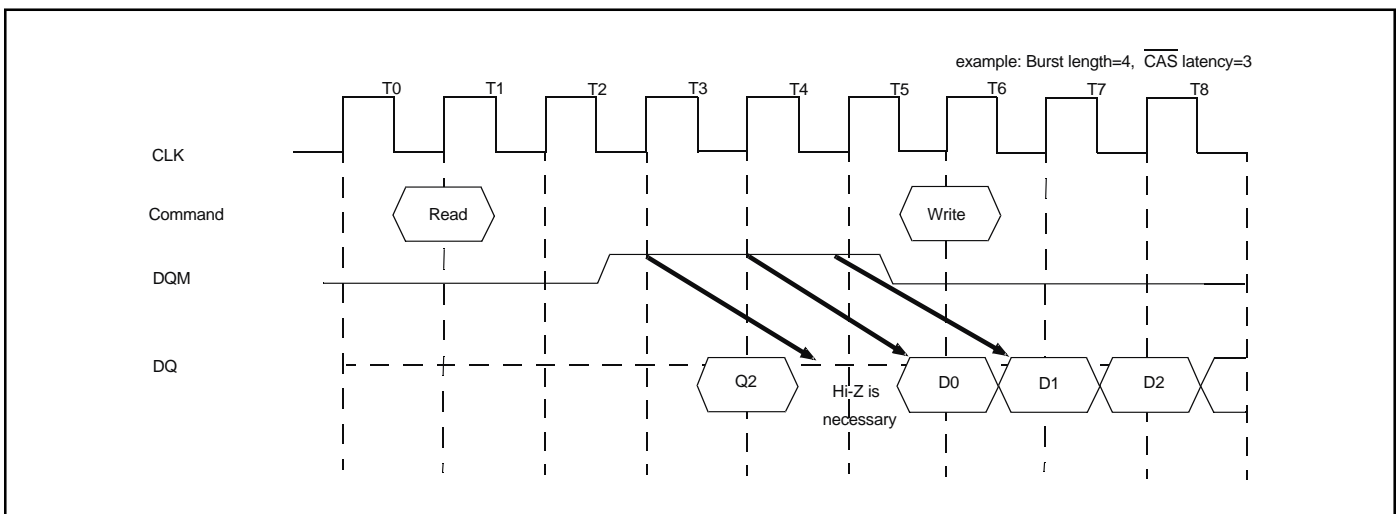
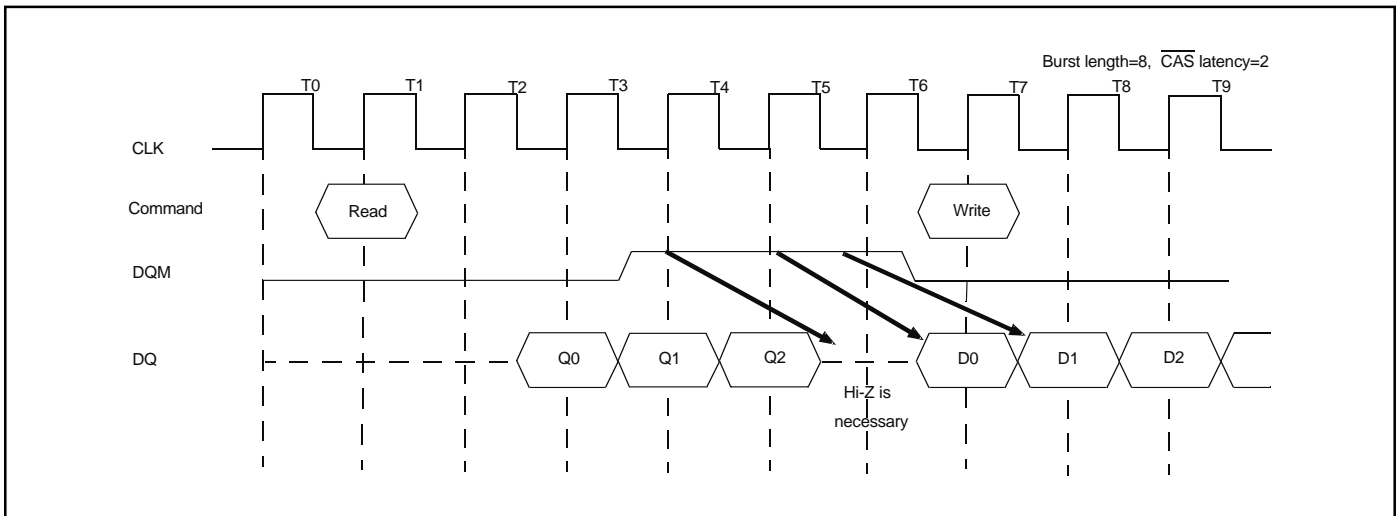
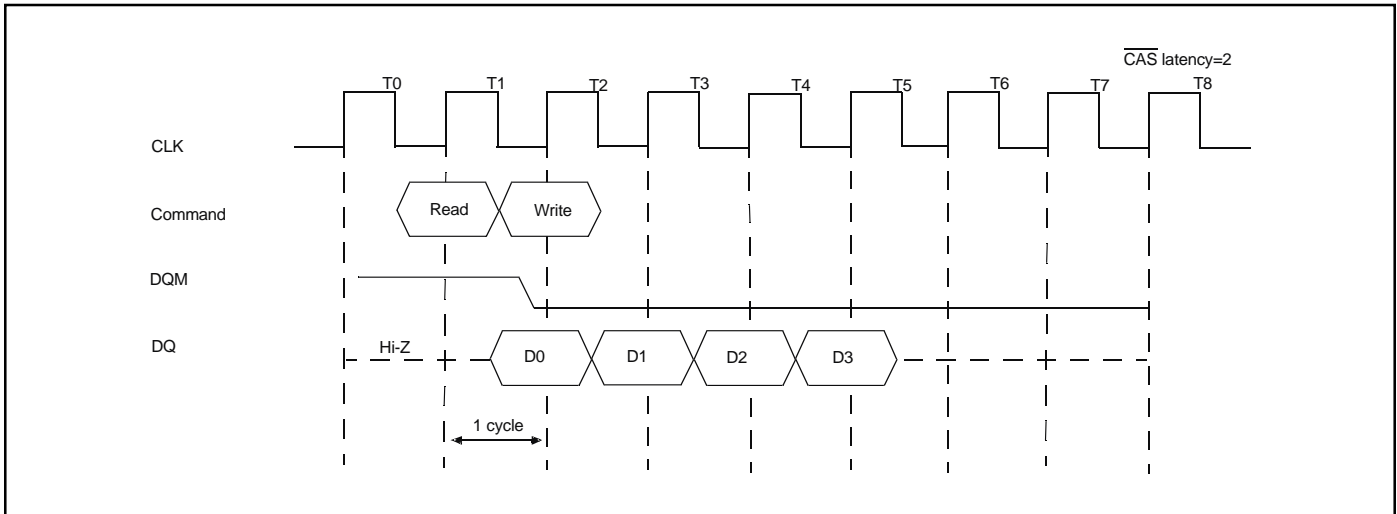


Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE.

DQM must be in High at least 3 clocks prior to the write command. There is a restriction to avoid a data conflict. The data bus must be Hi-Z using DQM before Write.

READ to WRITE Command Interval



BURST Termination

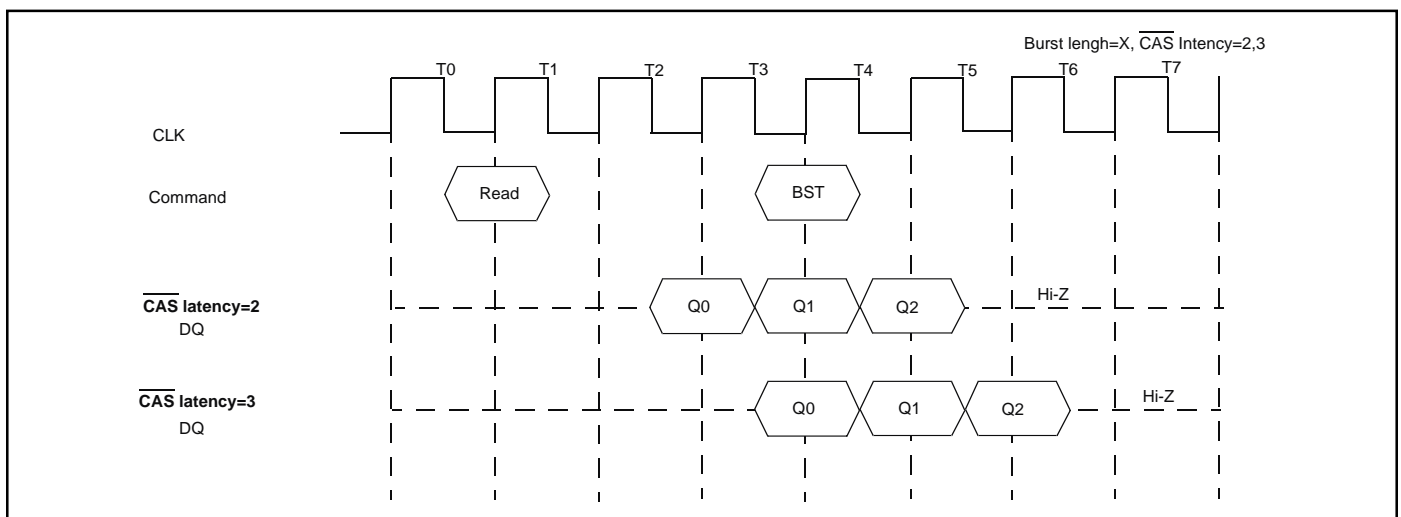
There are two methods to terminate a burst operation other than using a read or a write command. One is the burst stop command and the other is the precharge command.

BURST Stop Command

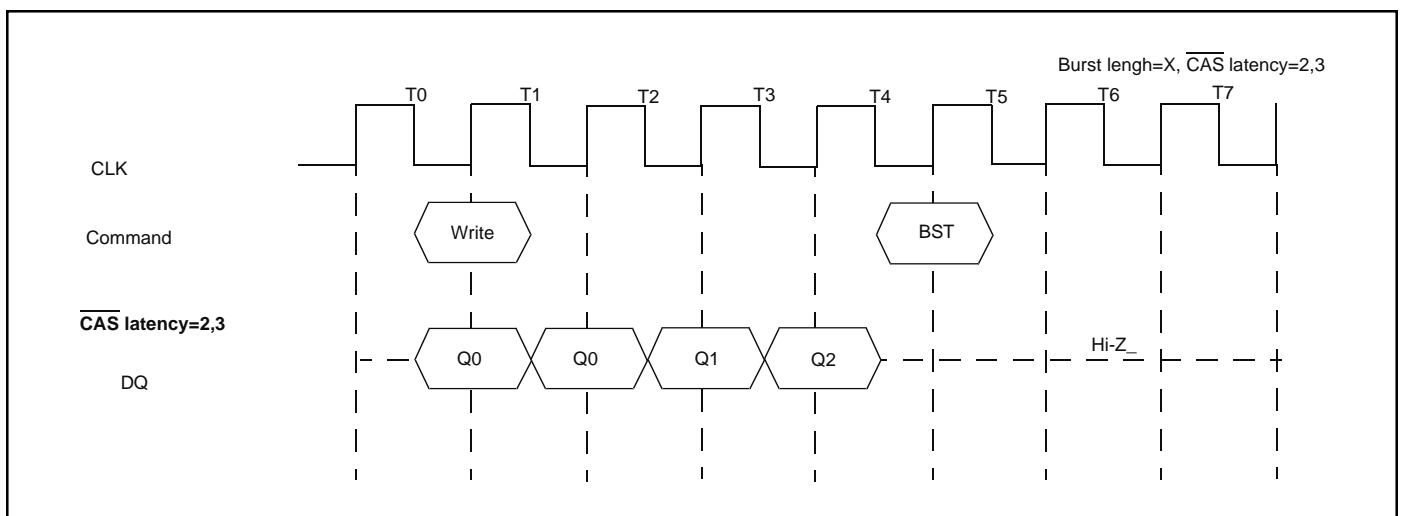
During a read burst, when the burst stop command is issued, the burst read data are terminated and the data bus goes to high-impedance after the CAS latency from the burst stop command.

During a write burst, when the burst stop command is issued, the burst write data are terminated and data bus goes to Hi-Z at the same clock with the burst stop command.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst command

PRECHARGE TERMINATION

PRECHARGE TERMINATION in READ Cycle

During READ cycle, the burst read operation is terminated by a precharge command.

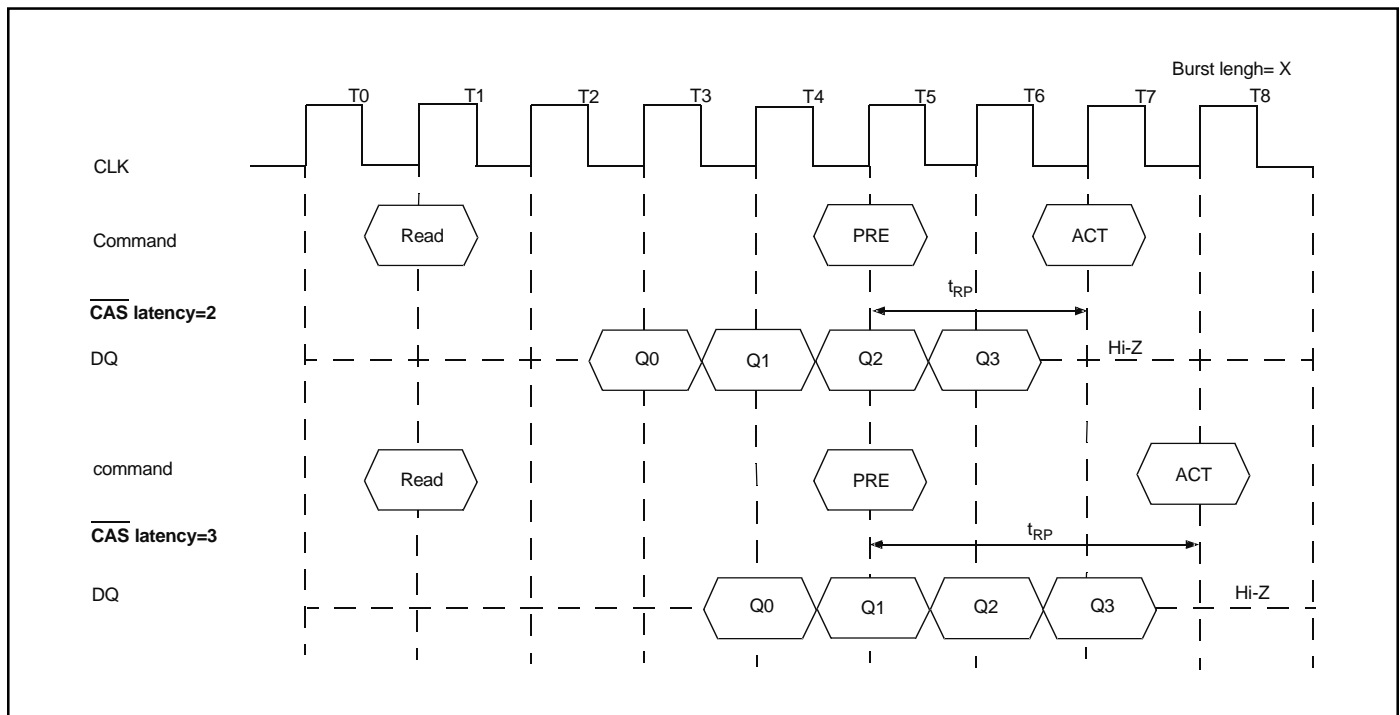
When the precharge command is issued, the burst read operation is terminated and precharge starts.

The same bank can be activated again after t_{RP} from the precharge command.

When CAS latency is 2, the read data will remain valid until one clock after the precharge command.

When CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

Precharge Termination in READ Cycle



Precharge Termination in WRITE Cycle

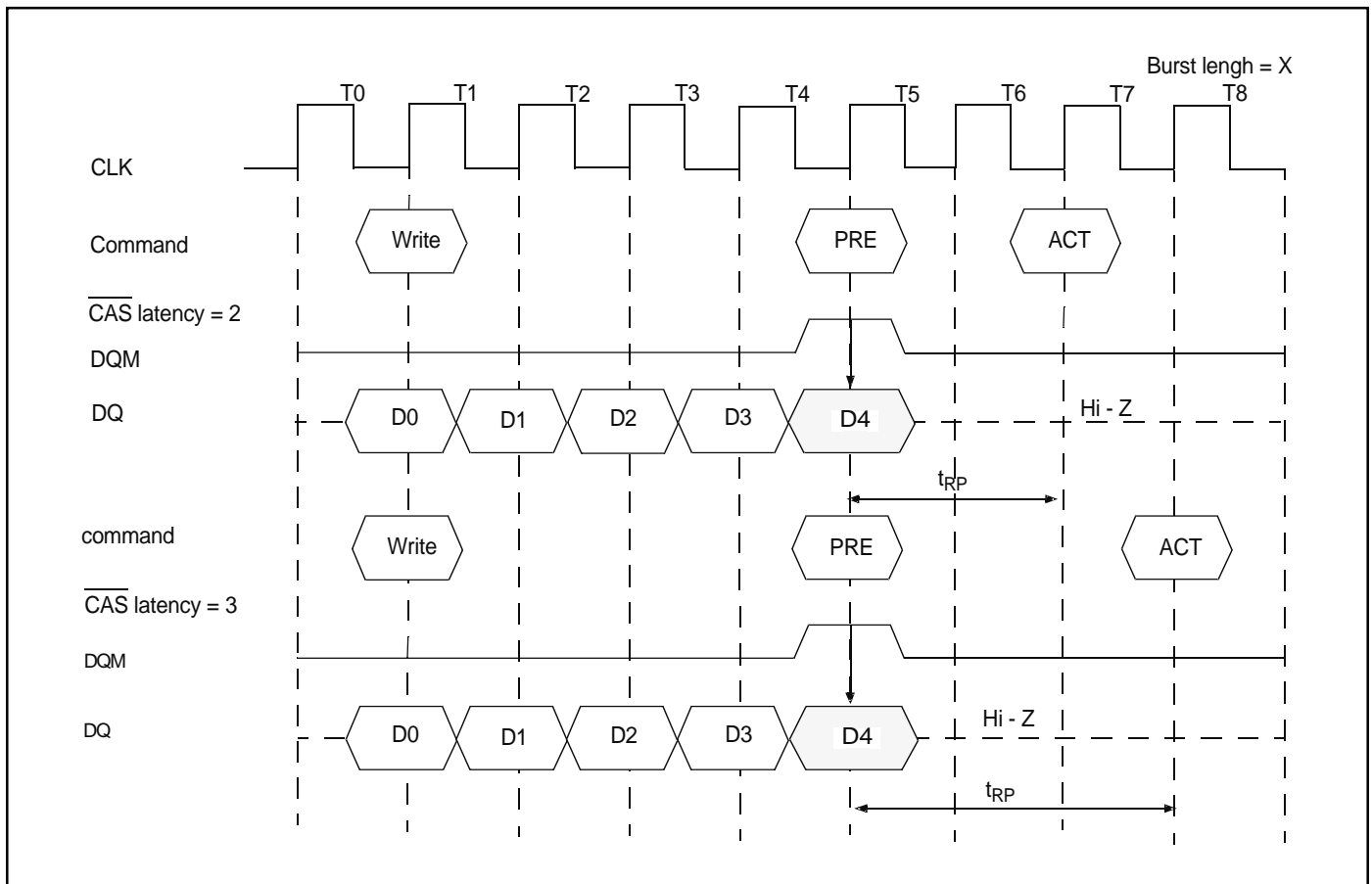
During WRITE cycle, the burst write operation is terminated by a precharge command.

When the precharge command is issued, the burst write operation is terminated and precharge starts.

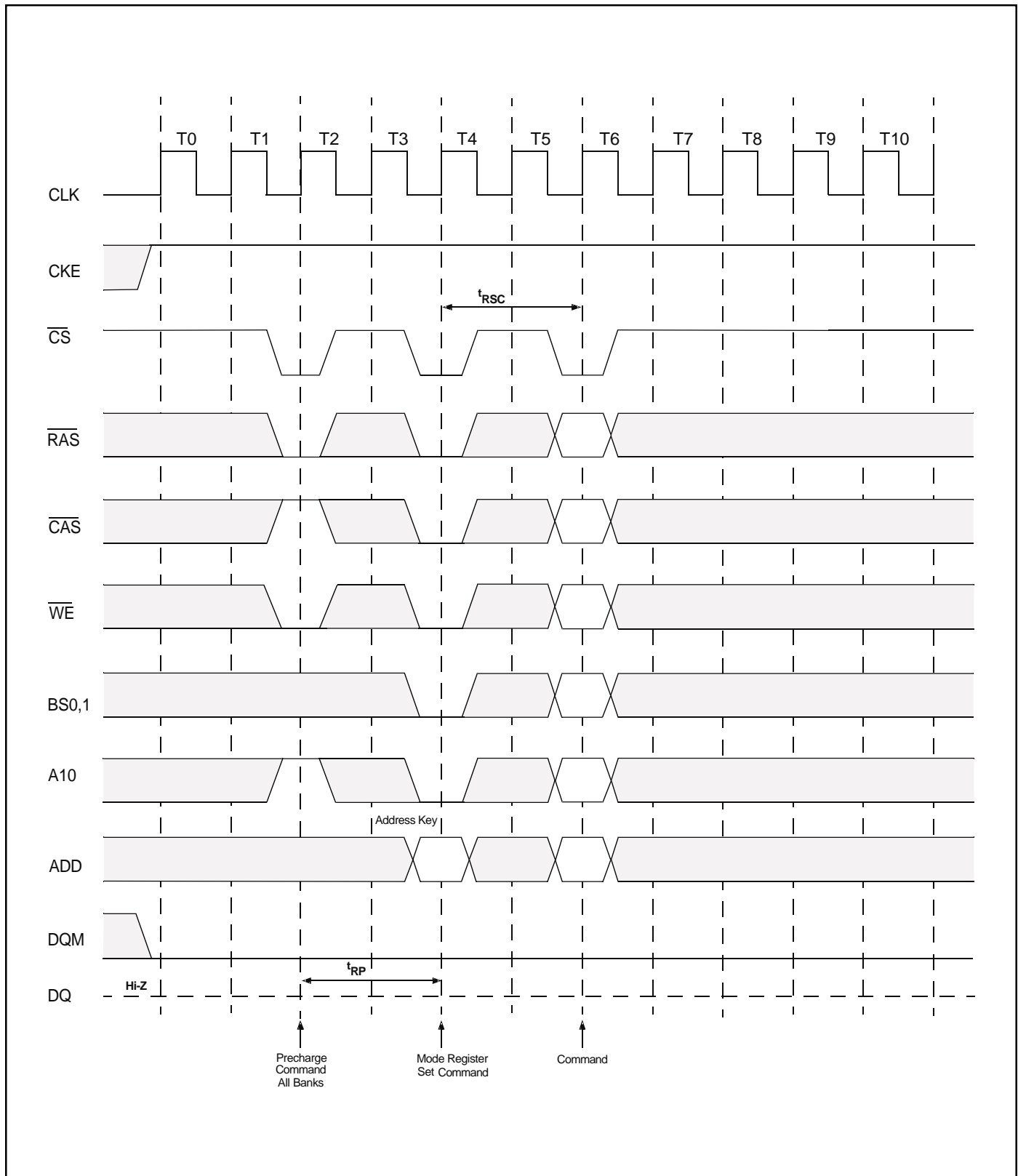
The same bank can be activated again after t_{RP} from the precharge command. The DQM must be high to mask invalid data in.

During WRITE cycle, the write data written prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command. To prevent this from happening, DQM must be high at the same clock as the precharge command. This will mask the invalid data.

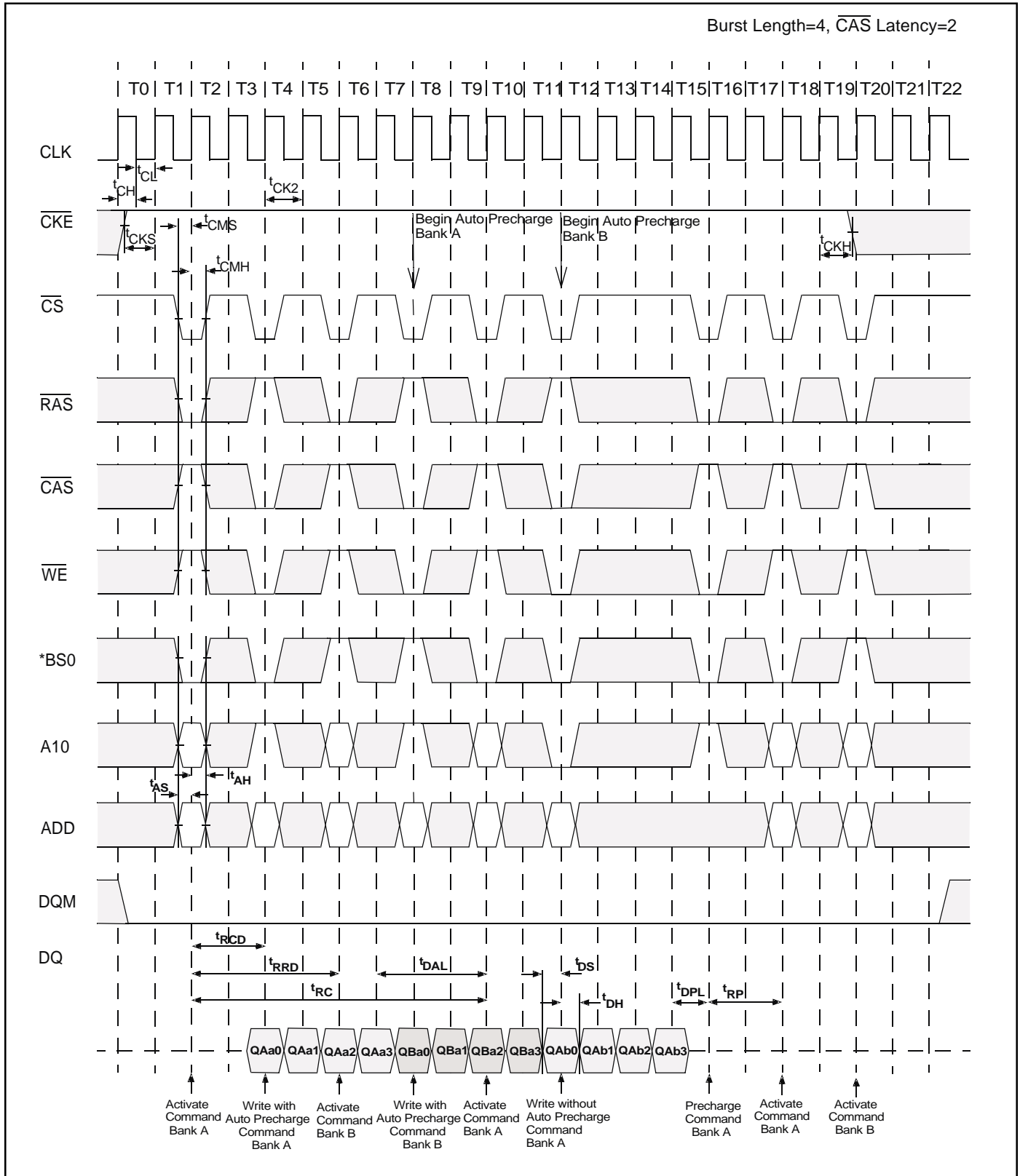
PRECHARGE TERMINATION in WRITE Cycle



Mode Register Set

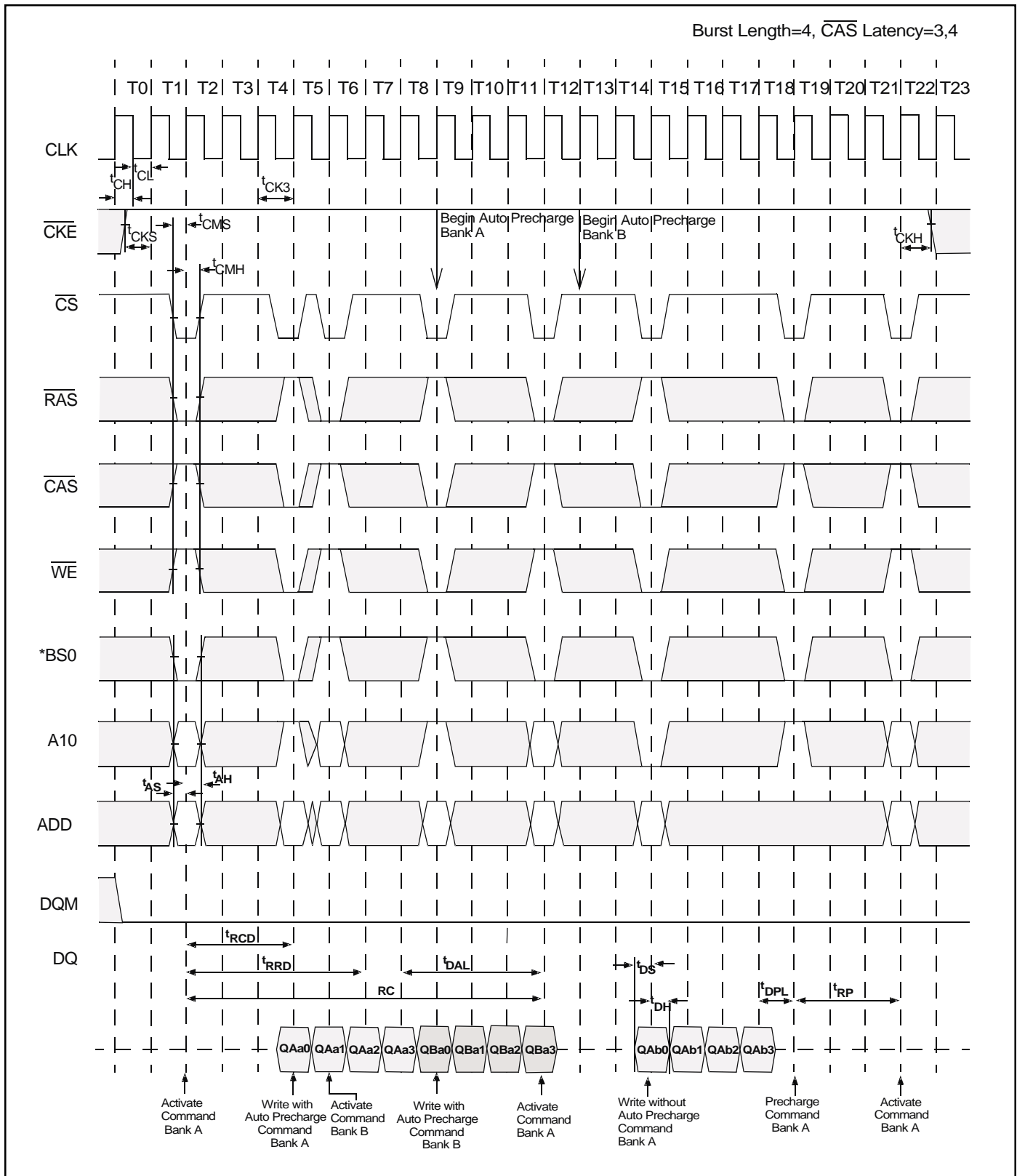


AC Parameters for Write Timing (1 of 2)



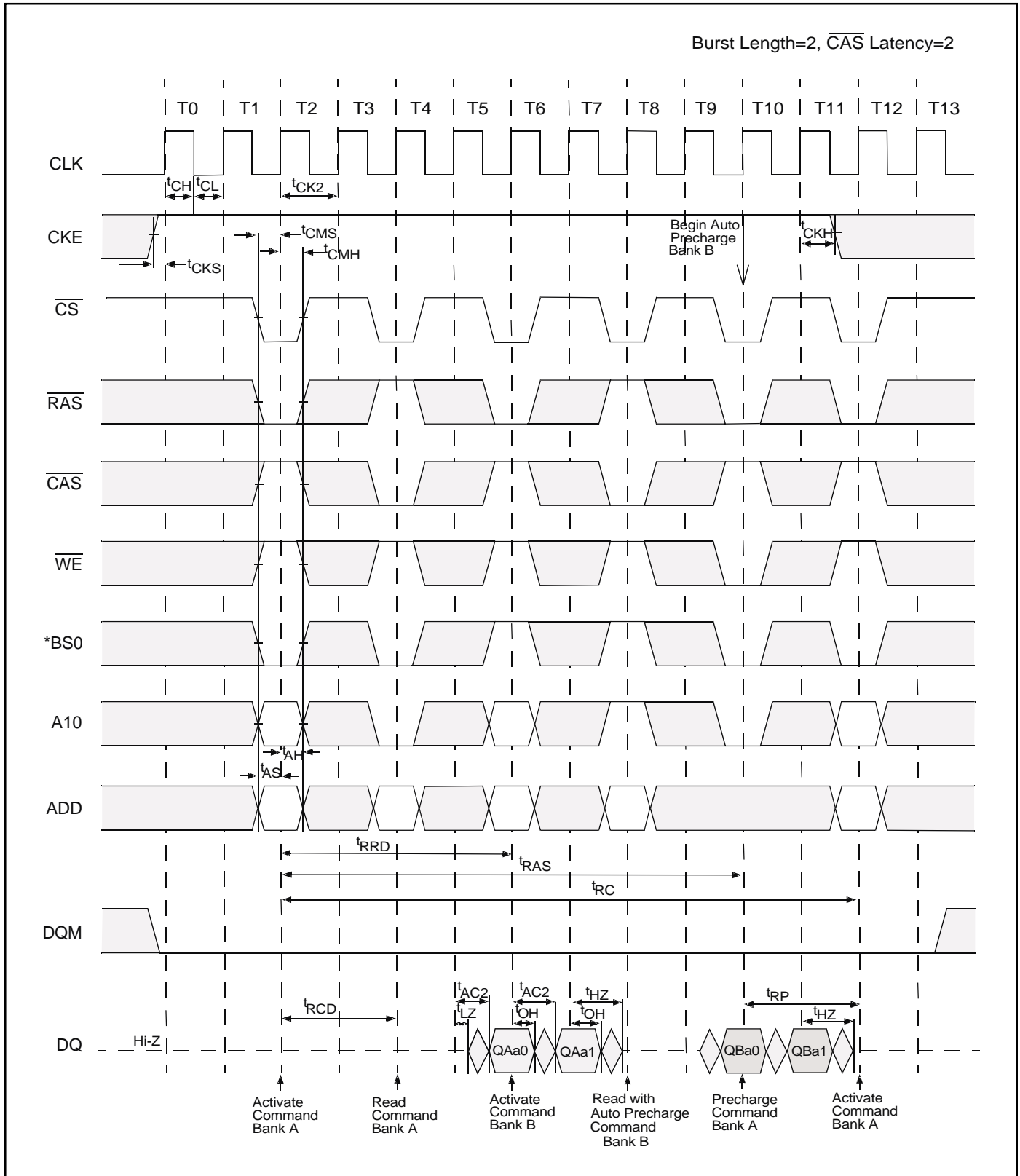
BS1="L", Bank C,D = Idle

AC Parameters for Write Timing (2 of 2)



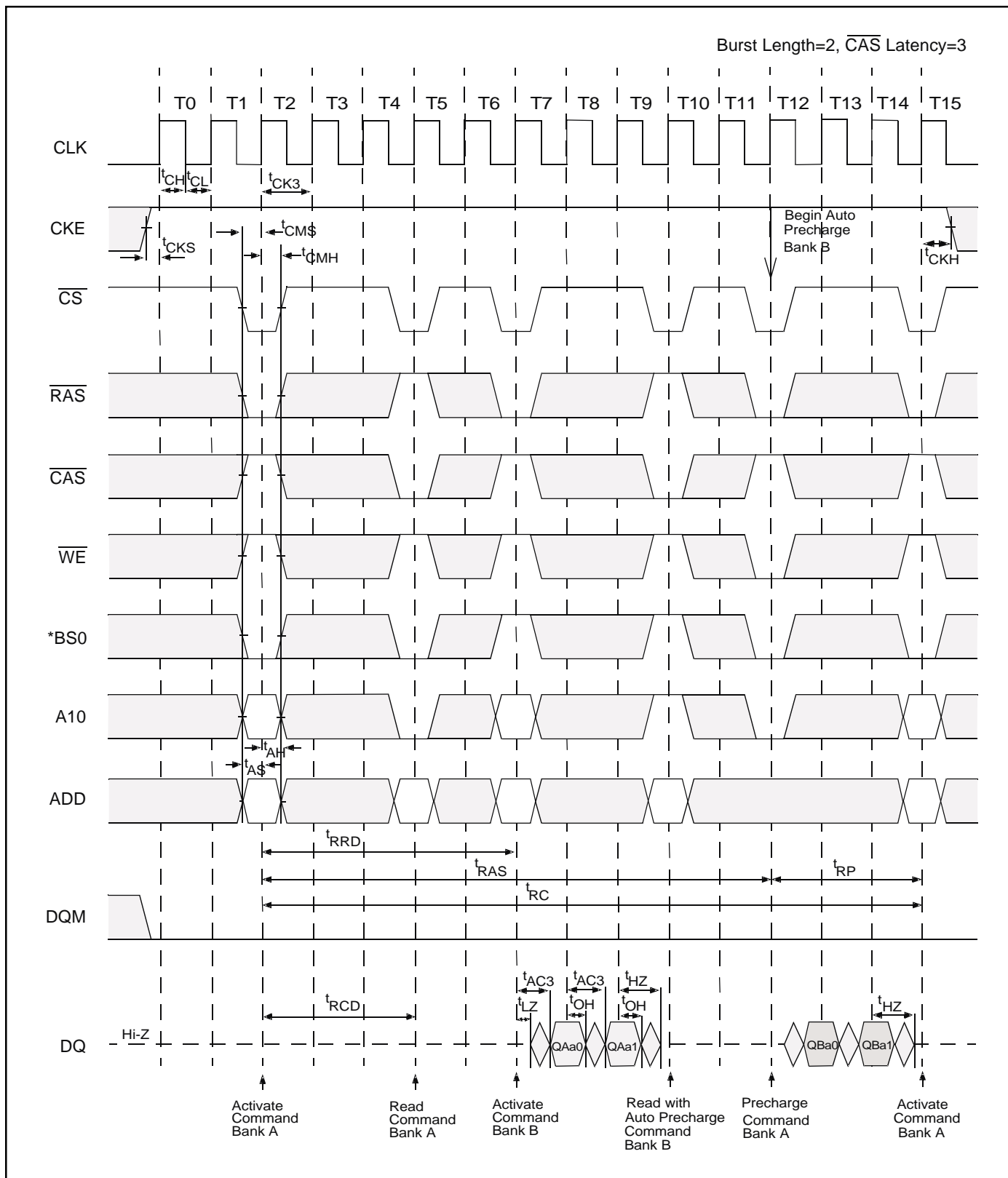
BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (1 of 2)



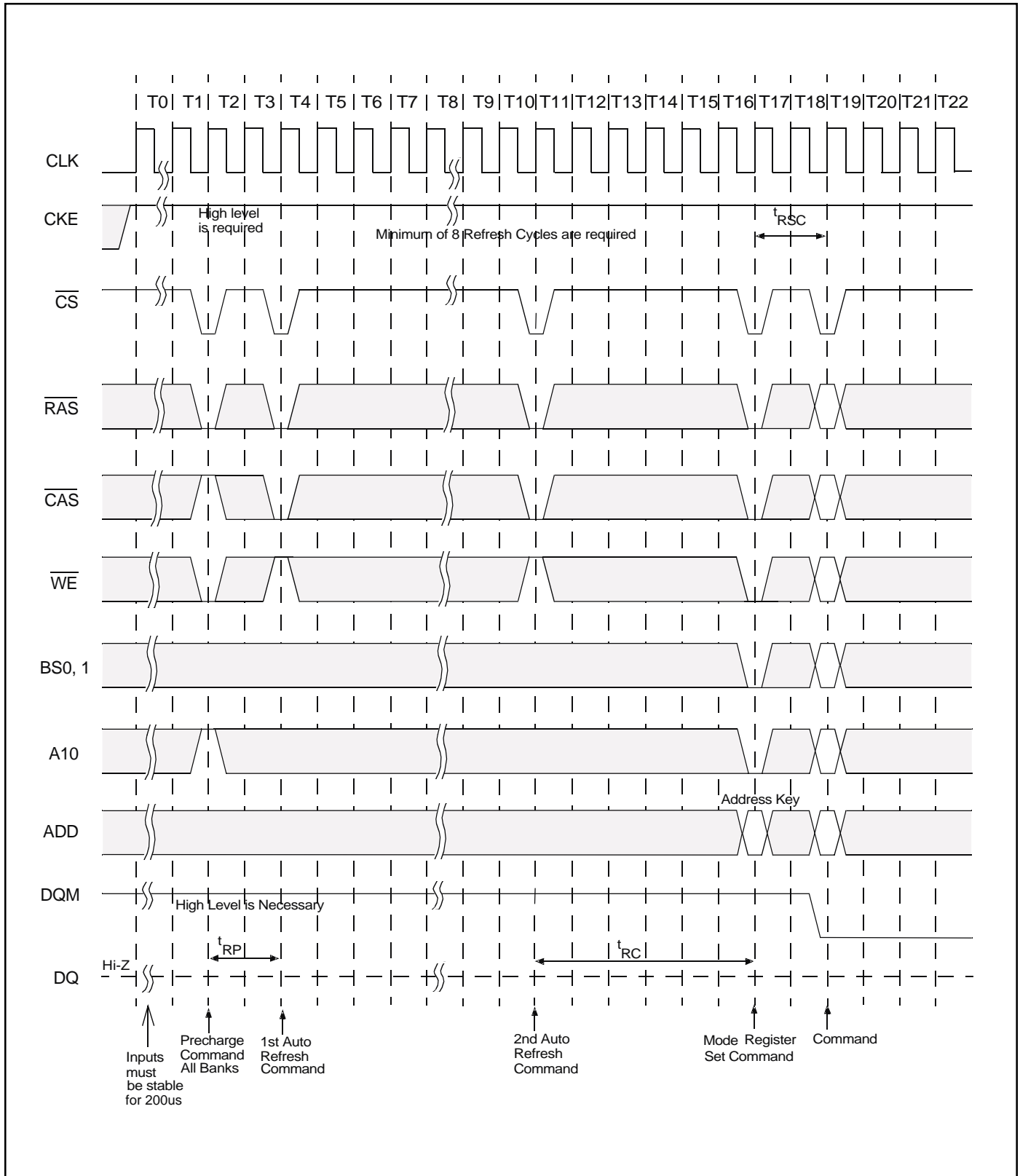
BS1="L", Bank C,D = Idle

AC Parameters for Read Timing (2 of 2)

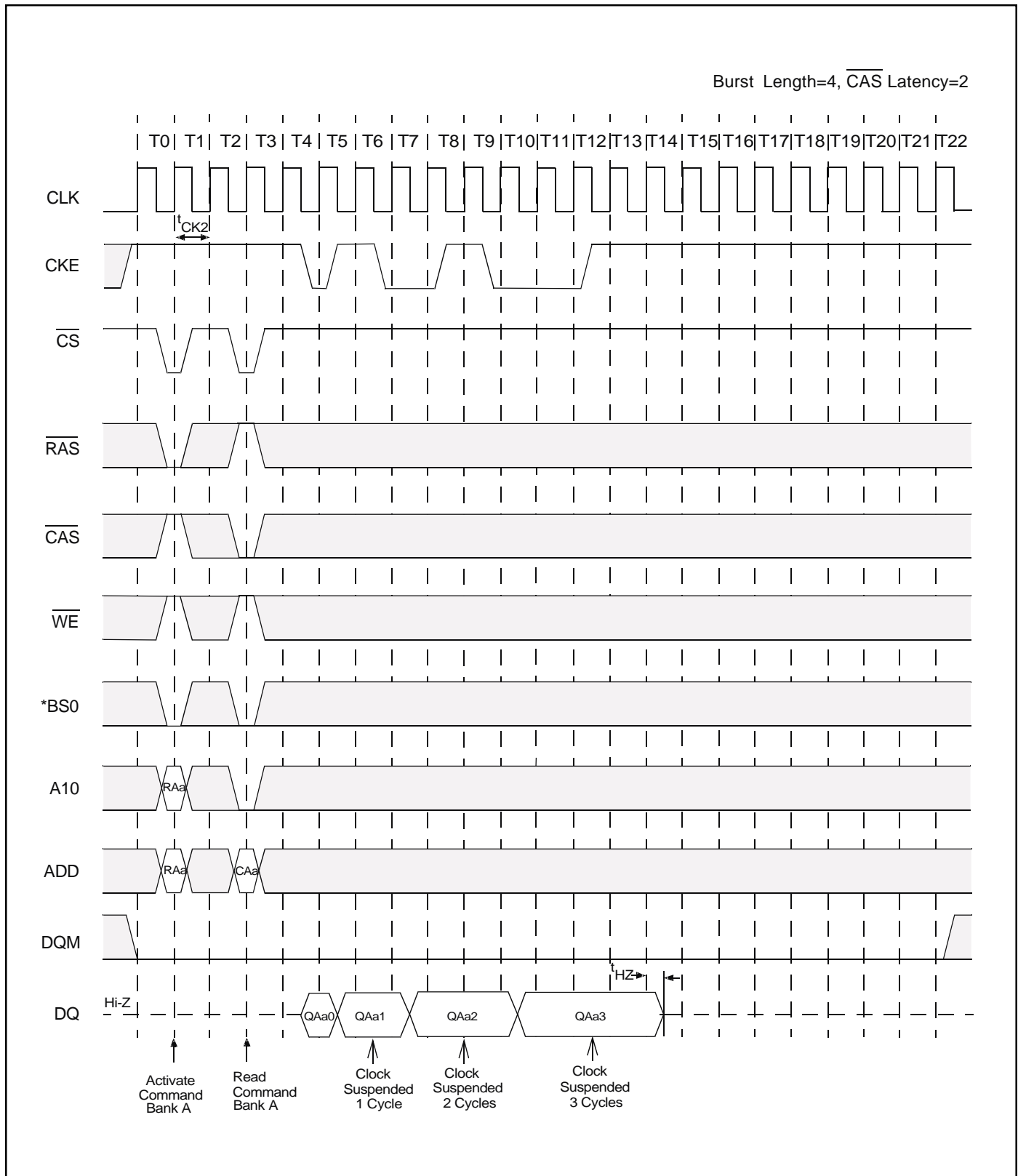


BS1="L", Bank C,D = Idle

Power on Sequence and Auto Refresh (CBR)

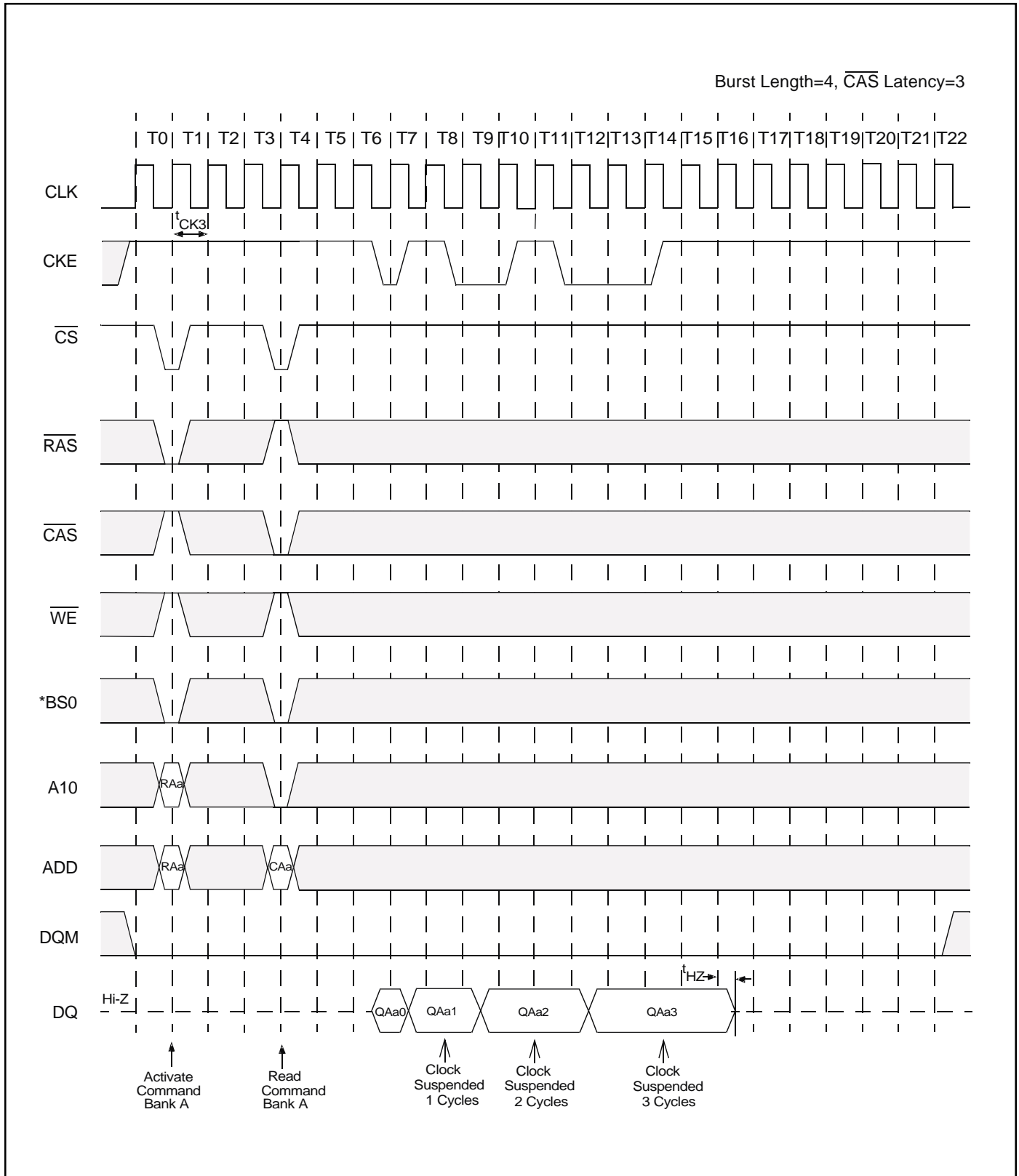


Clock Suspension During Burst Read (Using CKE) (1 of 2)



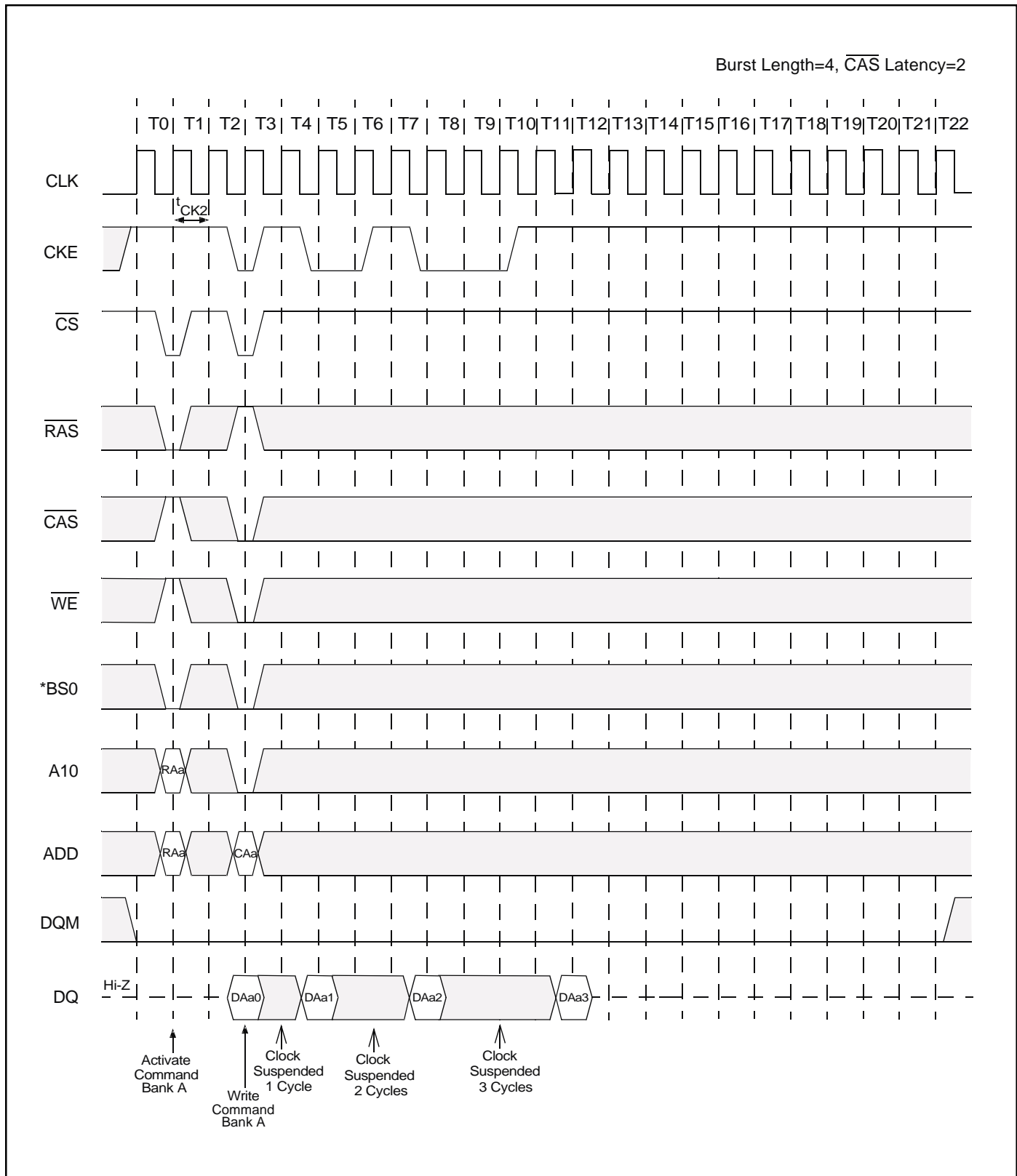
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Read (Using CKE) (2 of 2)



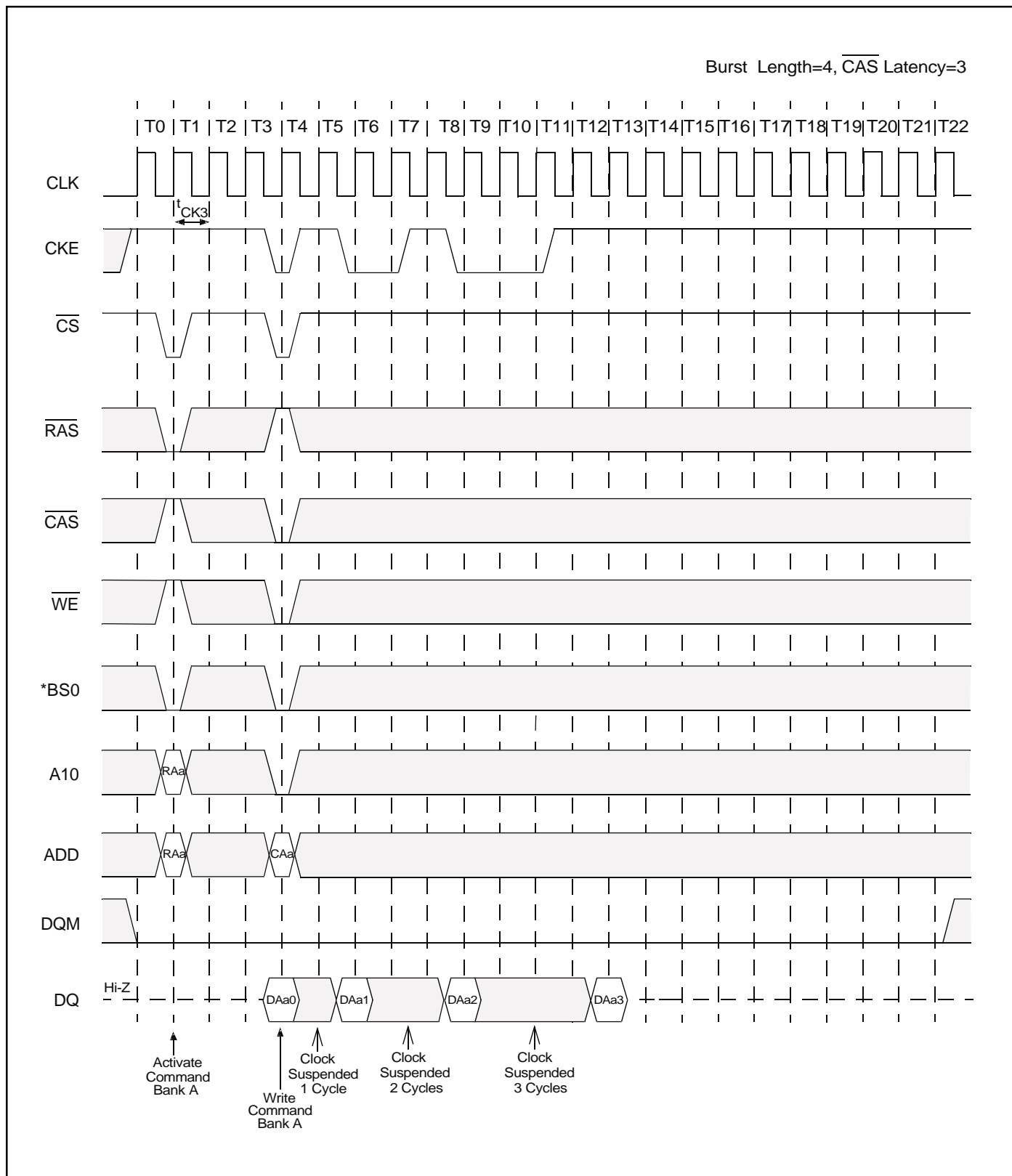
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (1 of 2)



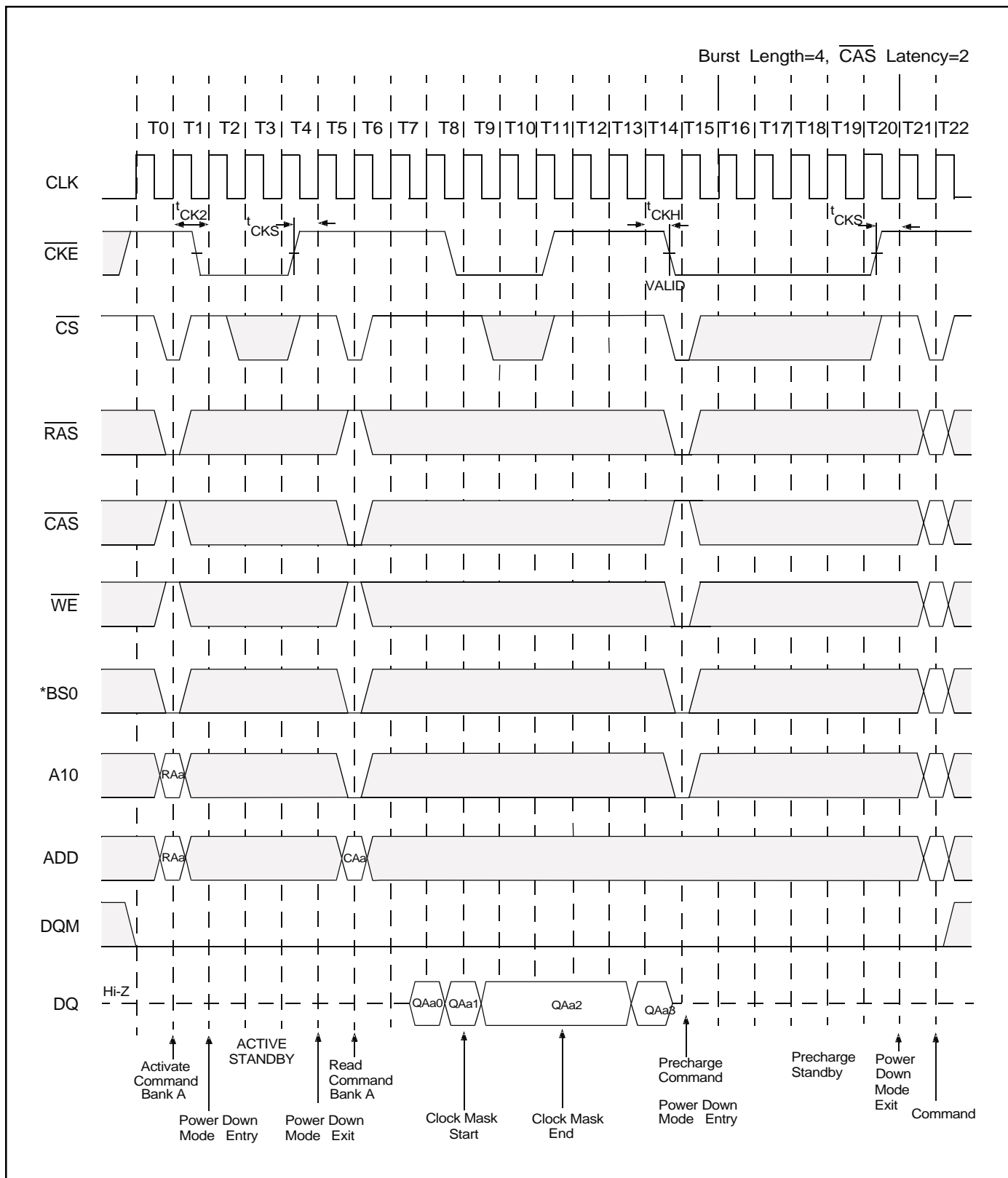
BS1="L", Bank C,D = Idle

Clock Suspension During Burst Write (Using CKE) (2 of 2)



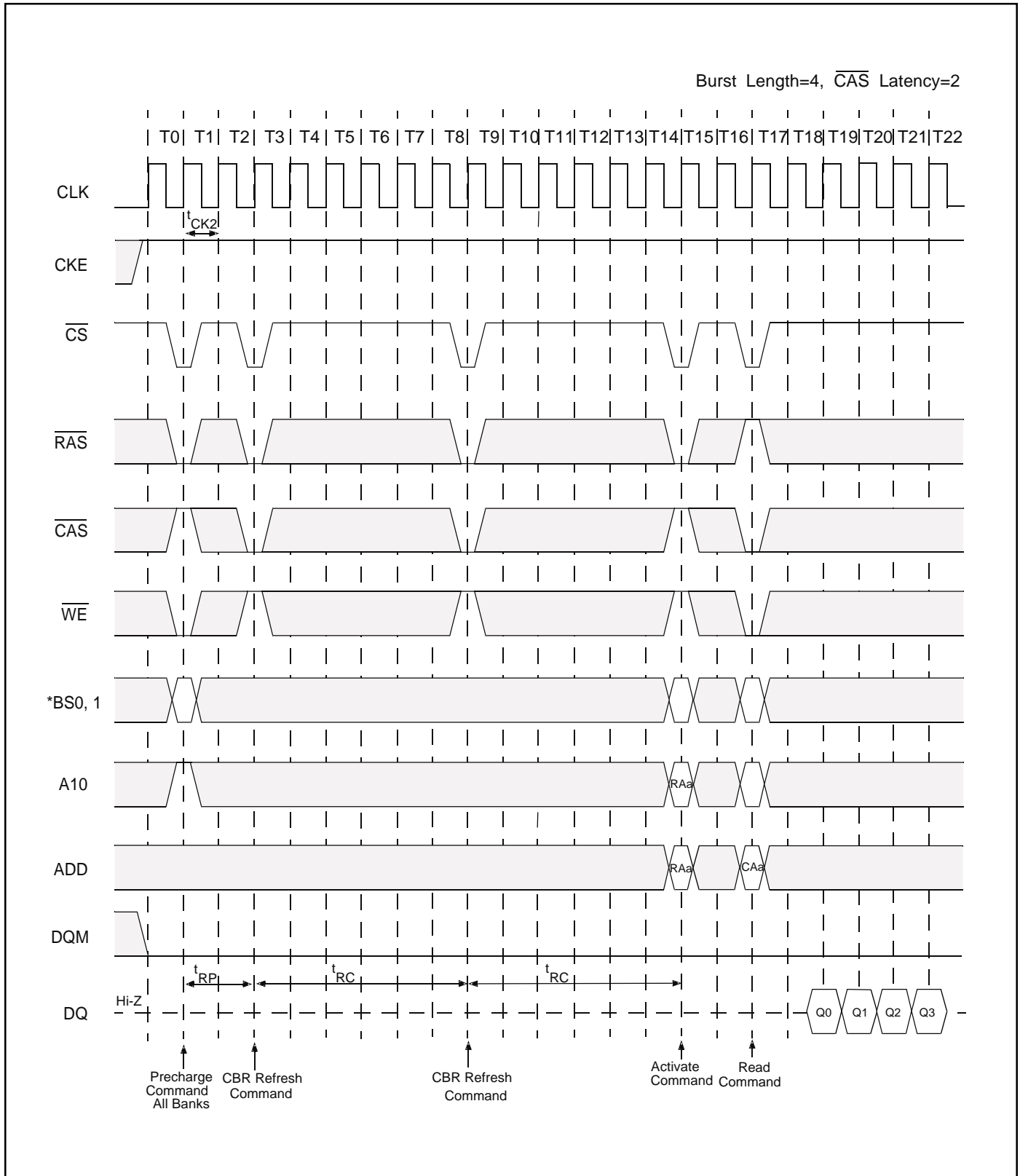
BS1="L", Bank C,D = Idle

Power Down Mode and Clock Mask



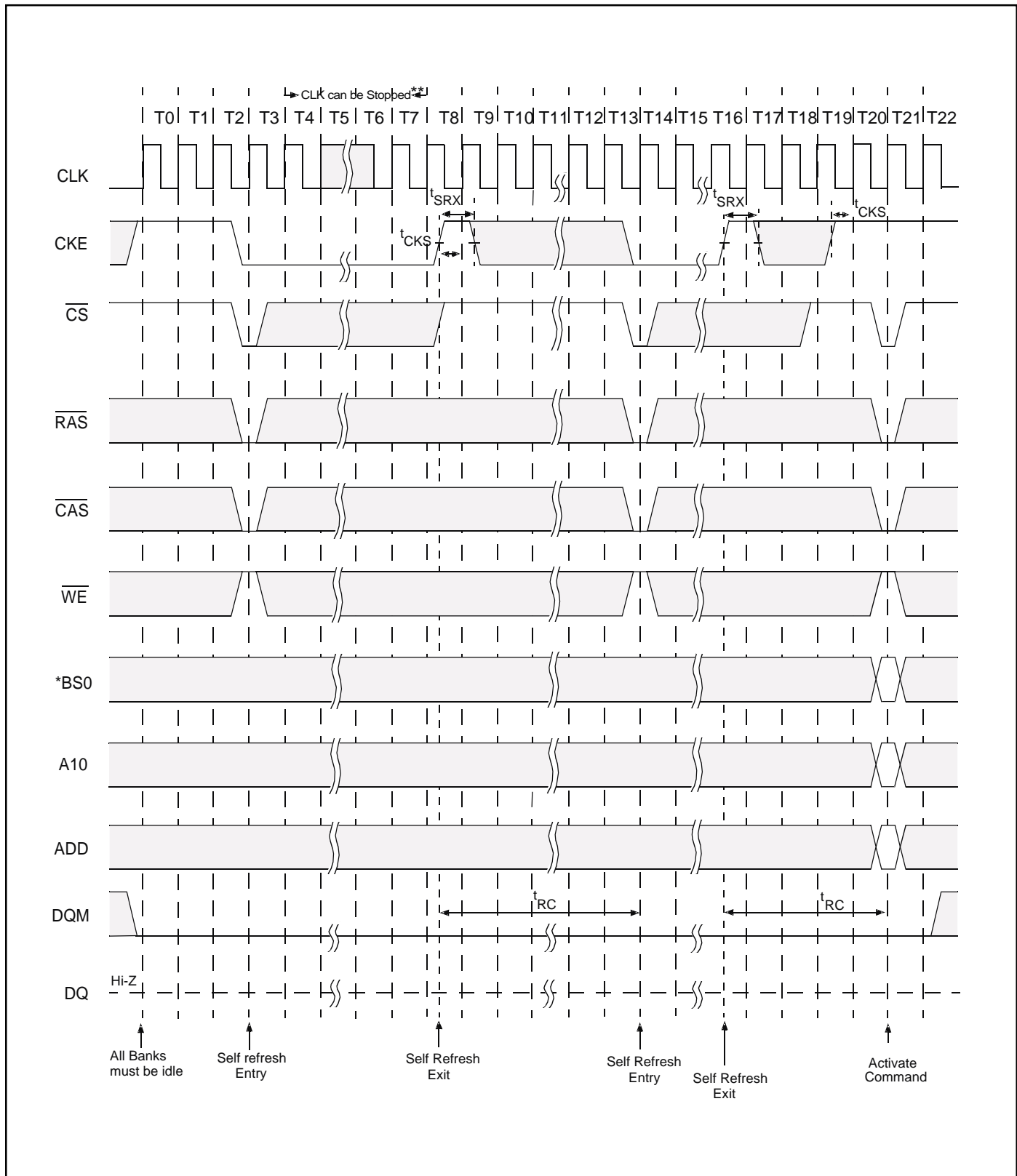
BS1="L", Bank C,D = Idle

Auto Refresh (CBR)



BS1="L", Bank C,D = Idle

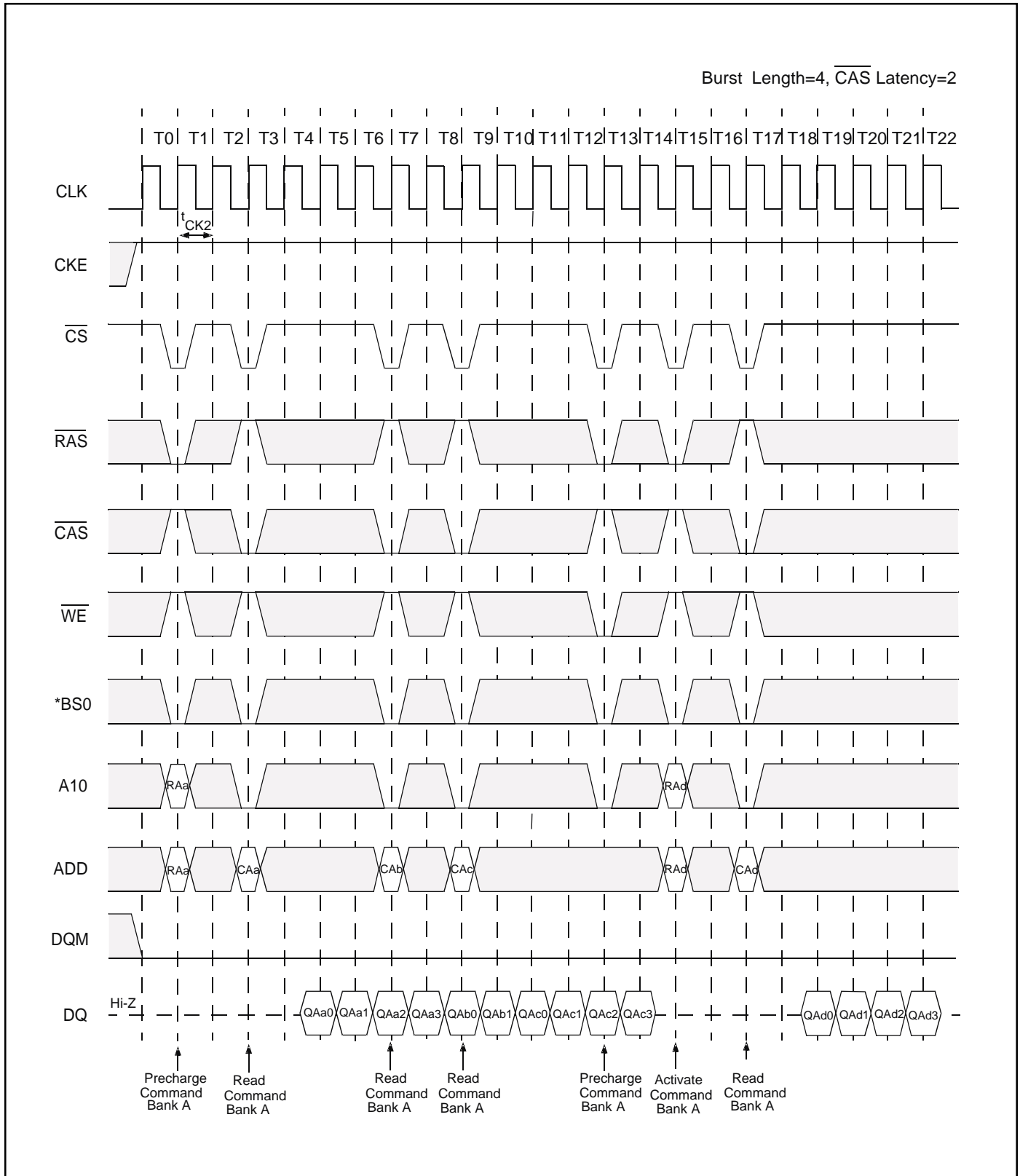
Self Refresh (Entry and Exit)



BS1="L", Bank C,D = Idle

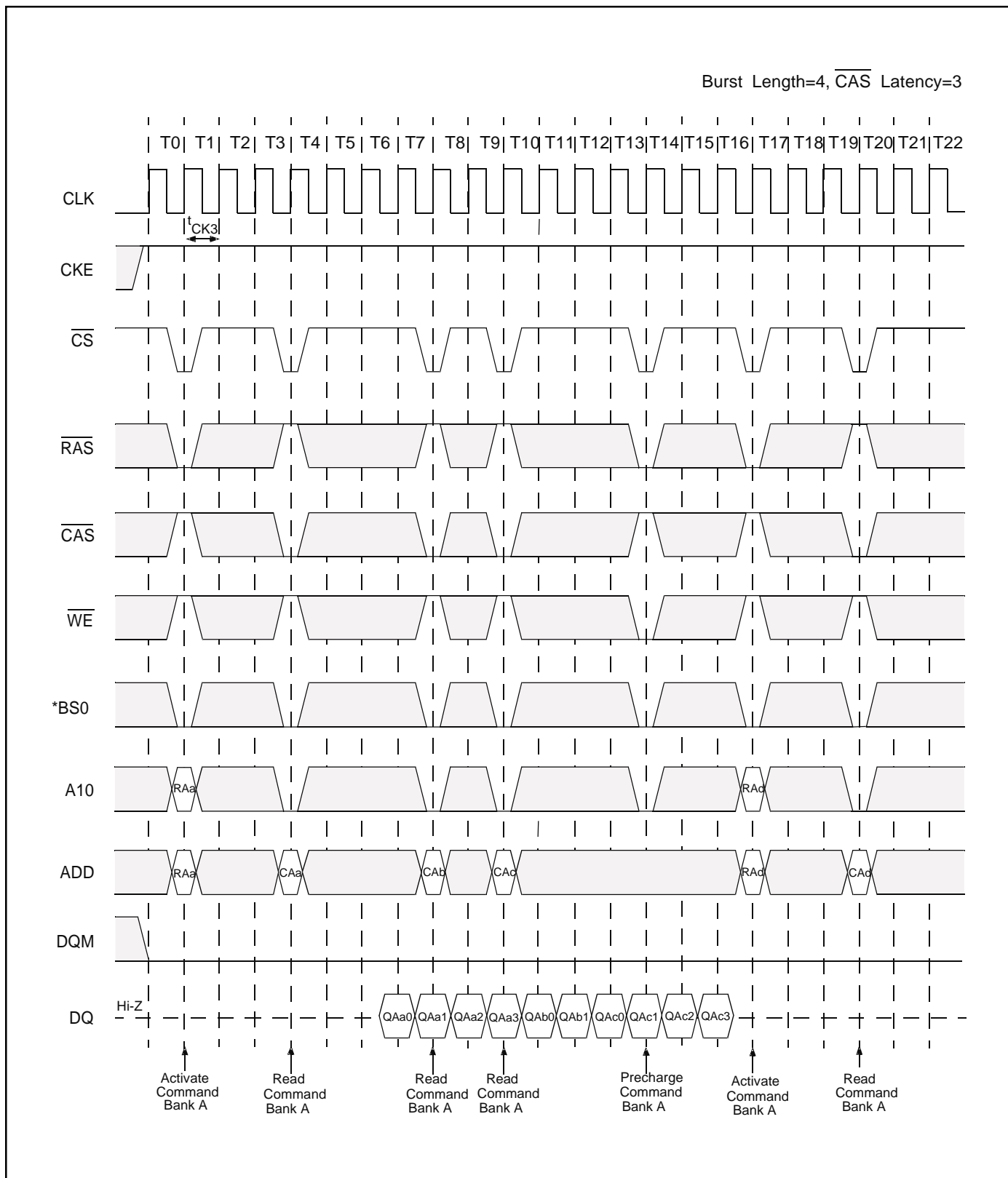
Clock can be stopped at CKE=Low. If clock is stopped, it must be restarted/stable for 4 clock cycles before CKE=High

Random Column Read (Page With Same Bank) (1 of 2)



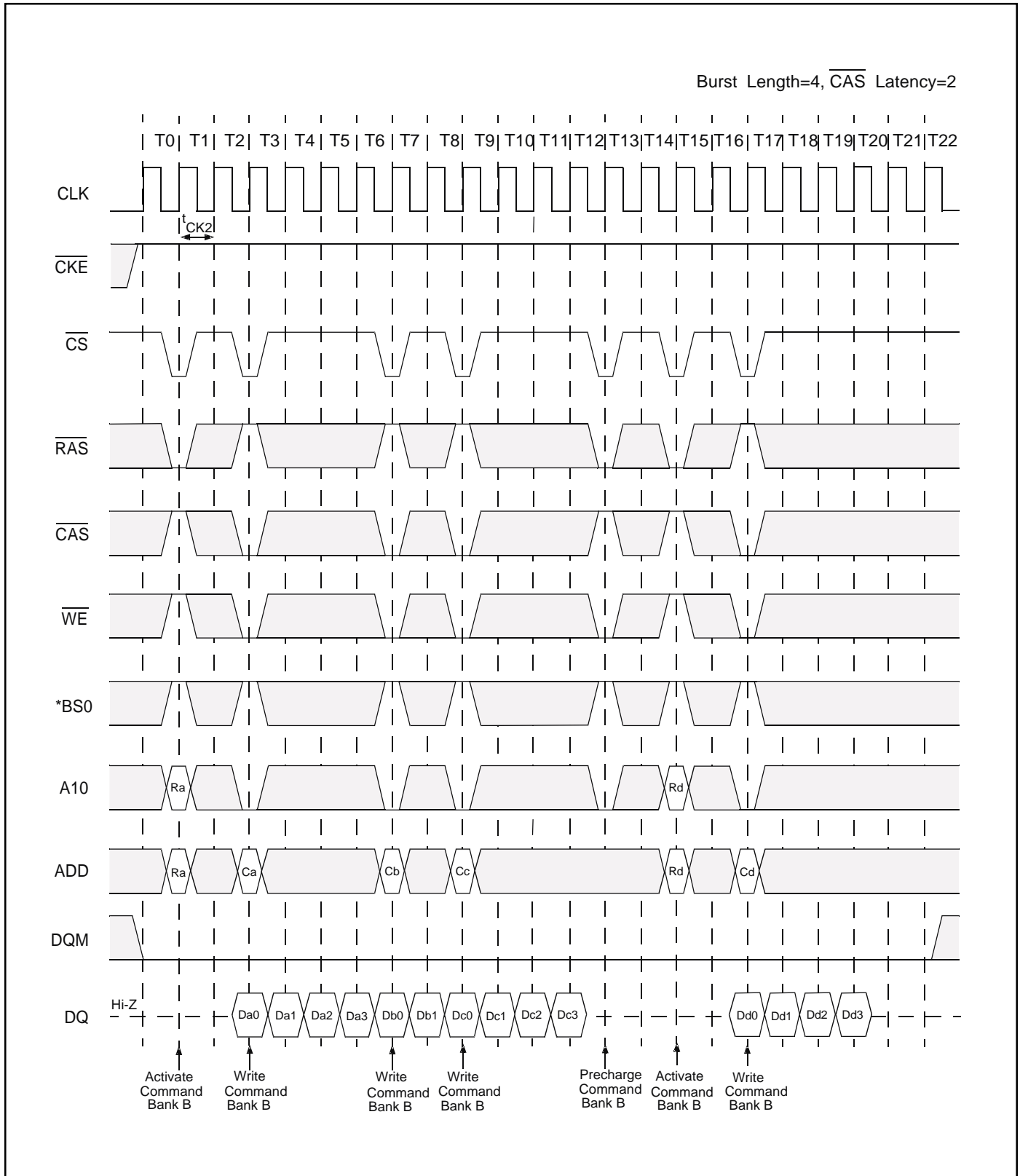
BS1="L", Bank C,D = Idle

Random Column Read (Page With Same Bank) (2 of 2)



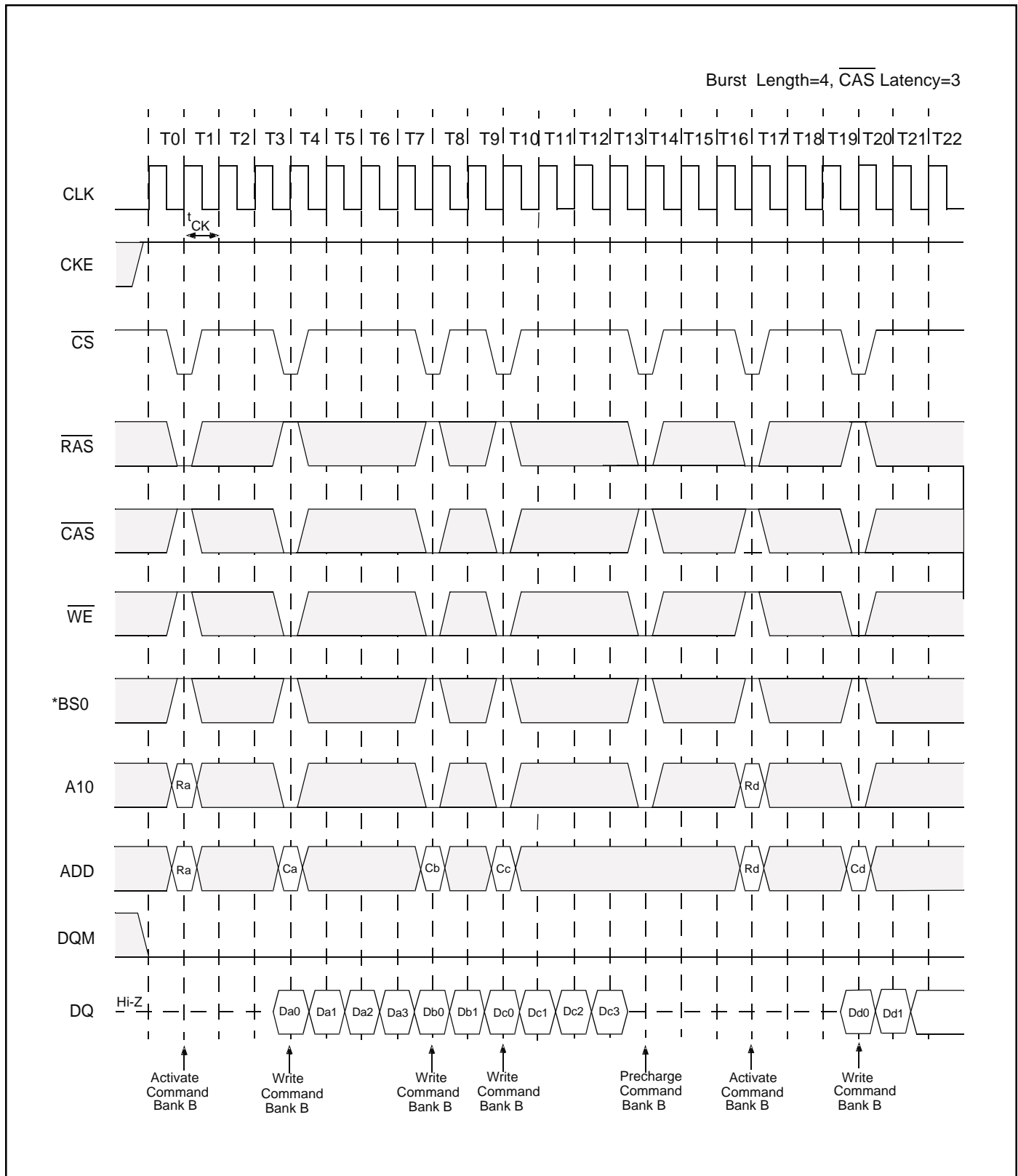
BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



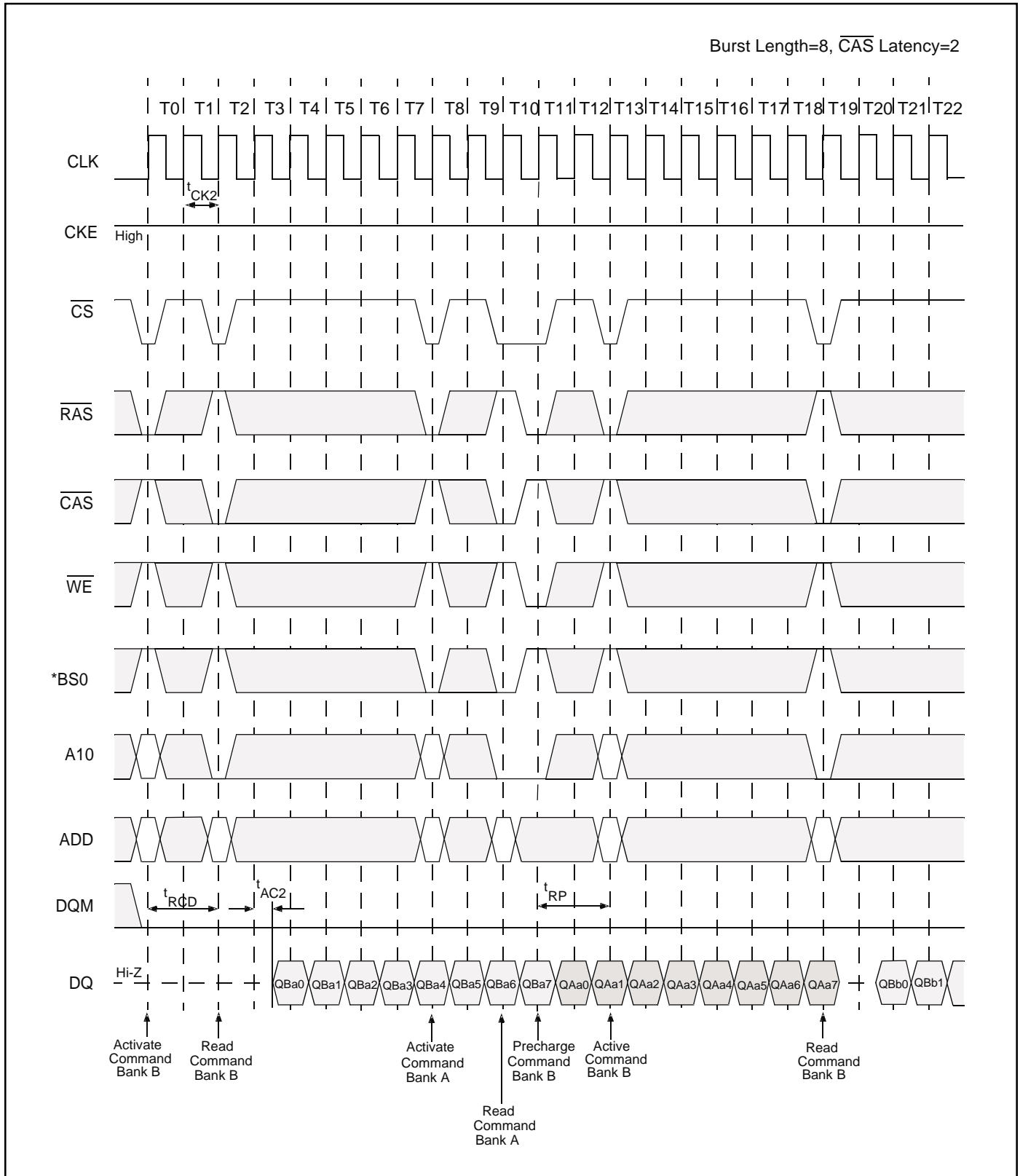
BS1="L", Bank C,D = Idle

Random Column Write (Page With Same Bank) (1 of 2)



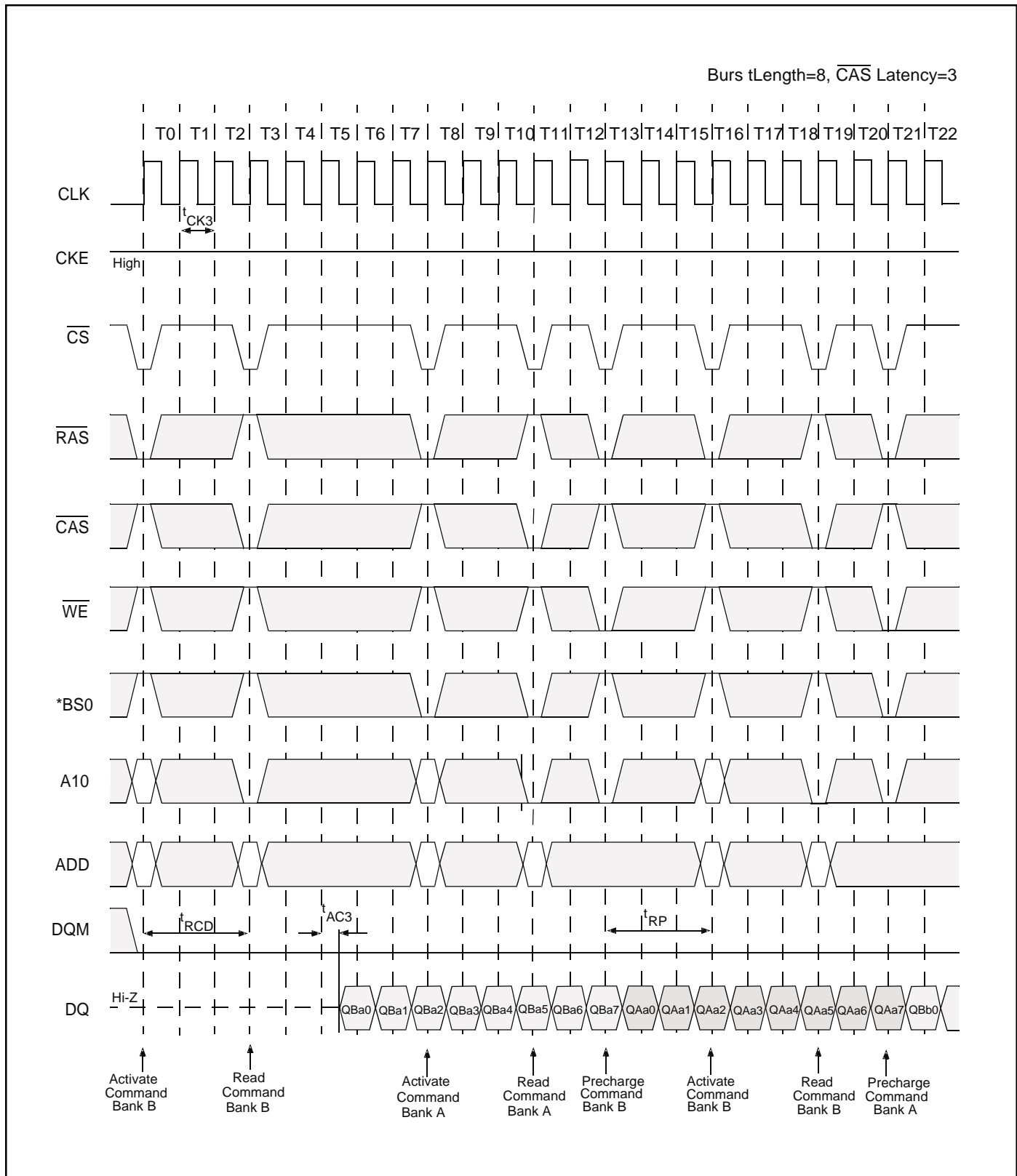
BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (1 of 2)



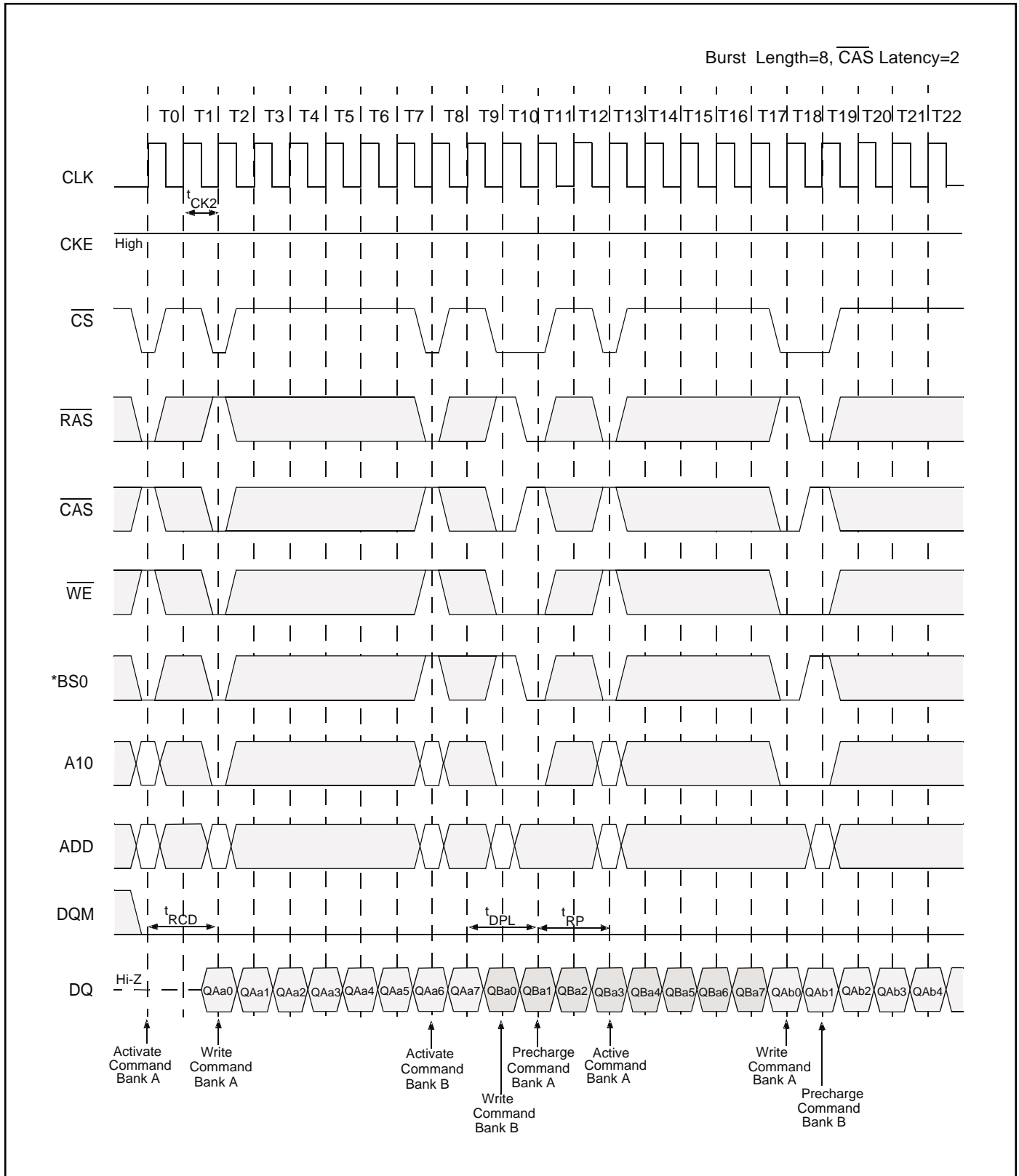
BS1="L", Bank C,D = Idle

Random Row Read (Interleaving Banks) (2 of 2)



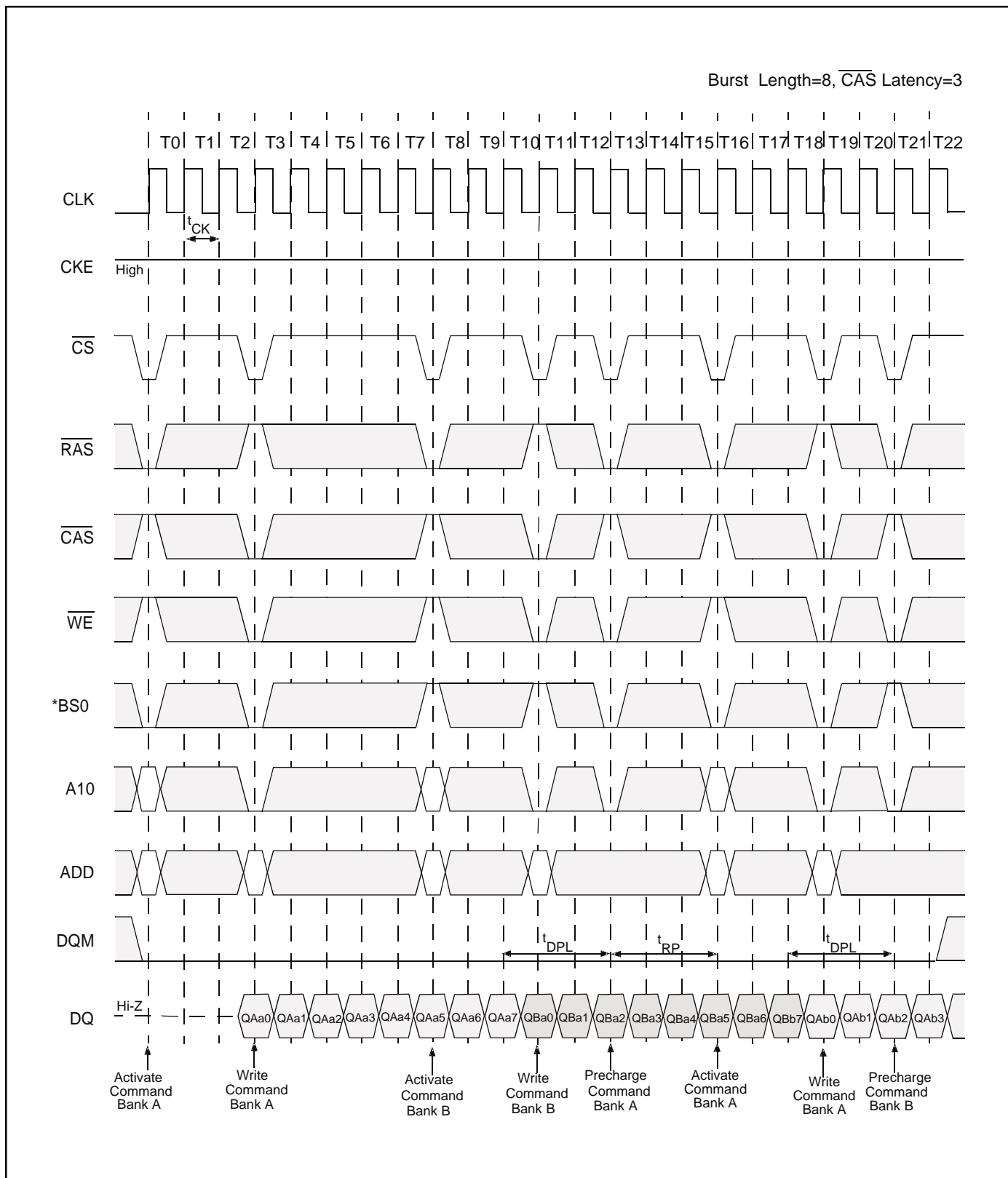
BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (1 of 2)



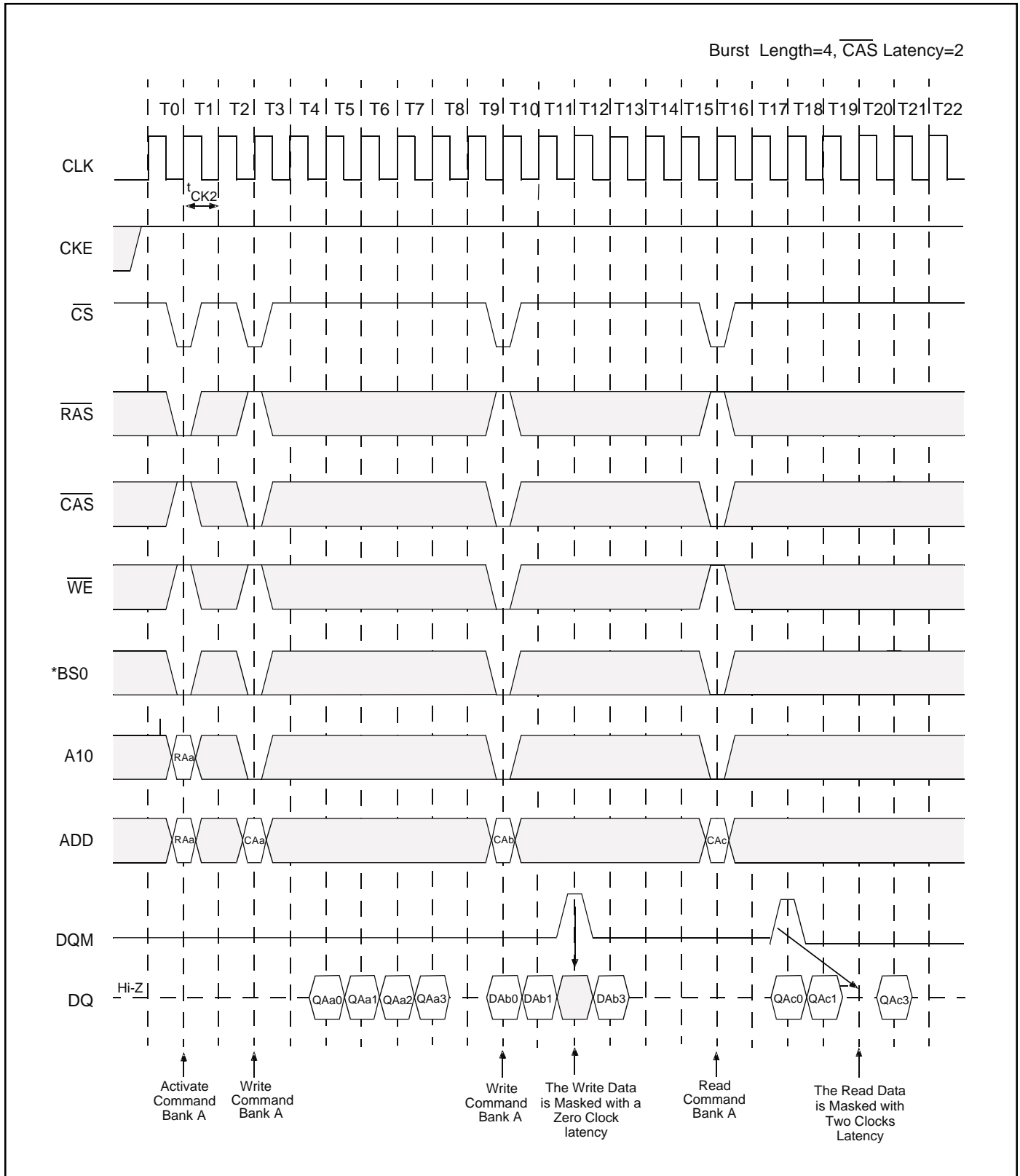
BS1="L", Bank C,D = Idle

Random Row Write (Interleaving Banks) (2 of 2)



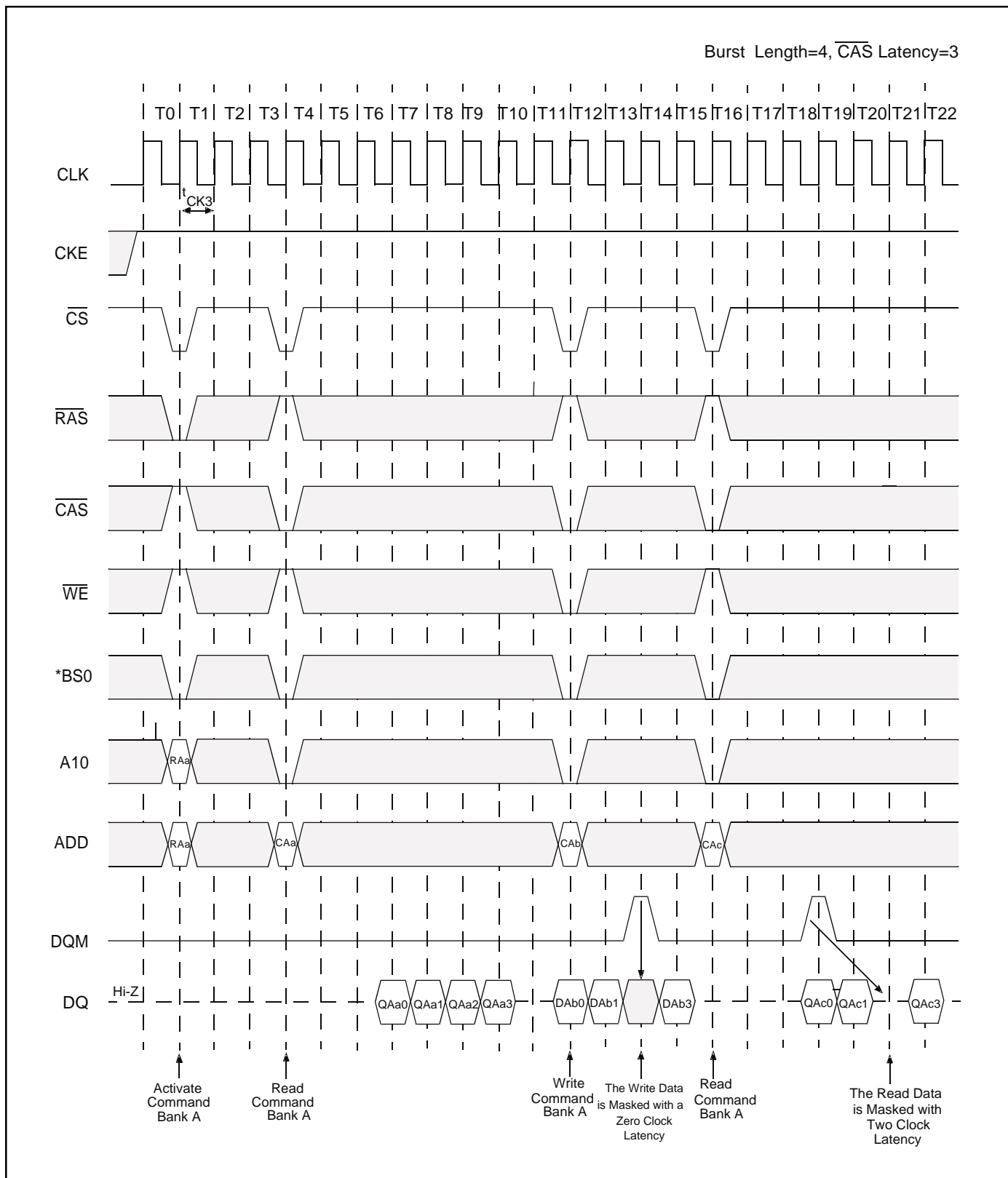
BS1="L", Bank C,D = Idle

Read and Write Cycle (1 of 2)



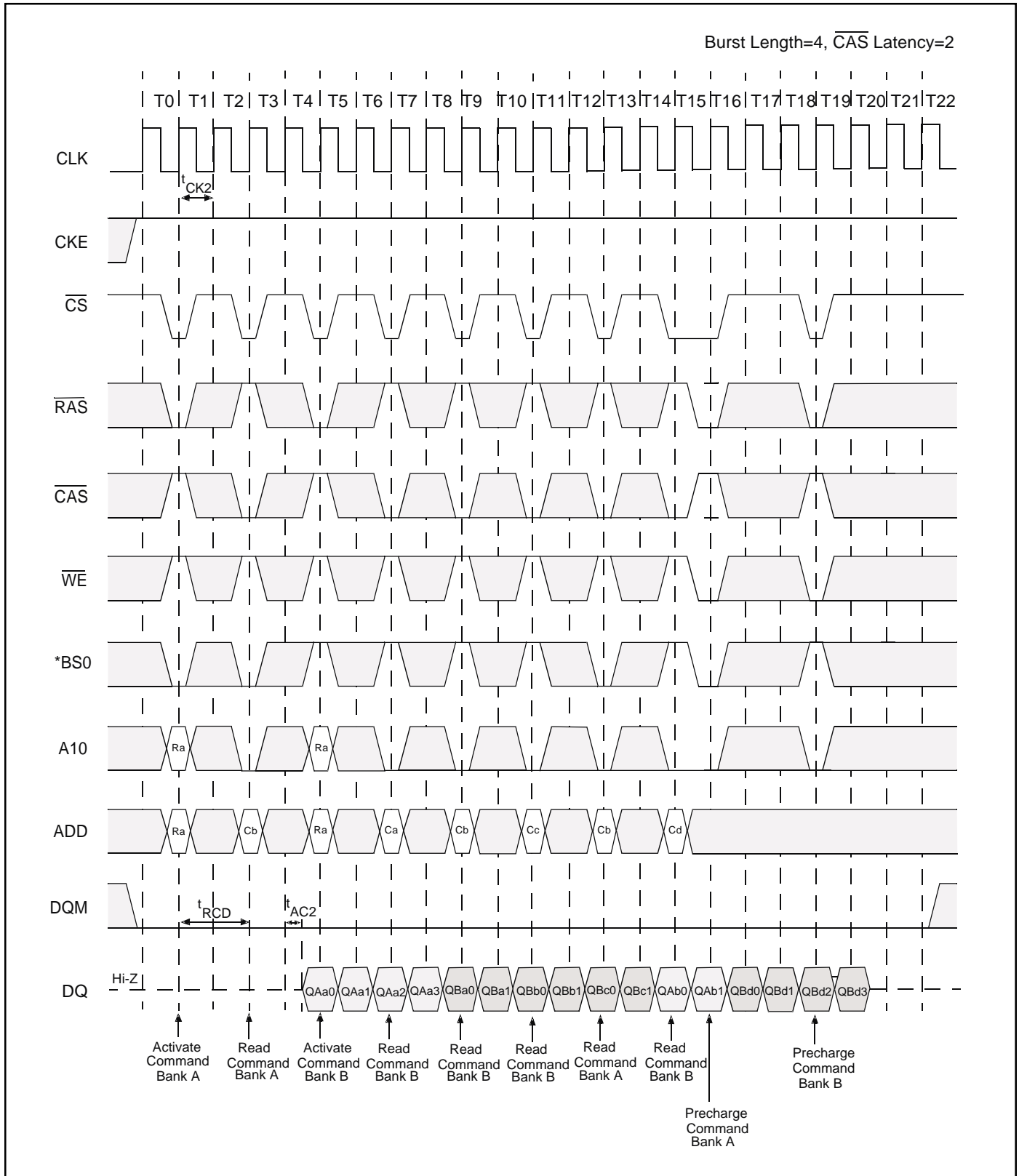
BS1="L", Bank C,D = Idle

Read and Write Cycle (2 of 2)



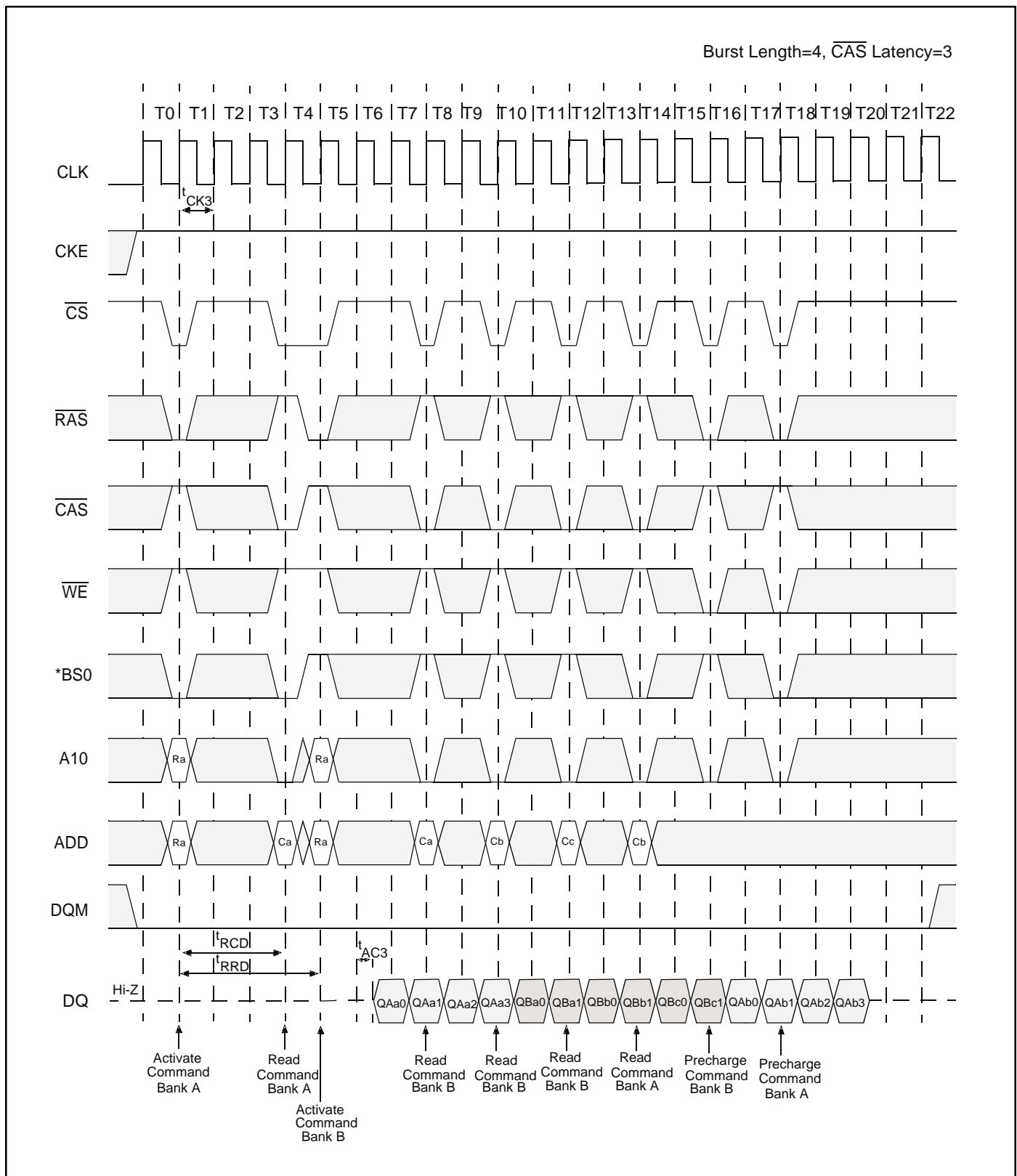
BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (1 of 2)



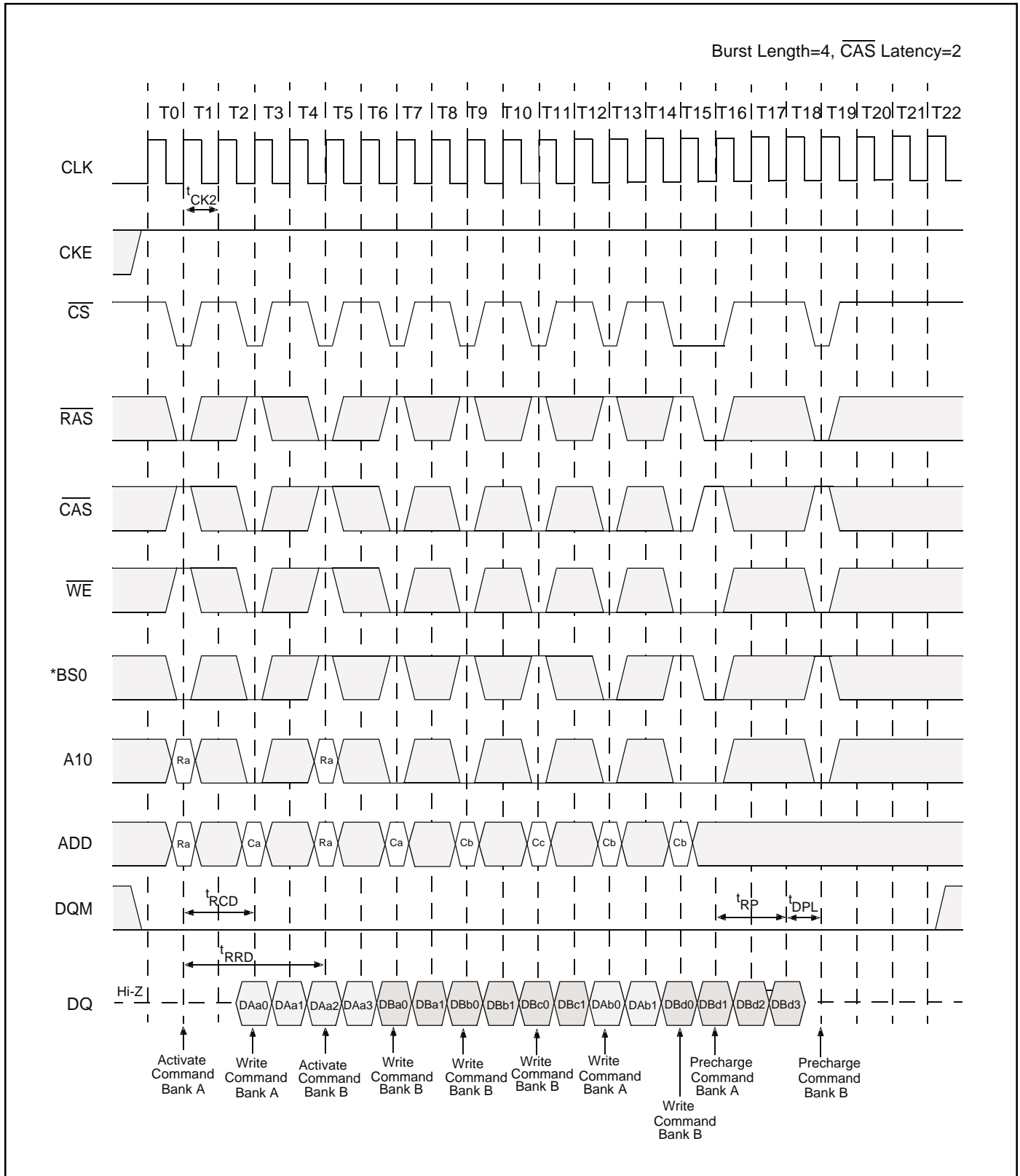
BS1="L", Bank C,D = Idle

Interleaved Column Read Cycle (2 of 2)



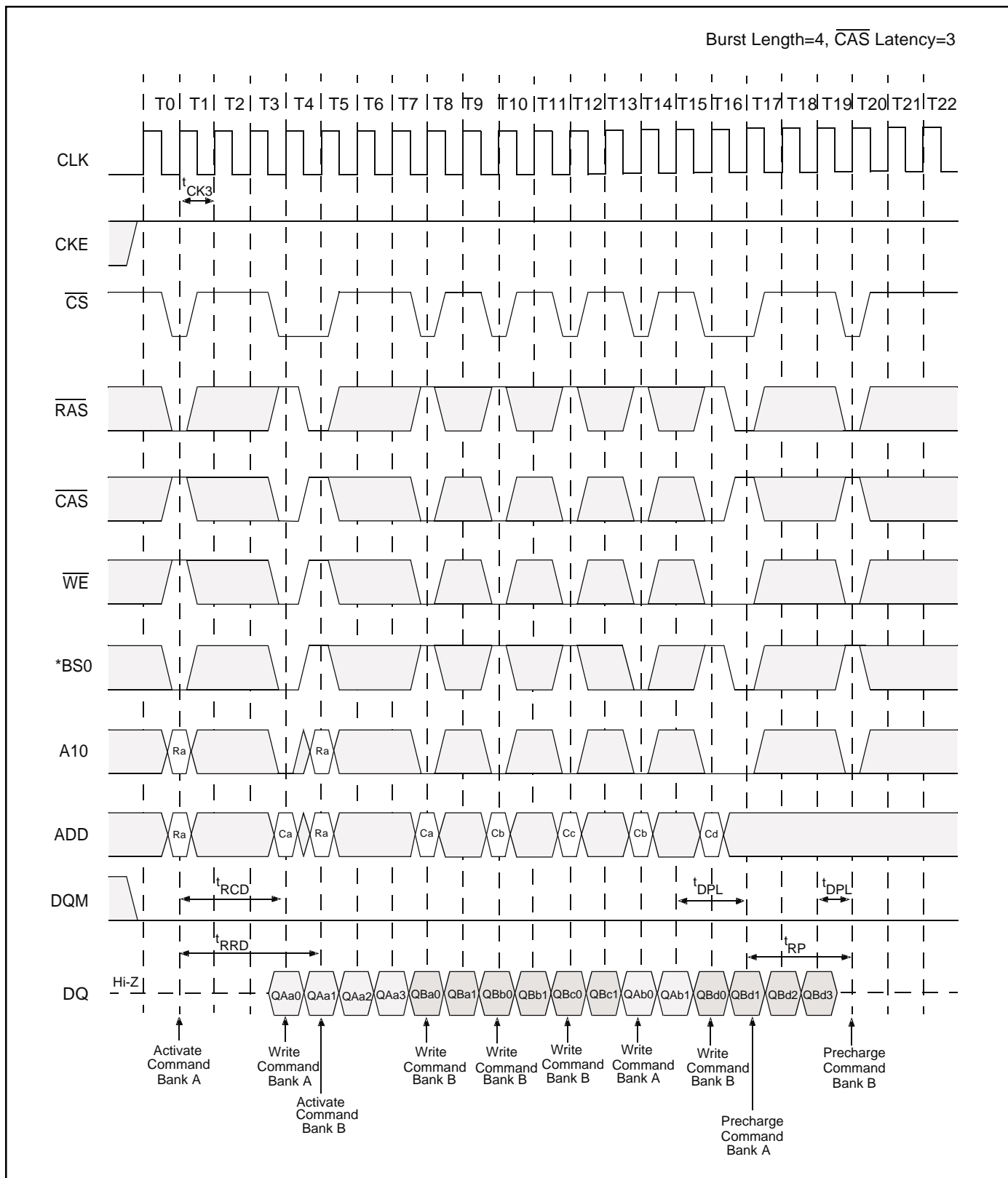
BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (1 of 2)



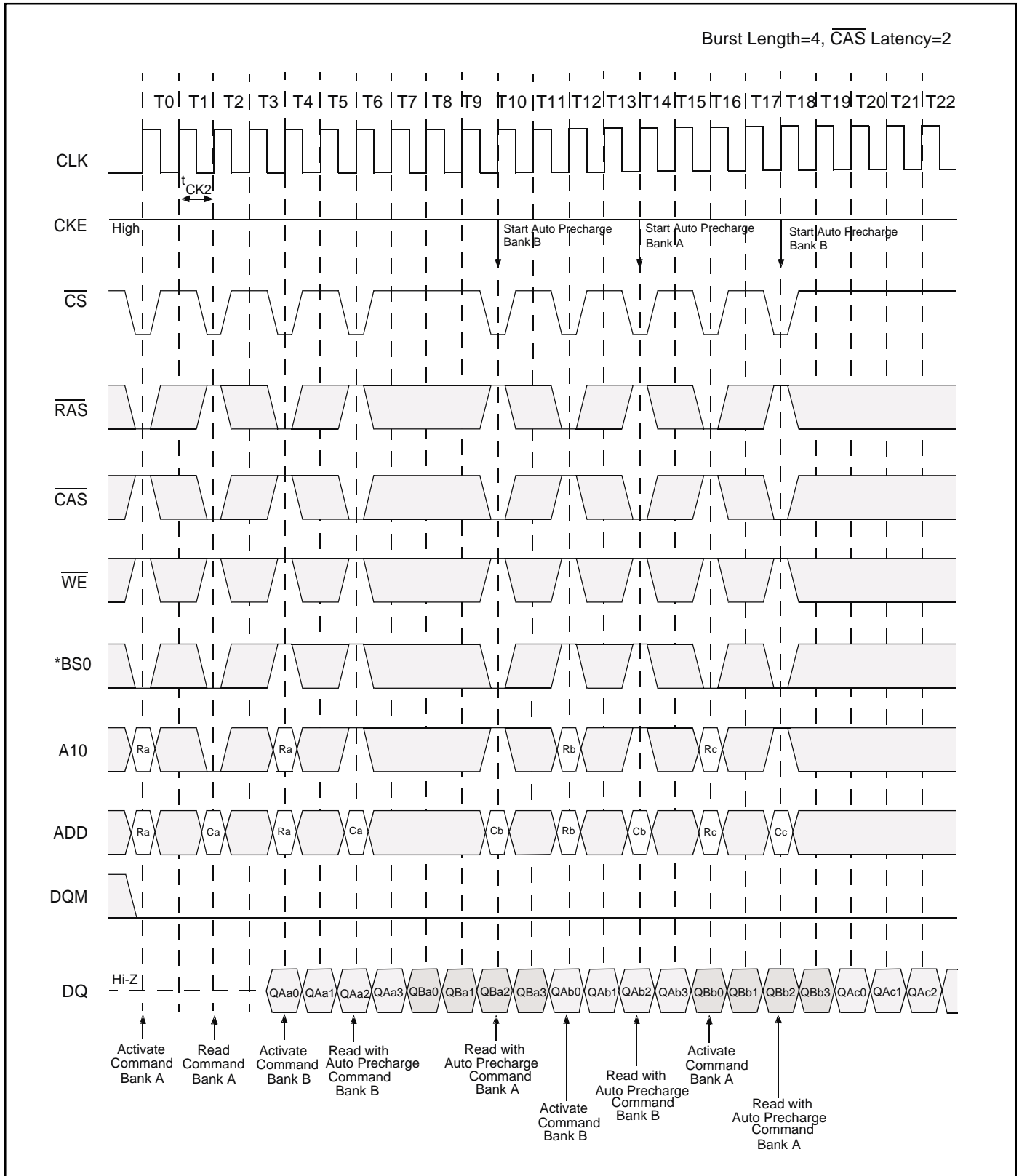
BS1="L", Bank C,D = Idle

Interleaved Column Write Cycle (2 of 2)



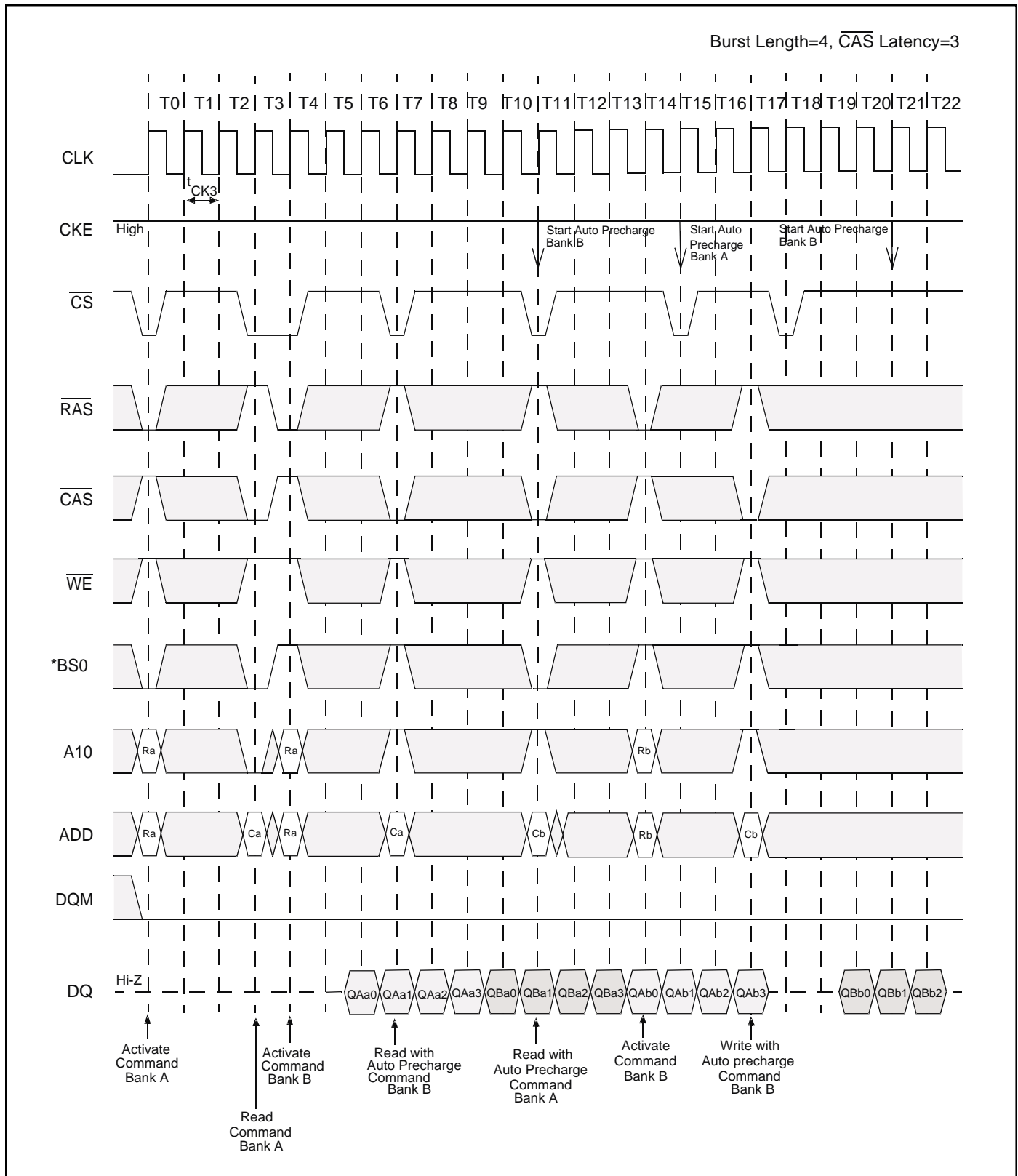
BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (1 of 2)



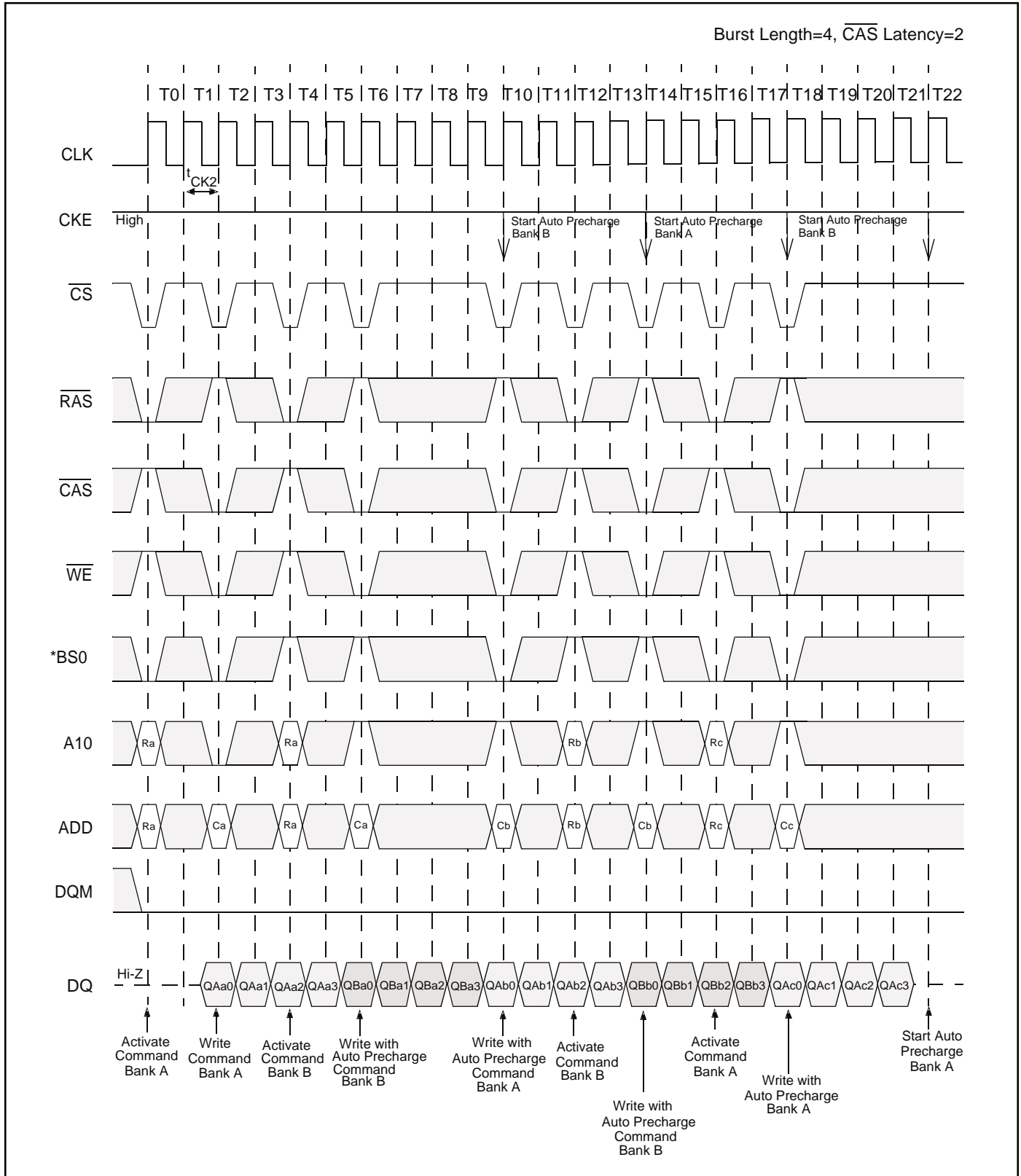
BS1="L", Bank C,D = Idle

Auto Precharge after Read Burst (2 of 2)



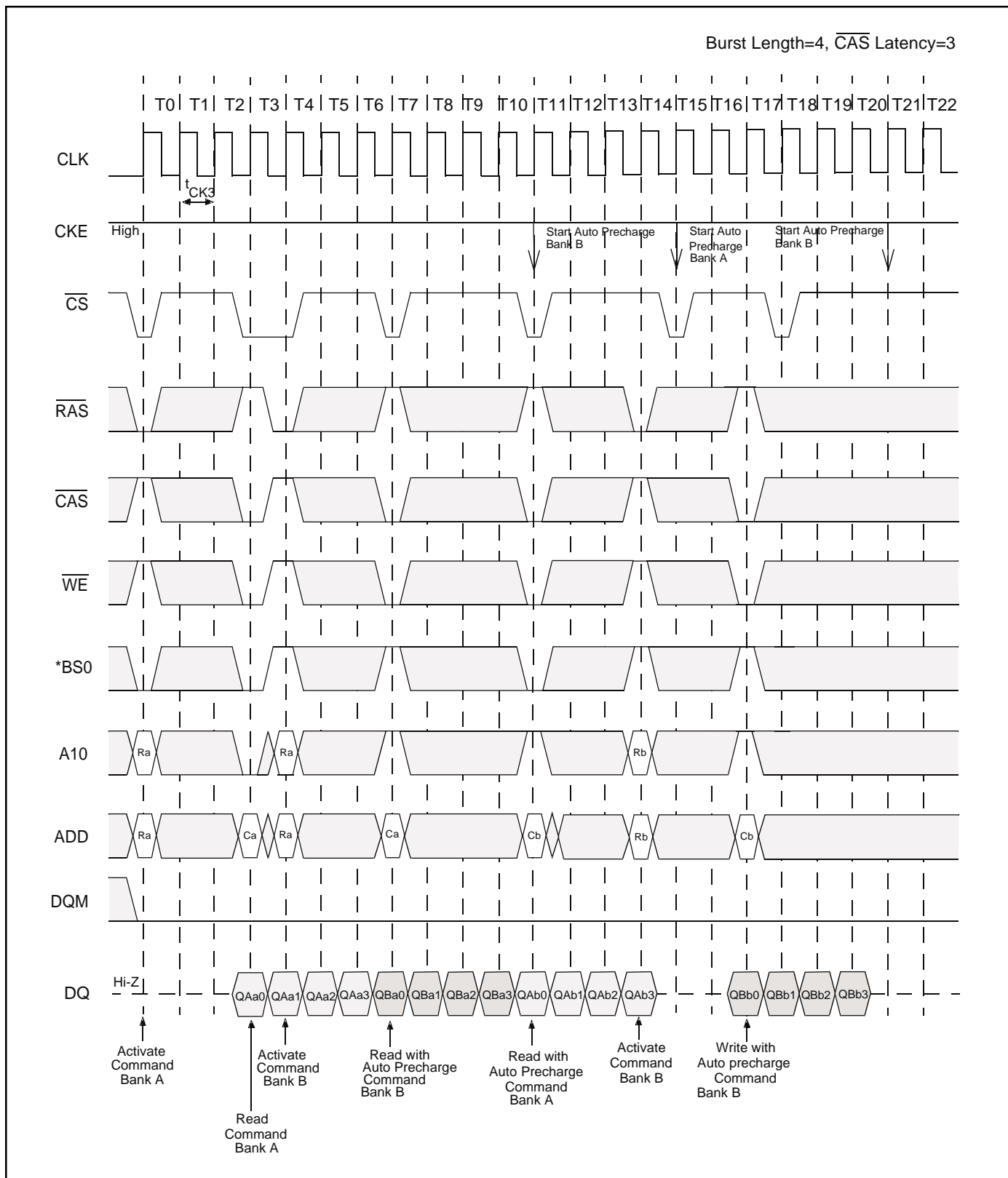
BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (1 of 2)



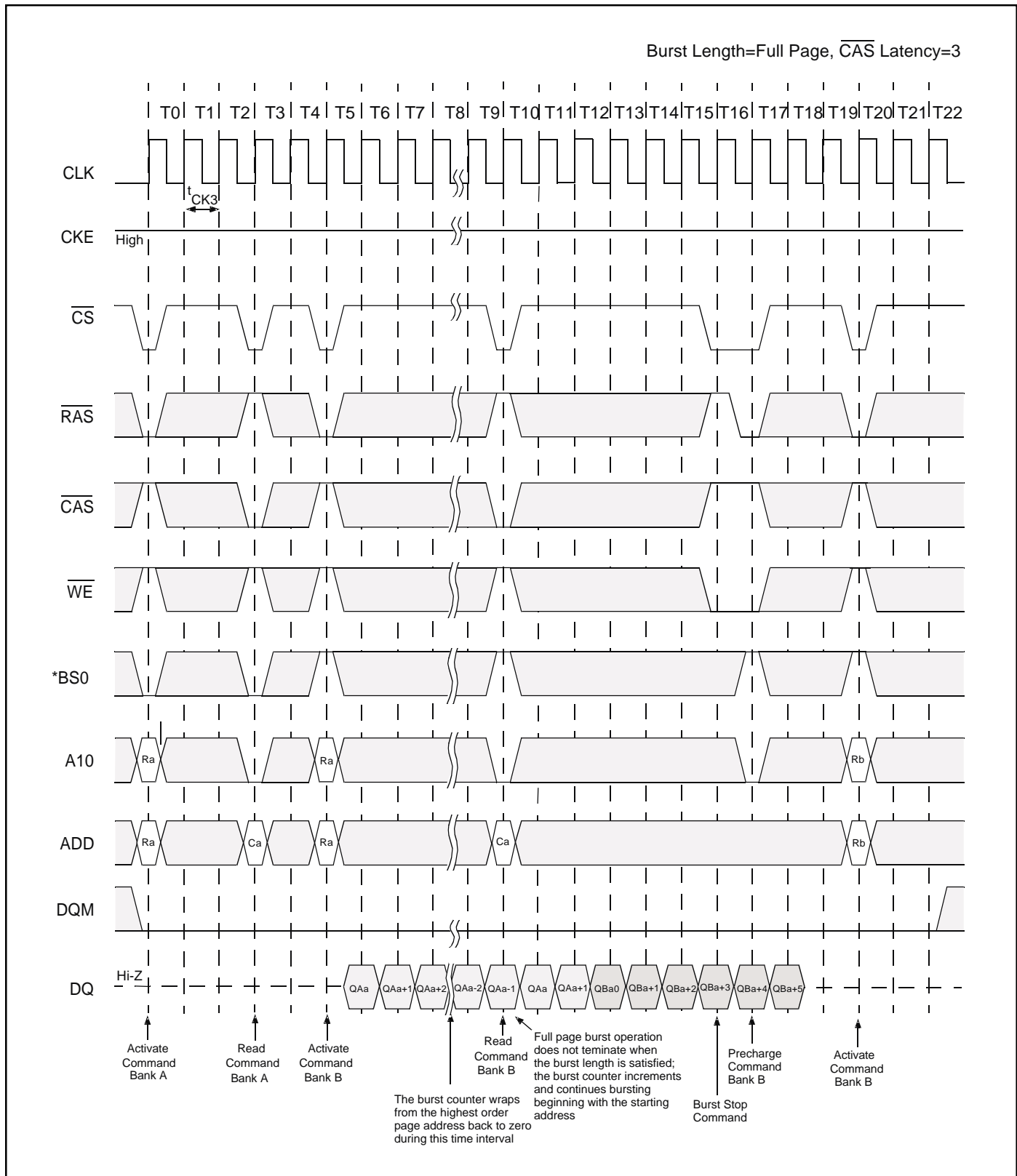
BS1="L", Bank C,D = Idle

Auto Precharge after Write Burst (2 of 2)



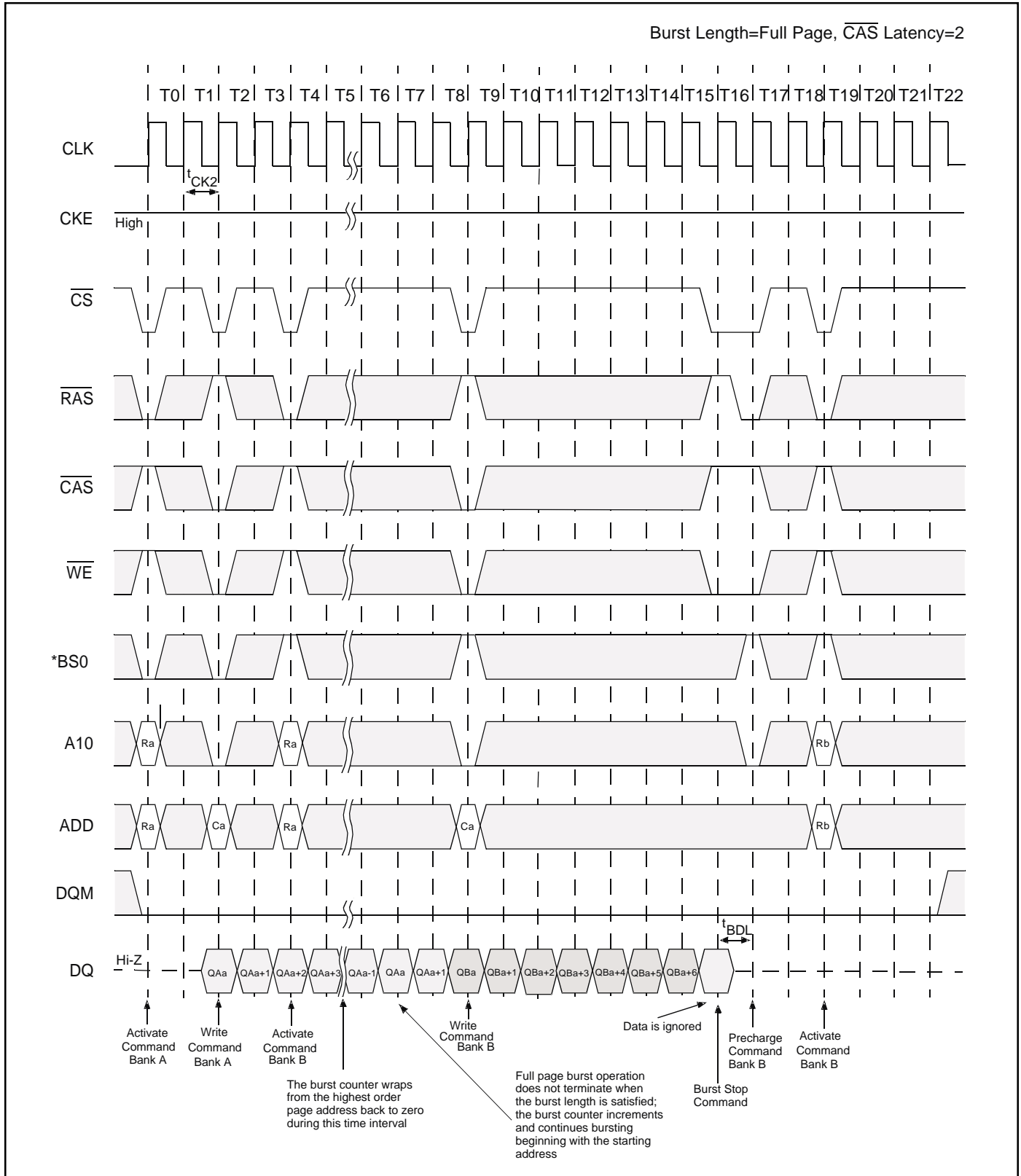
BS1="L", Bank C,D = Idle

Full Page Read Cycle (2 of 2)



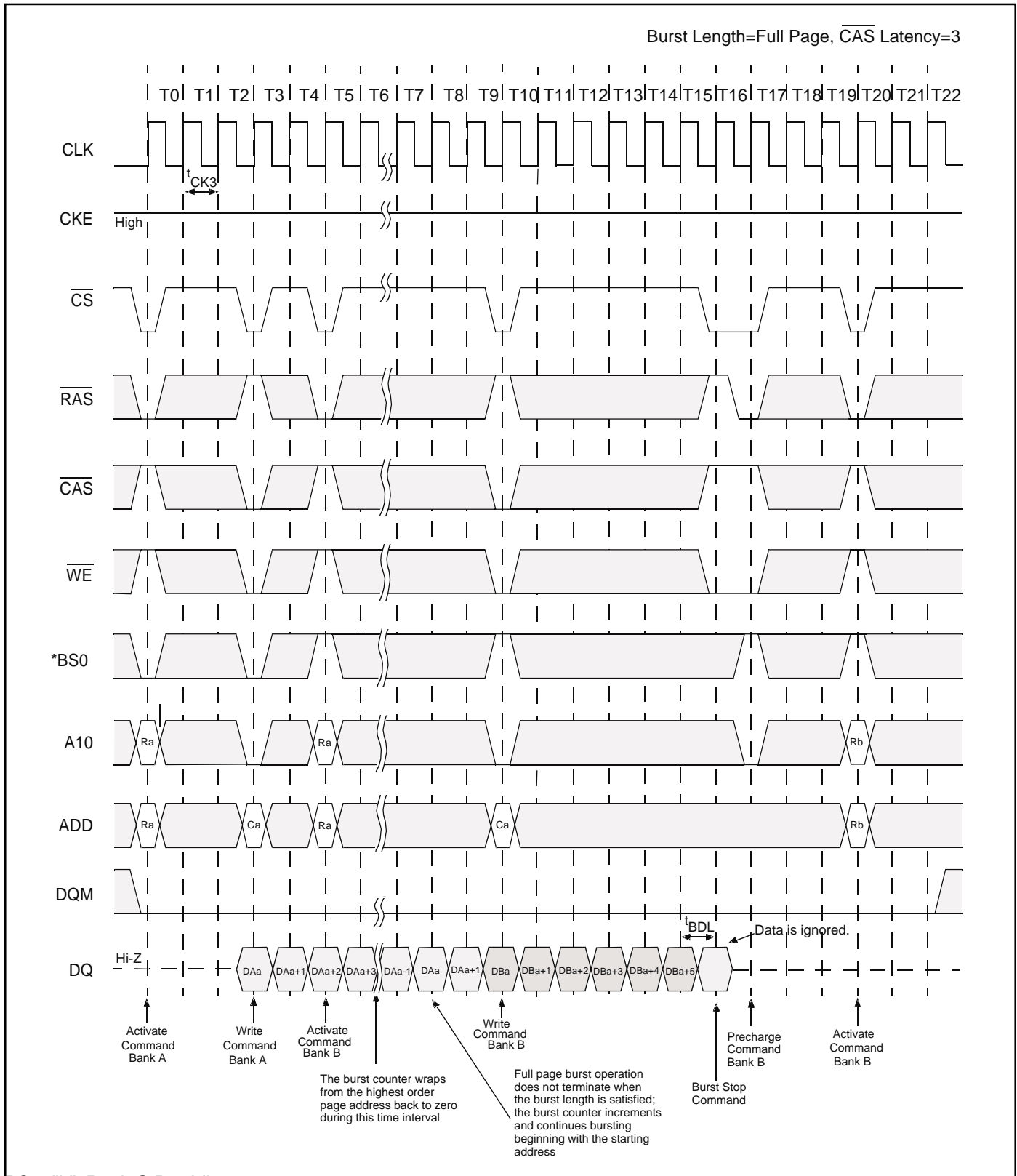
BS1="L", Bank C,D = Idle

Full Page Write Cycle (1 of 2)

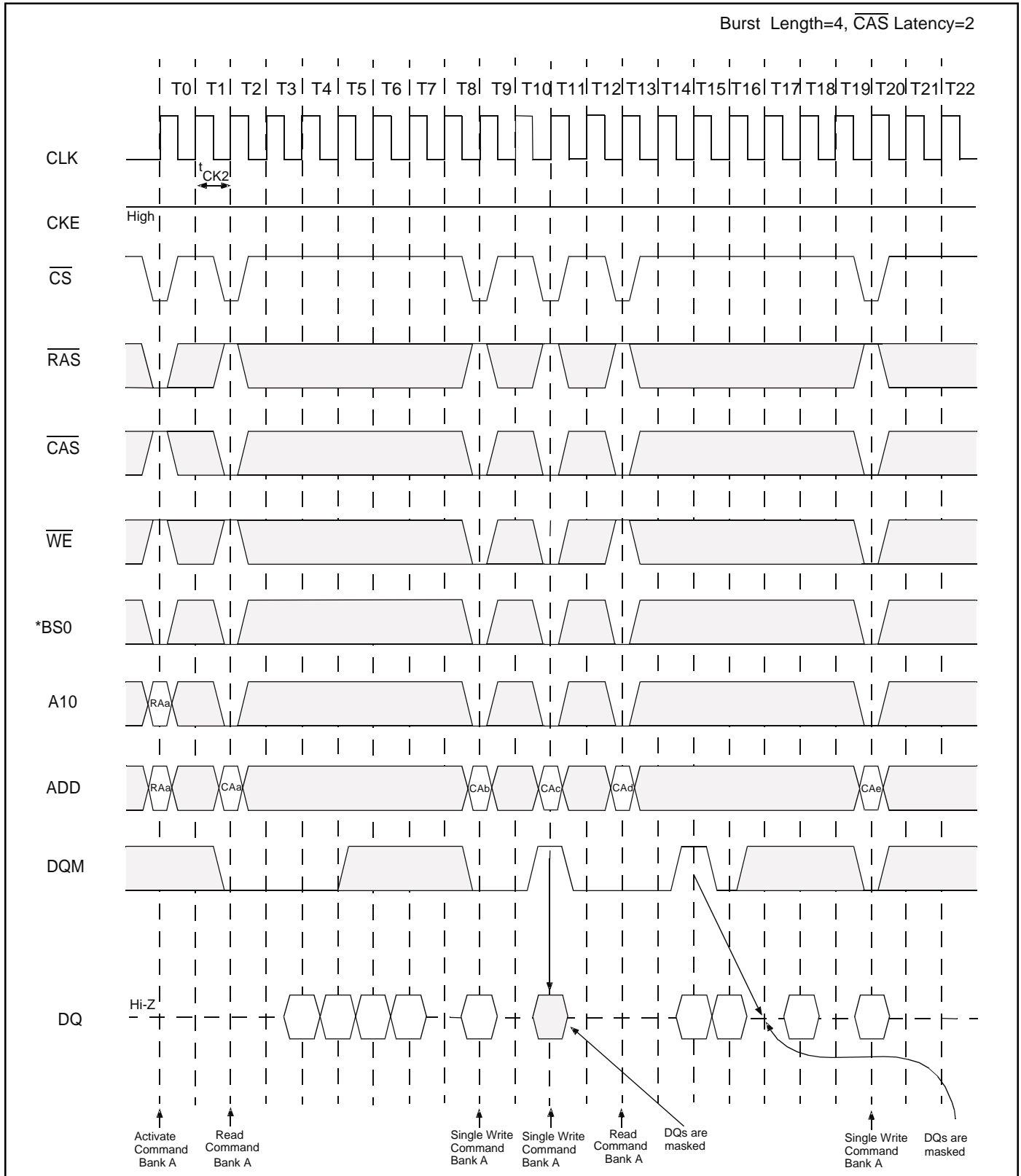


BS1="L", Bank C,D = Idle

Full Page Write Cycle (2 of 2)

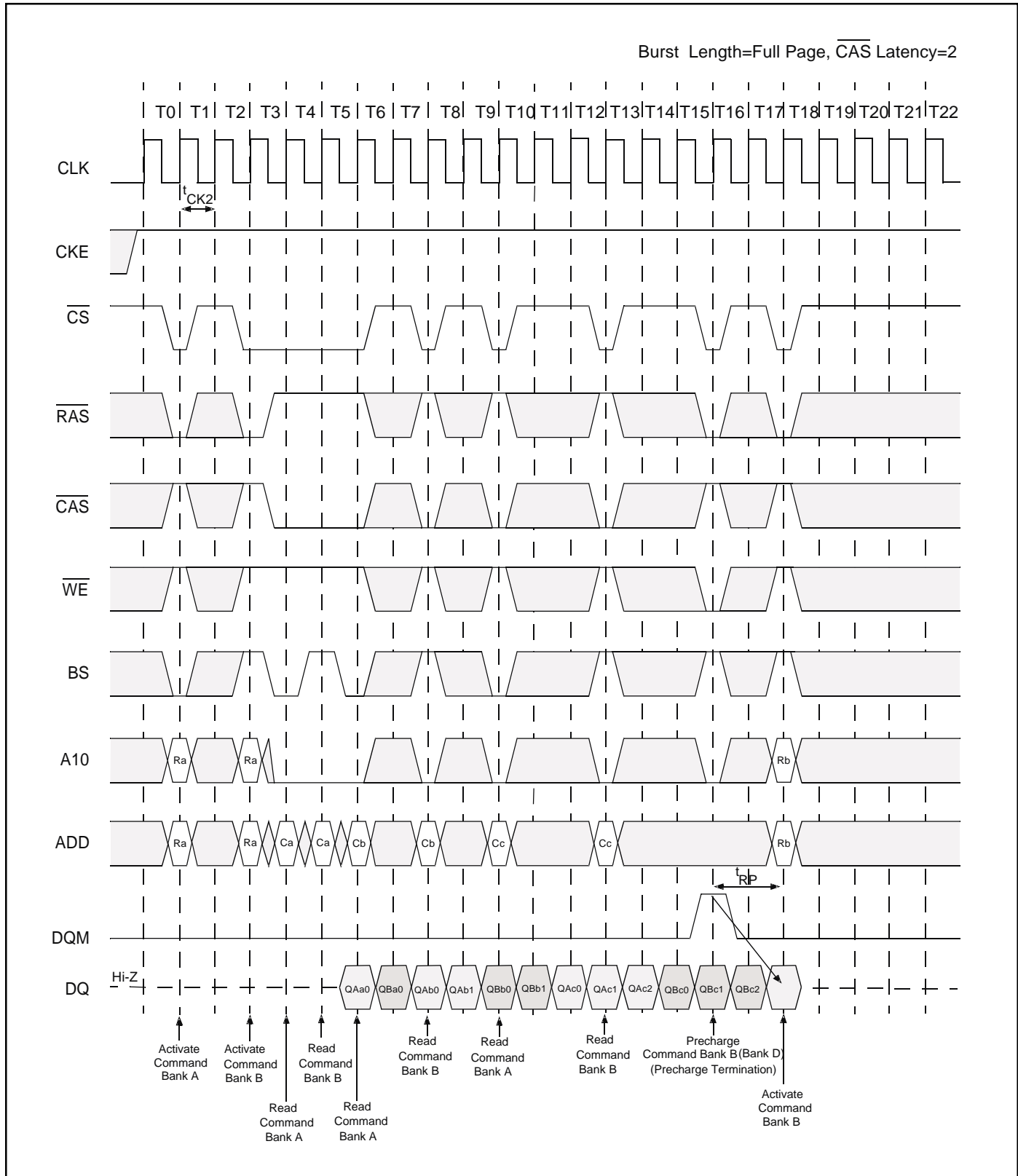


Burst Read and Single Write Operation



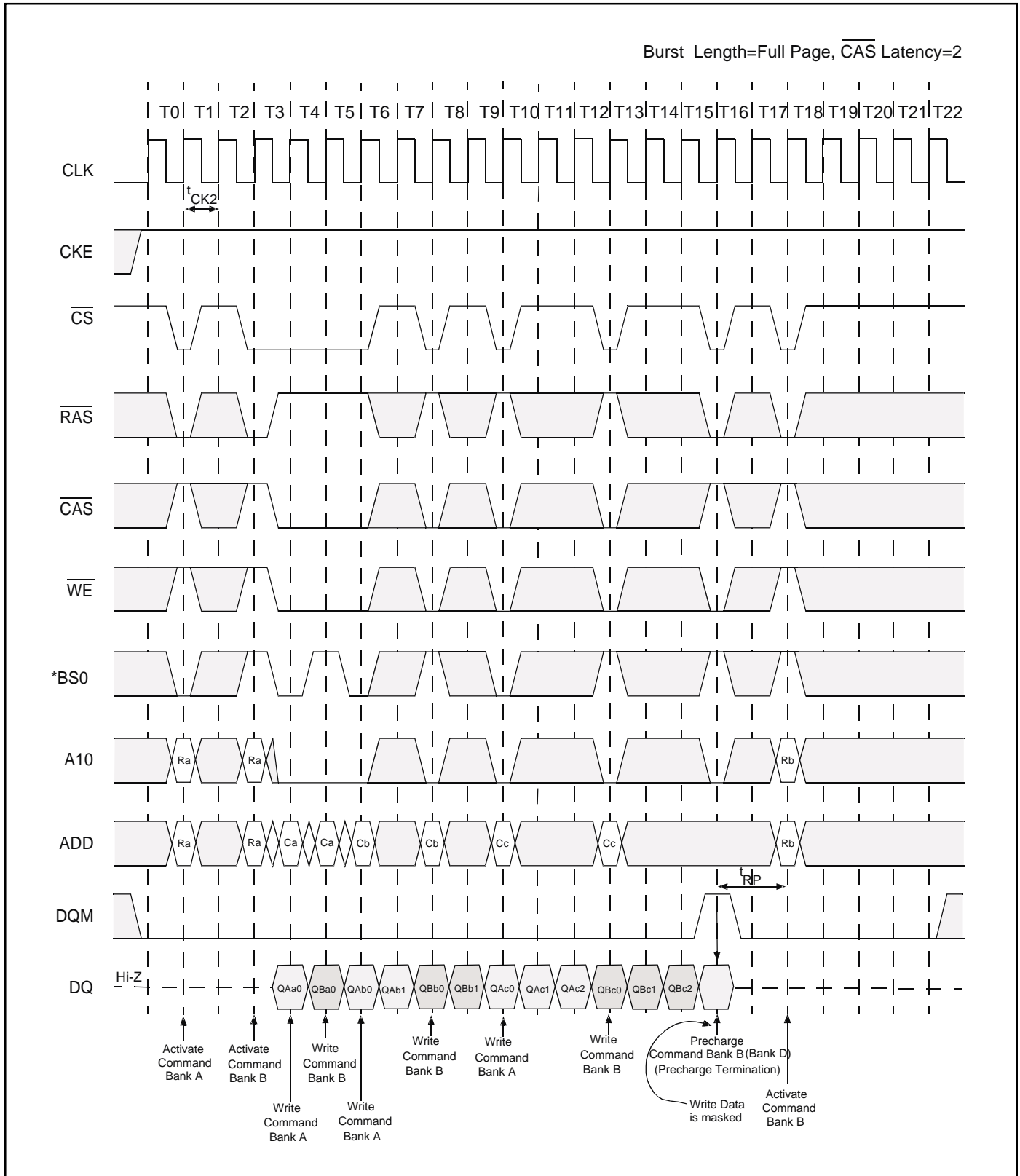
BS1="L", Bank C,D = Idle

Full Page Random Column Read



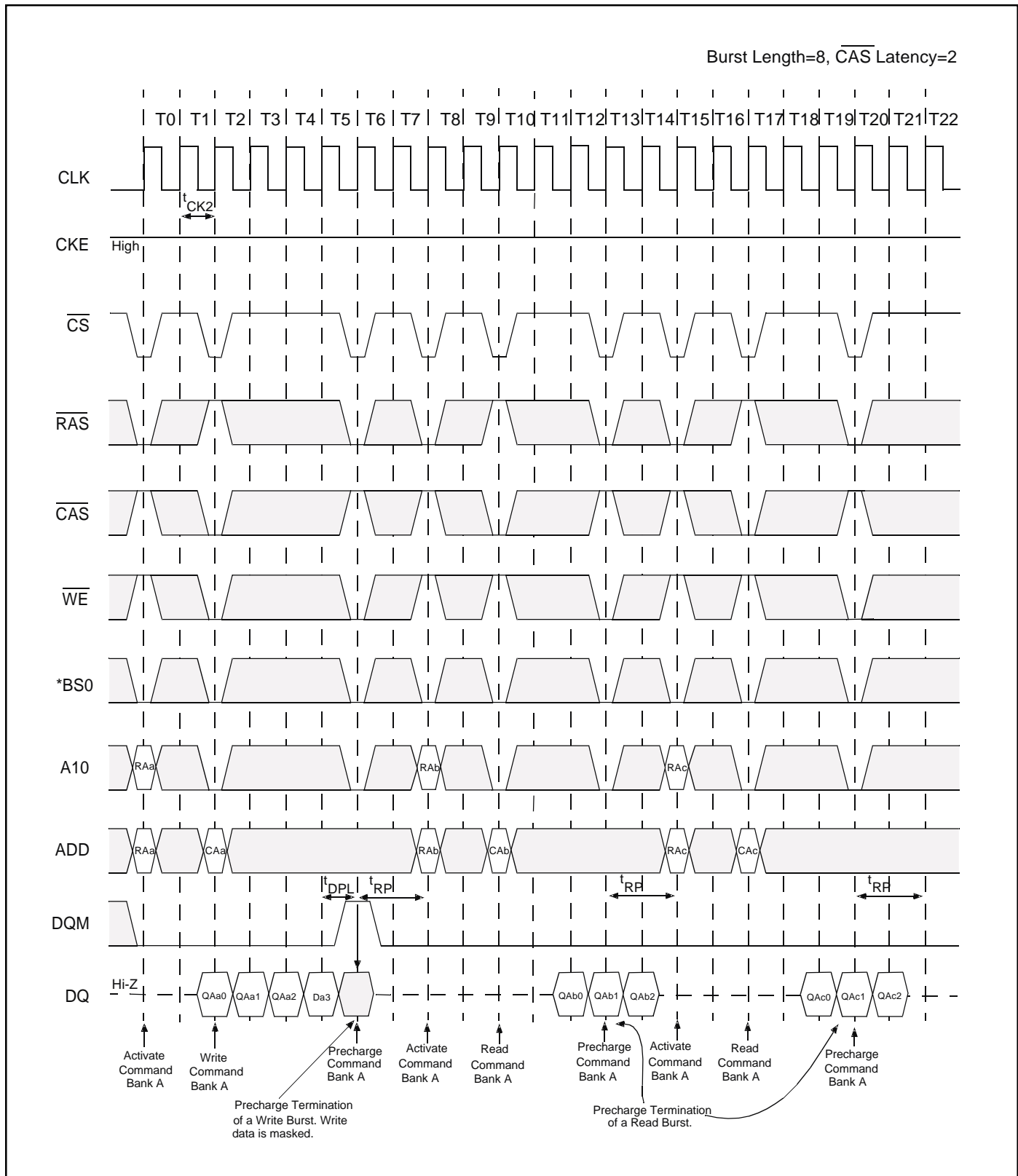
BS1="L", Bank C,D = Idle

Full Page Random Column Write



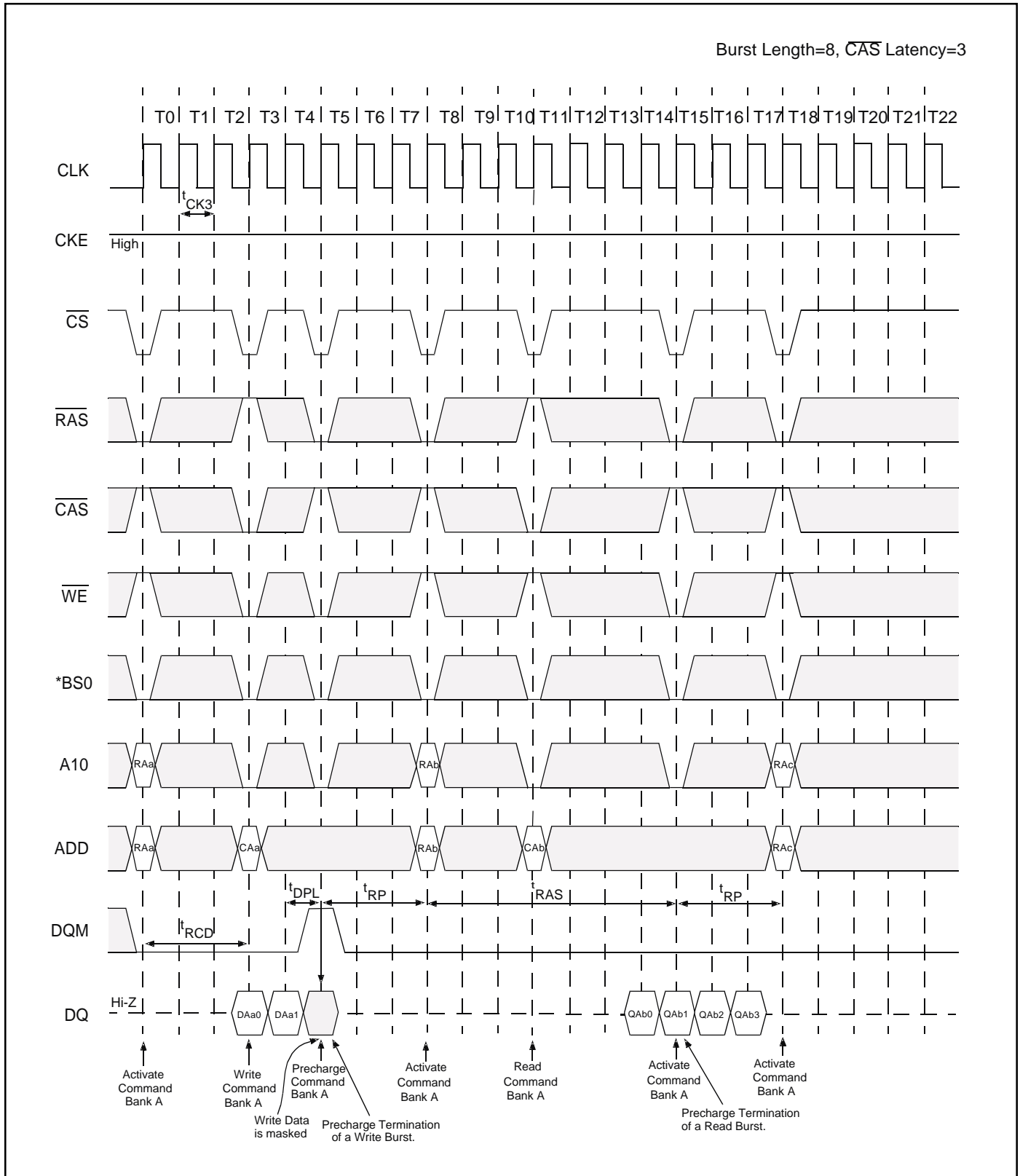
BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (1 of 2)



BS1="L", Bank C,D = Idle

Precharge Termination of a Burst (2 of 2)



BS1="L", Bank C,D = Idle

ORDERING INFORMATION

Commercial Range: 0°C to 70°C

| Speed (ns) | Order Part No. | Package |
|------------|----------------|---------------|
| 7 | IS42S8800-7T | 400mil TSOP-2 |
| | IS42S8800L-7T | 400mil TSOP-2 |
| 8 | IS42S8800-8T | 400mil TSOP-2 |
| | IS42S8800L-8T | 400mil TSOP-2 |
| 7 | IS42S16400-7T | 400mil TSOP-2 |
| | IS42S16400L-7T | 400mil TSOP-2 |
| 8 | IS42S16400-8T | 400mil TSOP-2 |
| | IS42S16400L-8T | 400mil TSOP-2 |

ORDERING INFORMATION

Industrial Temperature Range: -40°C to 85°C

| Speed (ns) | Order Part No. | Package |
|------------|-----------------|---------------|
| 7 | IS42S8800-7TI | 400mil TSOP-2 |
| | IS42S8800L-7TI | 400mil TSOP-2 |
| 8 | IS42S8800-8TI | 400mil TSOP-2 |
| | IS42S8800L-8TI | 400mil TSOP-2 |
| 7 | IS42S16400-7TI | 400mil TSOP-2 |
| | IS42S16400L-7TI | 400mil TSOP-2 |
| 8 | IS42S16400-8TI | 400mil TSOP-2 |
| | IS42S16400L-8TI | 400mil TSOP-2 |



Integrated Circuit Solution Inc.

HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.

TEL: 886-3-5780333

Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.

TEL: 886-2-26962140

FAX: 886-2-26962252

<http://www.icsi.com.tw>