# UTC MC14511                    CMOS IC

## BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

## DESCRIPTION

The UTC MC14511 BCD–to–seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light-emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

## FEATURES
* Low Logic Circuit Power Dissipation
* High–Current Sourcing Outputs (Up to 25 mA)
* Latch Storage of Code
* Blanking Input
* Lamp Test Provision
* Readout Blanking on all Illegal Input Combinations
* Lamp Intensity Modulation Capability
* Time Share (Multiplexing) Facility
* Supply Voltage Range = 3.0 V ~ 18 V
* Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
* Chip Complexity: 216 FETs or 54 Equivalent Gates
* Triple Diode Protection on all Inputs



SOP-16

DIP-16

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## PIN CONFIGURATION

```
        B  [ 1 ●        16 ]  VDD
        C  [ 2          15 ]  f
       LT  [ 3          14 ]  g
       BI  [ 4          13 ]  a
       LE  [ 5          12 ]  b
        D  [ 6          11 ]  c
        A  [ 7          10 ]  d
       Vss [ 8           9 ]  e
```

```
       a
   f /  g  / b
   e /  d  / c
```

### DISPLAY

```
 0  1  2  3  4  5  6  7  8  9
```
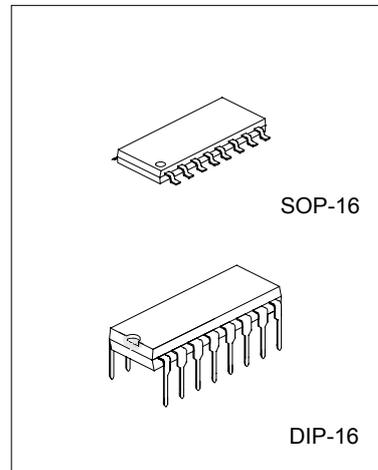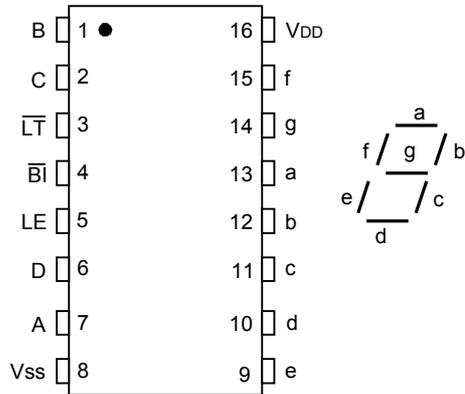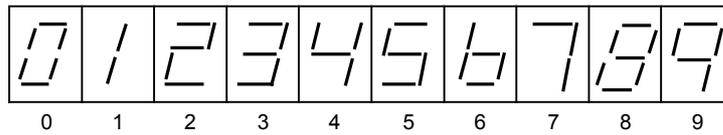
## TRUTH TABLE

| Inputs | | | | | | | Outputs | | | | | | | |
|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LE | BI | LT | D | C | B | A | a | b | c | d | e | f | g | Display |
| X | X | 0 | X | X | X | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| X | 0 | 1 | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 3 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 7 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 9 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Blank |
| 1 | 1 | 1 | X | X | X | X | * | | | | | | | * |

X=Don't Care

*Depends upon the BCD code previously applied when LE=0

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# UTC MC14511        CMOS IC

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if $V_{in}$ and $V_{out}$ are not constrained to the range:

       $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if $V_{DD}$ is applied, and the outputs are shorted to $V_{SS}$ and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$).

## BLOCK DIAGRAM



VDD=PIN 16
Vss=PIN 8

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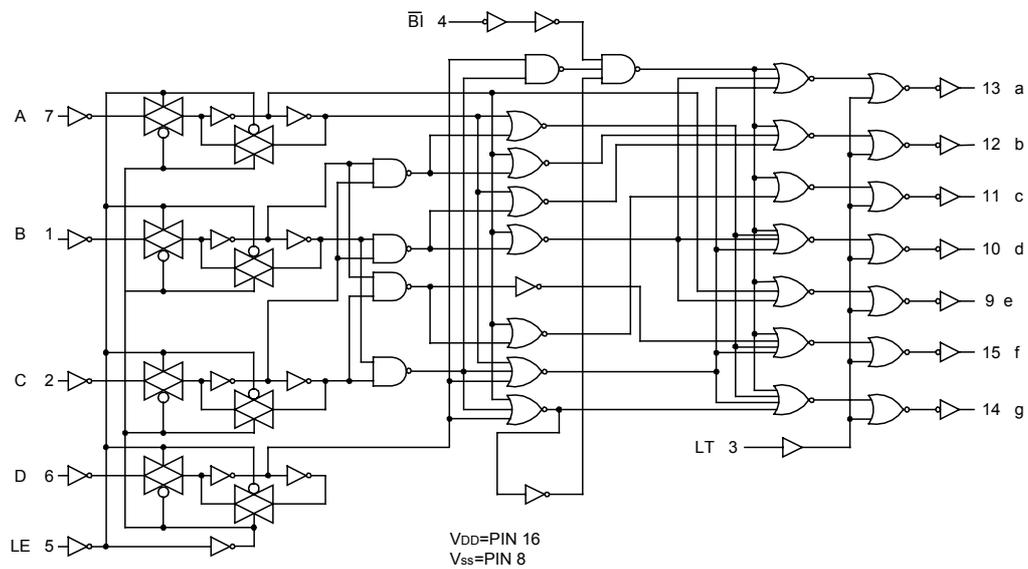
## ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to Vss) (Note 1)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| DC Supply Voltage Range | $V_{DD}$ | -0.5 ~ +18.0 | V |
| Input Voltage Range, All Inputs | Vin | -0.5 ~ $V_{DD}$+0.5 | V |
| DC Current Drain per Input Pin | I | 10 | mA |
| Power Dissipation, per Package (Note 2) | $P_D$ | 500 | mW |
| Maximum Output Drive Current (Source) per Output | $I_{OHmax}$ | 25 | mA |
| Maximum Continuous Output Power (Source) per Output (Note 3) | $P_{OHmax}$ | 50 | mA |
| Operating Temperature Range | $T_a$ | -55 ~ +125 | ℃ |
| Storage Temperature Range | Tstg | -65 ~ +150 | ℃ |

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Temperature Derating:
    Plastic "P and D/DW" Packages: - 7.0 mW/℃ From 65℃ ~ 125℃

Note 3: $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to Vss)

| PARAMETER | SYMBOL | VDD Vdc | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{OL}$ | 5.0 | "0" Level | | 0 | 0.05 | |
| | | 10 | Vin=$V_{DD}$ or 0 | | 0 | 0.05 | V |
| | | 15 | | | 0 | 0.05 | |
| | $V_{OH}$ | 5.0 | "1" Level | 4.1 | 4.57 | | |
| | | 10 | Vin=0 or $V_{DD}$ | 9.1 | 9.58 | | V |
| | | 15 | | 14.1 | 14.59 | | |
| Input Voltage # | $V_{IL}$ | 5.0 | "0" Level<br>Vo=3.8 or 0.5 V | | 2.25 | 1.5 | |
| | | 10 | Vo=8.8 or 1.0 V | | 4.50 | 3.0 | V |
| | | 15 | Vo=13.8 or 1.5V | | 6.75 | 4.0 | |
| | $V_{IH}$ | 5.0 | "1" Level<br>Vo=0.5 or 3.8 V | 3.5 | 2.75 | | |
| | | 10 | Vo=1.0 or 8.8 V | 7.0 | 5.50 | | V |
| | | 15 | Vo=1.5 or 13.8 V | 11 | 8.25 | | |
| Output Drive Voltage | $V_{OH}$ | 5.0 | $I_{OH}$=0mA    Source | 4.1 | 4.57 | | |
| | | | $I_{OH}$=5.0mA | | 4.24 | | |
| | | | $I_{OH}$=10mA | 3.9 | 4.12 | | V |
| | | | $I_{OH}$=15mA | | 3.94 | | |
| | | | $I_{OH}$=20mA | 3.4 | 3.70 | | |
| | | | $I_{OH}$=25mA | | 3.54 | | |
| | | 10 | $I_{OH}$=0mA    Source | 9.1 | 9.58 | | |
| | | | $I_{OH}$=5.0mA | | 9.26 | | |
| | | | $I_{OH}$=10mA | 9.0 | 9.17 | | V |
| | | | $I_{OH}$=15mA | | 9.04 | | |
| | | | $I_{OH}$=20mA | 8.6 | 8.90 | | |
| | | | $I_{OH}$=25mA | | 8.70 | | |

| PARAMETER | SYMBOL | $V_{DD}$ Vdc | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Drive Voltage | $V_{OH}$ | 15 | $I_{OH}$=0mA      Source<br>$I_{OH}$=5.0mA<br>$I_{OH}$=10mA<br>$I_{OH}$=15mA<br>$I_{OH}$=20mA<br>$I_{OH}$=25mA | 14.1<br><br>14<br><br>13.6 | 14.59<br>14.27<br>14.18<br>14.07<br>13.95<br>13.70 | | V |
| Output Drive Current | $I_{OL}$ | 5.0<br>10<br>15 | $V_{OL}$=0.4V      Sink<br>$V_{OL}$=0.5V<br>$V_{OL}$=1.5V | 0.51<br>1.3<br>3.4 | 0.88<br>2.25<br>8.8 | | mA |
| Input Current | $I_{in}$ | 15 | | | $\pm$0.00001 | $\pm$0.1 | $\mu$A |
| Input Capacitance | $C_{in}$ | | | | 5.0 | 7.5 | pF |
| Quiescent Current | $I_{DD}$ | 5.0<br>10<br>15 | (Per Package) Vin=0 or<br>$V_{DD}$,<br>Iout=0 $\mu$A | | 0.005<br>0.010<br>0.015 | 5.0<br>10<br>20 | $\mu$A |
| Total Supply Current (Notes 5 & 6) | $I_T$ | 5.0<br>10<br>15 | (Dynamic plus Quiescent, Per Package)<br>($C_L$=50pF on all outputs, all buffers switching) | $I_T$=(1.9 $\mu$A/kHz) f+$I_{DD}$<br>$I_T$=(3.8 $\mu$A/kHz) f+$I_{DD}$<br>$I_T$=(5.7 $\mu$A/kHz) f+$I_{DD}$ | | | $\mu$A |

Note 4: Noise immunity specified for worst–case input combination.

     Noise Margin for both "1" and "0" level =

        1.0 V min @ $V_{DD}$ = 5.0 V

        2.0 V min @ $V_{DD}$ = 10 V

        2.5 V min @ $V_{DD}$ = 15 V

Note 5: The formulas given are for the typical characteristics only at 25℃.

Note 6: To calculate total supply current at loads other than 50 pF:

     $I_T$ ($C_L$) = $I_T$(50 pF) + 3.5 x $10^{-3}$ ($C_L$ – 50) $V_{DD}$f

Where: $I_T$ is in $\mu$A (per package), $C_L$ in pF, $V_{DD}$ in Vdc, and f in kHz is input frequency.

## SWITCHING CHARACTERISTICS (Note 7) ($C_L$=50pF, $T_a$=25℃)

| PARAMETER | SYMBOL | $V_{DD}$ Vdc | TEST CONDITIONS | Min | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Rise Time | $t_{TLH}$ | 5.0 | $t_{TLH}$=(0.40 ns/pF) $C_L$+20 ns | | 40 | 80 | ns |
| | | 10 | $t_{TLH}$=(0.25 ns/pF) $C_L$+17.5 ns | | 30 | 60 | |
| | | 15 | $t_{TLH}$=(0.20 ns/pF) $C_L$+15 ns | | 25 | 50 | |
| Output Fall Time | $t_{THL}$ | 5.0 | $t_{THL}$=(1.5 ns/pF) $C_L$+50 ns | | 125 | 250 | ns |
| | | 10 | $t_{THL}$=(0.75 ns/pF) $C_L$+37.5 ns | | 75 | 150 | |
| | | 15 | $t_{THL}$=(0.55 ns/pF) $C_L$+37.5 ns | | 65 | 130 | |
| Data Propagation Delay Time | $t_{PLH}$ | 5.0 | $t_{PLH}$=(0.40 ns/pF) $C_L$+620 ns | | 640 | 1280 | ns |
| | | 10 | $t_{PLH}$=(0.25 ns/pF) $C_L$+237.5 ns | | 250 | 500 | |
| | | 15 | $t_{PLH}$=(0.20 ns/pF) $C_L$+165 ns | | 175 | 350 | |
| | $t_{PHL}$ | 5.0 | $t_{PHL}$=(1.3 ns/pF) $C_L$+655 ns | | 720 | 1440 | |
| | | 10 | $t_{PHL}$=(0.60 ns/pF) $C_L$+260 ns | | 290 | 580 | |
| | | 15 | $t_{PHL}$=(0.35 ns/pF) $C_L$+182.5 ns | | 200 | 400 | |
| Blank Propagation Delay Time | $t_{PLH}$ | 5.0 | $t_{PLH}$=(0.30 ns/pF) $C_L$+585 ns | | 600 | 750 | ns |
| | | 10 | $t_{PLH}$=(0.25 ns/pF) $C_L$+187.5 ns | | 200 | 300 | |
| | | 15 | $t_{PLH}$=(0.15 ns/pF) $C_L$+142.5 ns | | 150 | 220 | |
| | $t_{PHL}$ | 5.0 | $t_{PHL}$=(0.85 ns/pF) $C_L$+442.5 ns | | 485 | 970 | |
| | | 10 | $t_{PHL}$=(0.45 ns/pF) $C_L$+177.5 ns | | 200 | 400 | |
| | | 15 | $t_{PHL}$=(0.35 ns/pF) $C_L$+142.5 ns | | 160 | 320 | |
| Lamp Test Propagation Delay Time | $t_{PLH}$ | 5.0 | $t_{PLH}$=(0.45 ns/pF) $C_L$+290.5 ns | | 313 | 625 | ns |
| | | 10 | $t_{PLH}$=(0.25 ns/pF) $C_L$+112.5 ns | | 125 | 250 | |
| | | 15 | $t_{PLH}$=(0.20 ns/pF) $C_L$+80 ns | | 90 | 180 | |
| | $t_{PHL}$ | 5.0 | $t_{PHL}$=(1.3 ns/pF) $C_L$+248 ns | | 313 | 625 | |
| | | 10 | $t_{PHL}$=(0.45 ns/pF) $C_L$+102.5 ns | | 125 | 250 | |
| | | 15 | $t_{PHL}$=(0.35 ns/pF) $C_L$+72.5 ns | | 90 | 180 | |
| Setup Time | $t_{su}$ | 5.0 | | 100 | | | ns |
| | | 10 | | 40 | | | |
| | | 15 | | 30 | | | |
| Hold Time | $t_h$ | 5.0 | | 60 | | | ns |
| | | 10 | | 40 | | | |
| | | 15 | | 30 | | | |
| Latch Enable Pulse Width | $t_{WL}$ | 5.0 | | 520 | 260 | | ns |
| | | 10 | | 220 | 110 | | |
| | | 15 | | 130 | 65 | | |

Note 7: The formulas given are for the typical characteristics only.

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SWITCHING TIME WAVEFORMS
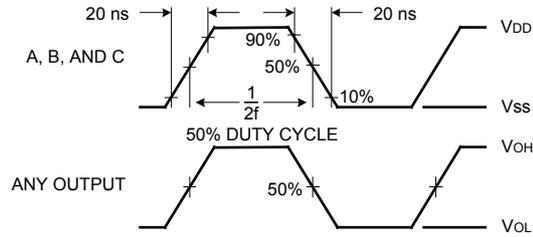
Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective $C_L$ loads.

Figure 1. Dynamic Power Dissipation Signal Waveforms
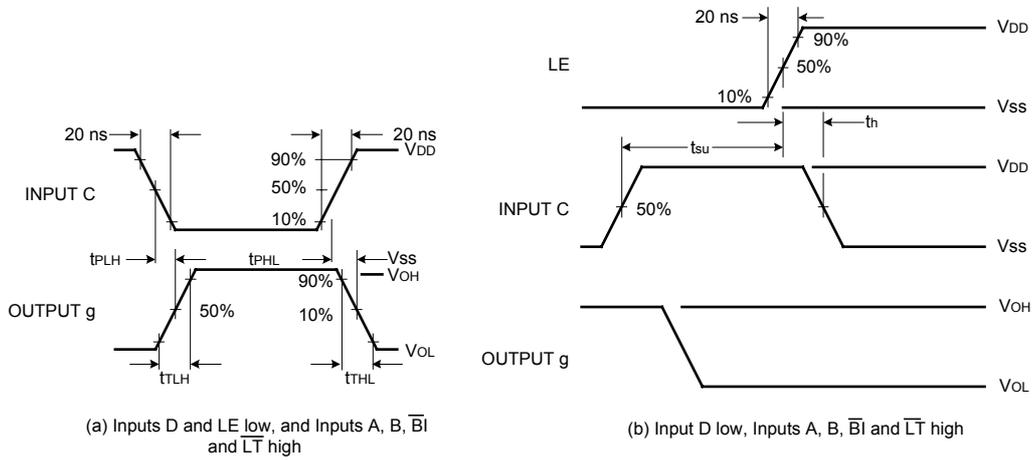
(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high

(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high

(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

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## CONNECTIONS TO VARIOUS DISPLAY READOUTS

### LIGHT EMITTING DIODE (LED) READOUT

$V_{DD}$

COMMON
CATHODE LED

$\approx 1.7V$

$V_{SS}$

$V_{DD}$

COMMON
ANODE LED

$\approx 1.7V$

$V_{SS}$
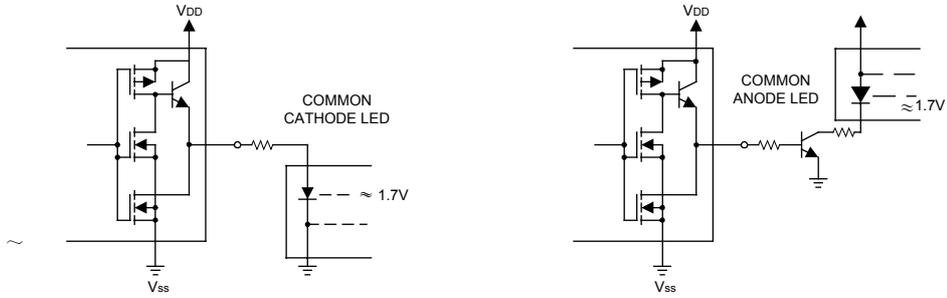
### INCANDESCENT READOUT

$V_{DD}$      $V_{DD}$

**

$V_{SS}$

### FLUORESCENT READOUT

$V_{DD}$

DIRECT
(LOW BRIGHTNESS)

FILAMENT
SUPPLY

$V_{SS}$

Vss OR APPROPRIATE
VOLTAGE BELOW Vss.

(CAUTION: Maximum working voltage=18.0V)

### GAS DISCHARGE READOUT

APPROPRIATE
VOLTAGE

$V_{DD}$

$V_{SS}$
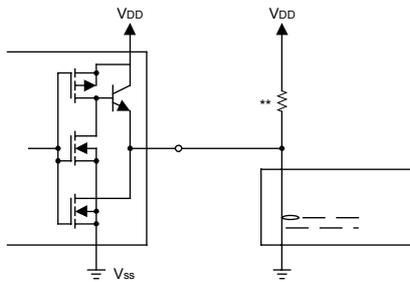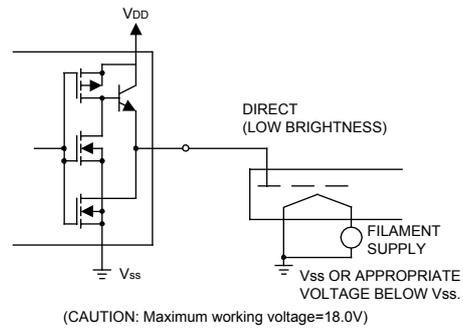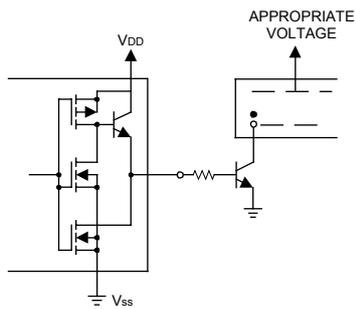
### LIQUID CRYSTAL(LCD) READOUT

EXCITATION
(SQUARE WAVE, Vss TO V$_{DD}$)

$V_{DD}$

1/4 OF MC14070B

$V_{SS}$
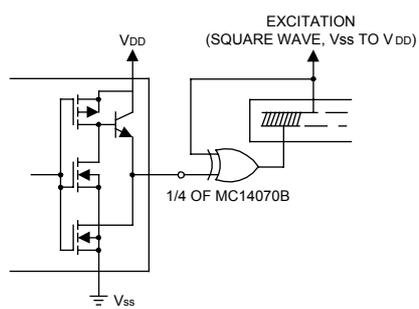
** A filament pre-warm resistor is recommended to reduce filament
thermal shock and increase the effective cold resistance of the
filament.

Direct dc drive of LCD's not recommended for life of
LCD readouts.

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QW-R502-021,B