



2x512Kx8 DUALITHIC™ SRAM

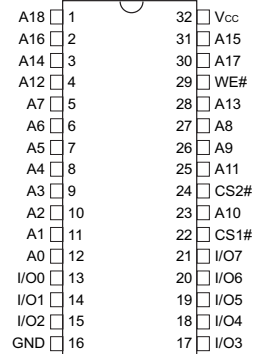
FEATURES

- Access Times 17, 20, 25, 35, 45, 55ns
- Evolutionary, Corner Power/Ground Pinout
- Packaging:
 - 32 pin, Hermetic Ceramic DIP (Package 300)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 3.3V Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Output Enable Internally tied to GND.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

PIN CONFIGURATION FOR WS1M8V-XCX

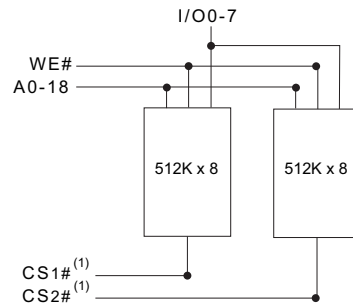
32 DIP TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS#1-2	Chip Selects
WE#	Write Enable
Vcc	+3.3V Power Supply
GND	Ground

BLOCK DIAGRAM



NOTE:

1. CS#₁ and CS#₂ are used to select the lower and upper 512Kx8 of the device. CS#₁ and CS#₂ must not be enabled at the same time.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	+4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	5.5	V

TRUTH TABLE

CS#	WE#	Mode	Data I/O	Power
H	X	Standby	High Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE: OE# is internally tied to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C

CAPACITANCE

T_A = +25°C

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1.0MHz	28	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1.0MHz	28	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{CC} = 3.6, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO} ¹	CS# = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current	I _{CC} ¹	CS# = V _{IL} , f = 5MHz, V _{CC} = 3.6		160	mA
Standby Current	I _{SB} ¹	CS# = V _{IH} , f = 5MHz, V _{CC} = 3.6		30	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE:

DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

1. OE# is internally tied to GND.



AC CHARACTERISTICS

$V_{CC} = 3.3V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		45		55		ns
Address Access Time	t_{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		17		20		25		35		45		55	ns
Chip Select to Output in Low Z	t_{CLZ}^1	2		2		2		4		4		4		ns
Chip Disable to Output in High Z	t_{CHZ}^1		9		10		12		15		20		20	ns

NOTES:

1. This parameter is guaranteed by design but not tested.
2. OE# is internally tied to GND.

AC CHARACTERISTICS

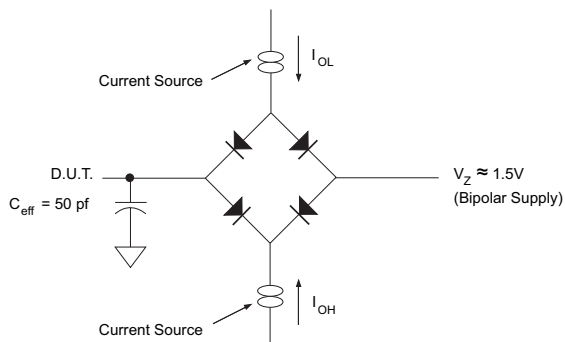
$V_{CC} = 3.3V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	14		14		15		25		35		50		ns
Address Valid to End of Write	t_{AW}	14		14		15		25		35		50		ns
Data Valid to End of Write	t_{DW}	9		10		10		20		25		25		ns
Write Pulse Width	t_{WP}	14		14		15		25		35		40		ns
Address Setup Time	t_{AS}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		5		5		ns
Output Active from End of Write	t_{OW}^1	2		3		4		4		5		5		ns
Write Enable to Output in High Z	t_{WHZ}^1		9		9		10		15		15		25	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		ns

NOTES:

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

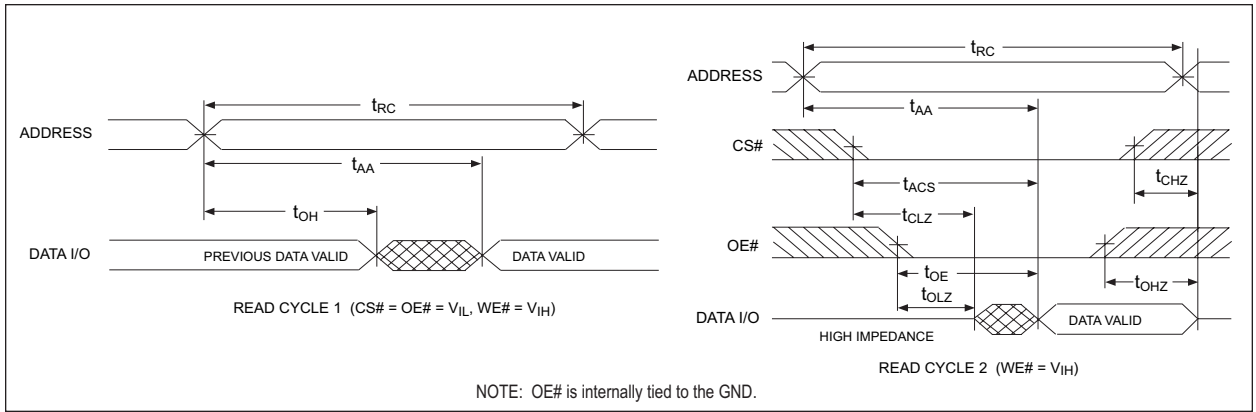
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

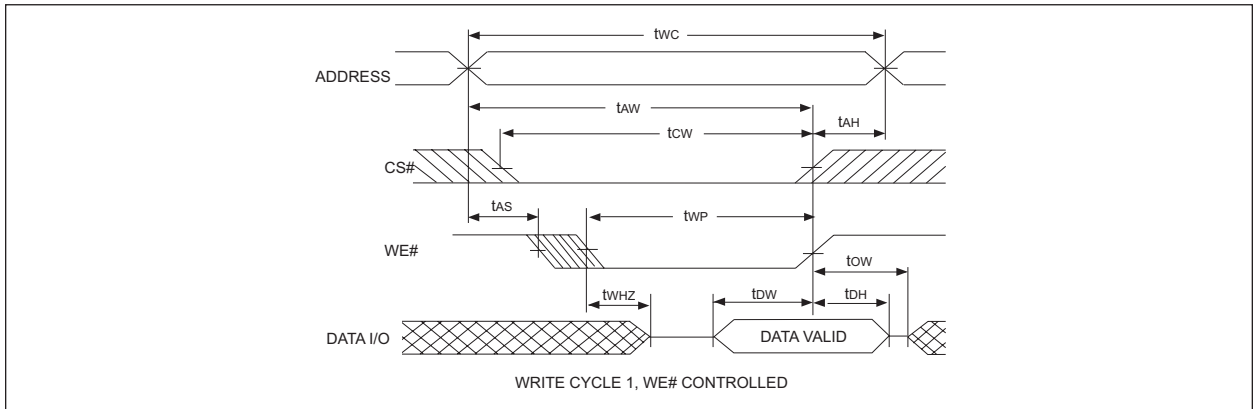
V_z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance $Z_0 = 75 \Omega$.
 V_z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



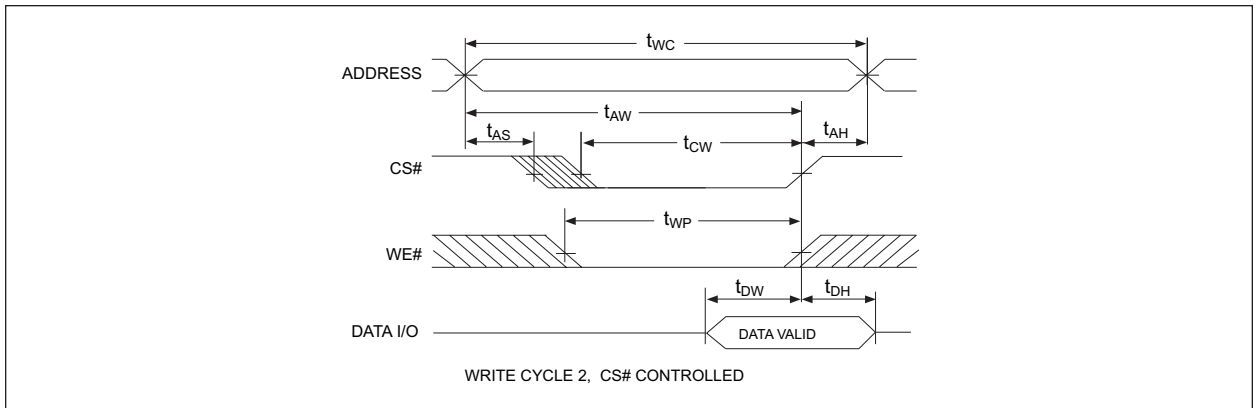
TIMING WAVEFORM – READ CYCLE



WRITE CYCLE – WE# CONTROLLED

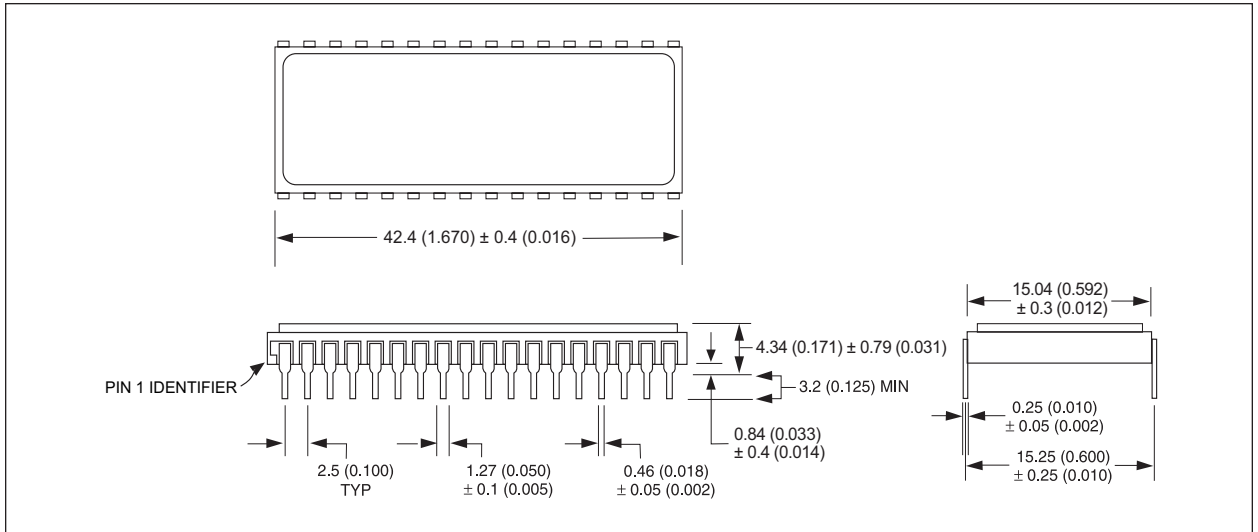


WRITE CYCLE – CS# CONTROLLED





PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 1M8 V - XXX C X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = 32 pin Ceramic 0.600" DIP (Package 300)

ACCESS TIME (ns)

LOW VOLTAGE SUPPLY 3.3V ±10%

ORGANIZATION, two banks of 512K x 8

SRAM

WHITE ELECTRONIC DESIGNS CORP.