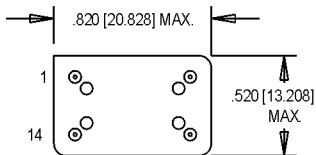
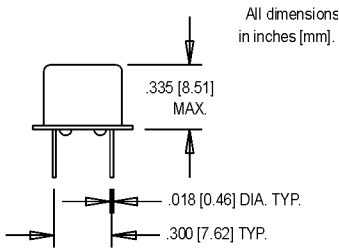
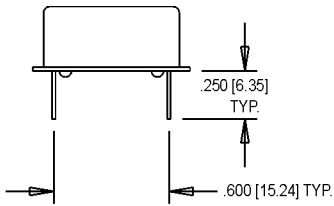


# K1528D Series

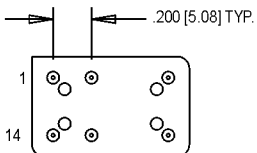
14 pin DIP, 5.0 Volt, CMOS, VCXO



- Former **Champion** product
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



OPTIONAL 6-PIN PACKAGE WITH TRISTATE



### Pin Connections

PIN	FUNCTION
1	Voltage Control
7	Ground/Case Ground
8	Output
14	+Vdd

### Ordering Information

Product Series	K1528D	X	X	X	X	-R	00.0000 MHz
Model Selection							
B:	±100 - ±150 ppm Pull						
D:	±60 - ±110 ppm Pull						
Symmetry/Logic Compatibility							
Blank:	CMOS 40%/60%						
S:	CMOS 45%/55%						
Temperature Range							
Blank:	0°C to +70°C						
M:	-40°C to +85°C						
Tri-State Option							
Blank:	No Tristate						
E:	Tristate Option						
RoHS Compliance							
Blank:	non-RoHS compliant part						
-R:	RoHS compliant part						
Frequency (customer specified)							

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Electrical Specifications	Frequency Range	F	35		85	MHz		
	Operating Temperature	T <sub>A</sub>	(See ordering information)					
	Storage Temperature	T <sub>S</sub>	-40		+125	°C		
	Frequency Stability Overall	ΔF/F	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
	0°C to 70°C				±25	ppm		
	-40°C to +85°C				±50	ppm		
	Aging 1 <sup>st</sup> Year		-5		+5	ppm		
	Thereafter (per year)		-2		+2	ppm		
	Pullability/APR		(See ordering information)					
	Control Voltage	V <sub>c</sub>	0.5	2.5	4.5	V		
	Linearity				15	%	Positive Monotonic Slope	
	Modulation Bandwidth	f <sub>m</sub>	20			kHz	±3dB	
	Input Impedance	Z <sub>in</sub>	50k			Ohms	@ 10 kHz	
	Input Voltage	V <sub>dd</sub>	4.75	5.0	5.25	V		
	Input Current	I <sub>dd</sub>			40	mA		
Output Type						HCMOS/TTL		
Load		5 TTL or 15 pF HCMOS					See Note 1	
Symmetry (Duty Cycle)		(See ordering information)						
Logic "1" Level	V <sub>oh</sub>	4.5			V			
Logic "0" Level	V <sub>ol</sub>			0.5	V			
Output Current				±16	mA			
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>			4	ns			
Start Up Time				10	ms			
Phase Jitter @ 40 MHz	Ö <sub>J</sub>		2		ps RMS	Integrated 12 kHz – 20 MHz		
Phase Noise (Typical) @40 MHz		10 Hz	100 Hz	1 kHz	10 kHz	Offset from Carrier		
		-65	-95	-115	-140	dBc/Hz		
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 mS duration, ½ sinewave)						
	Vibration	Per MIL-STD-202, Method 201 & 204 (10 g's from 10-2000 Hz)						
	Hermeticity	Per MIL-STD-202, Method 112, (1x10 <sup>-8</sup> atm. cc/s of Helium)						
	Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55°C to +125°C, 15 min. dwell, 10 cycles)						
	Solderability	Per EIAJ-STD-002						
Soldering Conditions	+240°C max. for 10 secs.							

1. TTL load - see load circuit diagrams #1 and #2
2. Symmetry is measured at 1.4 V with TTL load, and at 50% V<sub>dd</sub> with HCMOS load.

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