M5M44400BJ,L,TP,RT-5,-6,-7,-8,-5S,-6S,-7S,-8S

FAST PAGE MODE 4194304-BIT(1048576-WORD BY 4-BIT)DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMS, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of quadruple-layer polysilicon process combined with silicide technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs.

Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

Self or extended refresh current is small enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max. ns)	$\overline{CAS}$ access time (max. ns)	Address access (max. ns)
M5M44400BXX-5,-5S	50	13	25
M5M44400BXX-6,-6S	60	15	30
M5M44400BXX-7,-7S	70	20	35
M5M44400BXX-8,-8S	80	20	40

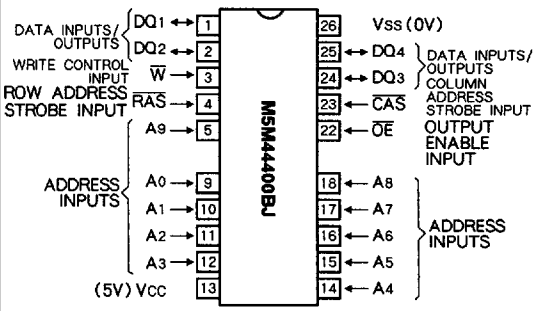
Type name	$\overline{OE}$ access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
M5M44400BXX-5,-5S	13	90	500
M5M44400BXX-6,-6S	15	110	400
M5M44400BXX-7,-7S	20	130	350
M5M44400BXX-8,-8S	20	150	300

XX = J, L, TP, RT

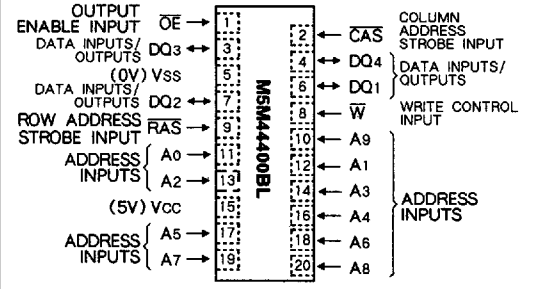
- Standard 26pin SOJ, 20pin ZIP, 26pin TSOP (II)
- Single 5V ± 10% supply
- Low stand-by power dissipation
  - CMOS Input level ..... 5.5mW (max)
  - CMOS Input level ..... 0.55mW (max)*
- Low operating power dissipation
  - M5M44400BXX-5,-5S ..... 687.5mW (max)
  - M5M44400BXX-6,-6S ..... 550.0mW (max)
  - M5M44400BXX-7,-7S ..... 467.5mW (max)
  - M5M44400BXX-8,-8S ..... 412.5mW (max)
- Self refresh capability*
  - Self refresh current ..... 150 μA (max)
- Extended refresh capability
  - Extended refresh current ..... 150 μA (max)
- Fast-page mode (1024-bit random access), Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, CBR Self Refresh (-5S, -6S, -7S, -8S) capabilities.
- Early write mode and $\overline{OE}$ to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
- 1024 refresh cycles every 128ms (A_0~A_9)*
- 4-bit parallel test mode capability

* : Applicable to self refresh version (M5M44400BJ, L, TP, RT-5S,-6S, -7S, -8S : option) only.

PIN CONFIGURATION (TIO WIVEW)



Outline 26P0J (300mil SOJ)



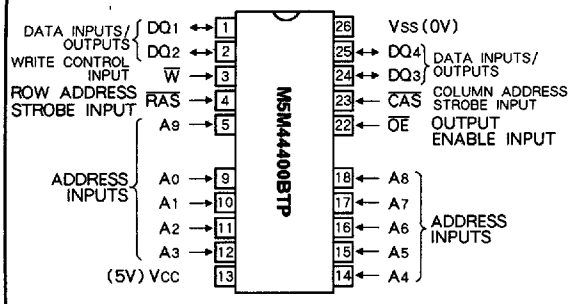
Outline 20P5L-B (ZIP)

APPLICATION

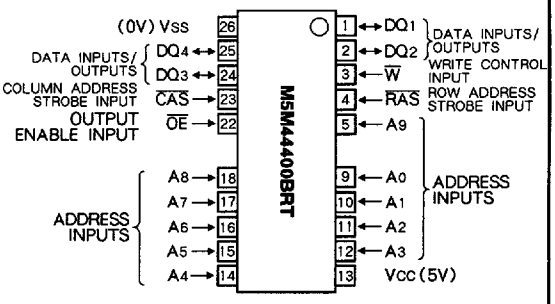
Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

M5M44400BJ, L, TP, RT-5,-5S : Under development

PIN CONFIGURATION (TOP VIEW)



Outline 26P3Z-E(TSOP)



Outline 26P3Z-F(TSOP)

FUNCTION

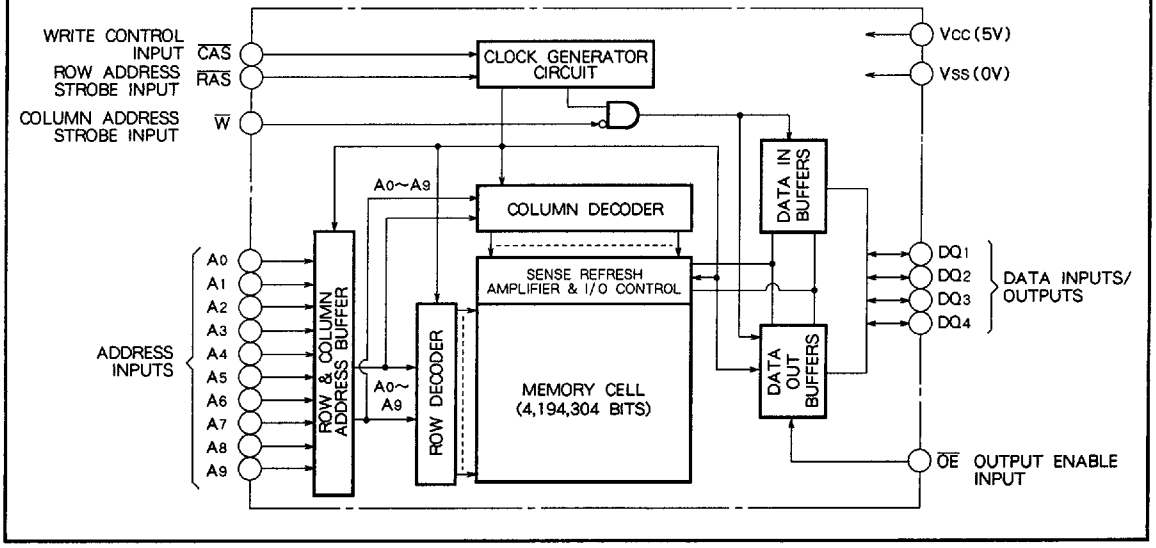
The M5M44400BJ, L, TP, RT provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1. Input condition for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input D	Output Q		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	Fast page mode identical
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh (Extended*)	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self Refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−1~7	V
V_I	Input voltage		−1~7	V
V_O	Output voltage		−1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta = 25℃	1000	mW
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low-level input voltage	DQ_1~DQ_4	−1.0		0.8	V
		Others	−2.0		0.8	

Note 1. All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH} = −5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL} = 4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V ≦ V_{OUT} ≦ 5.5V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦6.5V, 0ther inputs pins=0V	−10		10	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3, 4, 5)	M5M44400B-5, -5S	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{WC} = min., output open			125	mA
		M5M44400B-6, -6S				100	
		M5M44400B-7, -7S				85	
		M5M44400B-8, -8S				75	
$I_{CC2(AV)}$	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open			2	mA
		M5M44400B	$\overline{RAS}$ = $\overline{CAS}$ ≧ Vcc − 0.5, output open			1	
		M5M44400B(S)				0.1	
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 3, 5)	M5M44400B-5, -5S	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min., output open			125	mA
		M5M44400B-6, -6S				100	
		M5M44400B-7, -7S				85	
		M5M44400B-8, -8S				75	
$I_{CC4(AV)}$	Average supply current from Vcc, Fast-Page-Mode (Note 3, 4, 5)	M5M44400B-5, -5S	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{RC} = min, output open			125	mA
		M5M44400B-6, -6S				100	
		M5M44400B-7, -7S				85	
		M5M44400B-8, -8S				75	
$I_{CC6(AV)}$	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400B-5, -5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{PC} = min., output open			105	mA
		M5M44400B-6, -6S				85	
		M5M44400B-7, -7S				75	
		M5M44400B-8, -8S				65	
$I_{CC8(AV)}$	Average supply current from Vcc Extended-Refresh cycle (Note 6)		Stand-by: $\overline{RAS}$ ≧ Vcc − 0.2V, $\overline{CAS}$ ≧ Vcc − 0.2V or $\overline{CAS}$ ≦ 0.2V; $\overline{CAS}$ before $\overline{RAS}$ refresh: $\overline{RAS}$ cycling $\overline{CAS}$ ≦ 0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling, W ≦ 0.2V or ≧ Vcc − 0.2V, $\overline{OE}$ ≦ 0.2V or ≧ Vcc − 0.2V, A0~A9 ≦ 0.2V or ≧ Vcc − 0.2V, DQ = open, t_{RC} = 125 μs, t_{RAS} = t_{RAS} min~1 μs			150	μA
$I_{CC9(AV)}$	Average supply current from Vcc Self-Refresh cycle (Note 6)	M5M44400B(S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			150	μA

Note 2. Current flowing into an IC is positive. out is negative.
3. $I_{CC1(AV)}$, $I_{CC3(AV)}$ and $I_{CC4(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.
5. Column Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M44400BJ, TP, RT	V_I = Vss f = 1MHz V_i = 25mVrms			5	pF
		M5M44400BL				6	
$C_{I(CLK)}$	Input capacitance, clock inputs	M5M44400BJ, TP, RT				7	pF
		M5M44400BL				7	
$C_{I/O}$	Input/Output capacitance, data ports	M5M44400BJ, TP, RT				7	pF
		M5M44400BL				7	

SWITCHING CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter		Limits								Unit
			M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7, 8)		13		15		20		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7, 9)		50		60		70		80	ns
t_{AA}	Column Address access time	(Note 7, 10)		25		30		35		40	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		30		35		40		45	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20		20	ns
t_{CLZ}	Output low impedance from $\overline{CAS}$ low	(Note 7)	5		5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)	0	13	0	15	0	20	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)	0	13	0	15	0	20	0	20	ns

Note 6. An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7. Measured with a load circuit equivalent to 2TTL loads and 100pF.
8. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{ASC} \geq t_{ASC}$(max).
9. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RAD} exceeds the value shown.
10. Assumes that $t_{RAD} \geq t_{RAD}$(max) and $t_{ASC} \leq t_{ASC}$(max).
11. Assumes that $t_{CP} \leq t_{CP}$(max) and $t_{ASC} \geq t_{ASC}$(max).
12. t_{OFF}(max) and t_{OEZ}(max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10\,\mu A |$) and is not reference to V_{OH}(min) or V_{OL}(max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast Page Cycles)

(T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Symbol	Parameter		Limits								Unit
			M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time	M5M44400B		16.4		16.4		16.4		16.4	ms
		M5M44400B(S)		128		128		128		128	
t_{RP}	$\overline{RAS}$ high pulse width		30		40		50		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note 15)		18	37	20	45	20	50	20	60	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		5		ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note 16)		13	25	15	30	15	35	15	40	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note 17)		0	10	0	10	0	10	0	15	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		8		10		10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low		13		15		15		15		ns
t_{DZC}	Delay time, data to $\overline{CAS}$ low (Note 18)		0		0		0		0		ns
t_{DZO}	Delay time, data to $\overline{OE}$ low (Note 18)		0		0		0		0		ns
t_{CDD}	Delay time, $\overline{CAS}$ high to data (Note 19)		13		15		20		20		ns
t_{ODD}	Delay time, $\overline{OE}$ high to data (Note 19)		13		15		20		20		ns
t_T	Transition time (Note 20)		1	50	1	50	1	50	1	50	ns

Note 13. The timing requirements are assumed t_T = 5ns.
14. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals.
15. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is less than t_{RCD}(max), access time is t_{RAC}.
If t_{RCD} is greater than t_{RCD}(max), access time is controlled exclusively by t_{CAC} or t_{AA}.
t_{RCD}(min) is specified as t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min).
16. t_{RAD}(max) is specified as a reference point only. If $t_{RAD} \geqq t_{RAD}$(max) and $t_{ASC} \leqq t_{ASC}$(max), access time is controlled exclusively by t_{AA}.
17. t_{ASC}(max) is specified as a reference point only. If $t_{RCD} \geqq t_{RCD}$(max) and $t_{ASC} \geqq t_{ASC}$(max), access time is controlled exclusively by t_{CAC}.
18. Either t_{DZC} or t_{DZO} must be satisfied.
19. Either t_{CDD} or t_{ODD} must be satisfied.
20. t_T is measured between V_{IH}(min) and V_{IL}(max).

Read and Refresh Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7-7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	90		110		130		150		ns
t_{RAS}	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	80	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		80		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		20		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (Note 21)	0		0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (Note 21)	10		10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	25		30		35		40		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	13		15		20		20		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	13		15		20		20		ns

Note 21. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write Cycles)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7-7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	90		110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width	50	10000	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	13	10000	15	10000	20	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	50		60		70		80		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	13		15		20		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 23)	0		0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	8		10		15		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		20		ns
tWP	Write pulse width	8		10		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	8		10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		20		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWC	Read Write/read modify write cycle time (Note 22)	126		150		175		195		ns
tRAS	$\overline{RAS}$ low pulse width	86	10000	95	10000	115	10000	125	10000	ns
tCAS	$\overline{CAS}$ low pulse width	49	10000	50	10000	65	10000	65	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	86		95		115		125		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	49		50		65		65		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	35		35		40		40		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	73		80		90		100		ns
tAWD	Delay time, address to $\overline{W}$ low (Note 23)	48		50		55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	13		15		20		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	13		15		20		20		ns
tWP	Write pulse width	8		10		15		15		ns
tDS	Data setup time before $\overline{W}$ low	0		0		0		0		ns
tDH	Data hold time after $\overline{W}$ low	8		10		15		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low	13		15		15		20		ns

Note 22. tRWC is specified as tRWC(min) = tRAC(max) + tODD(min) + tRWL(min) + tRP(min) + 4tT.

23. tWCS, tCWD, tRWD and tAWD and tCPWD are specified as reference points only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD ≥ tCWD(min), tRWD ≥ tRWD(min), tAWD ≥ tAWD(min), and tCPWD ≥ tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed-write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	35		40		45		50		ns
tPRWC	Fast Page mode read write/read modify write cycle time	71		75		95		100		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note 25)	85	100000	100	100000	115	100000	135	100000	ns
tCP	$\overline{CAS}$ high pulse width (Note 26)	8	12	10	15	10	15	10	20	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	30		35		40		45		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	30		35		40		45		ns

Note 24. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

25. tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

26. tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, Extended Refresh*Cycle (Note 27)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		5		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		15		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		15		ns
t_{CAS}	$\overline{CAS}$ low pulse width	25		25		30		30		ns

Note 27. Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle*

Symbol	Parameter	Limits								Unit
		M5M44400B-5S		M5M44400B-6S		M5M44400B-7S		M5M44400B-8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RASS}	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		100		μs
t_{RPS}	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		150		ns
t_{CHS}	CBR self refresh $\overline{CAS}$ hold time	−50		−50		−50		−50		ns
t_{RSR}	Read setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{RHR}	Read hold time after $\overline{RAS}$ low	10		10		15		15		ns

Test Mode Specification (Note 28)

ELECTRICAL CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4, 5)	M5M44400B-5, -5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min. output open			145	mA
		M5M44400B-6, -6S				115	
		M5M44400B-7, -7S				100	
		M5M44400B-8, -8S				85	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3, 5)	M5M44400B-5, -5S	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}, t_{RC} = min. output open			145	mA
		M5M44400B-6, -6S				115	
		M5M44400B-7, -7S				100	
		M5M44400B-8, -8S				85	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast-Page-Mode (Note 3, 4, 5)	M5M44400B-5, -5S	$\overline{RAS}$ = V_{IL} $\overline{CAS}$ cycling t_{PC} = min., output open			145	mA
		M5M44400B-6, -6S				115	
		M5M44400B-7, -7S				100	
		M5M44400B-8, -8S				85	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M44400B-5, -5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling, t_{RC} = min. output open			120	mA
		M5M44400B-6, -6S				100	
		M5M44400B-7, -7S				85	
		M5M44400B-8, -8S				75	

Note 28. All previously specified electrical characteristics, switching characteristics and timing requirements are applicable to that of test mode.

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 6, 13, 14)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7, 8)		18		20		25		25	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7, 9)		55		65		75		85	ns
t_{AA}	Column Address access time (Note 7, 10)		30		35		40		45	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge (Note 7, 11)		35		40		45		50	ns
t_{OEA}	Access time from $\overline{OE}$ (Note 7)		18		20		25		25	ns

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Notes 13, 14)

Read and Refresh Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	95		115		135		155		ns
t_{RAS}	$\overline{RAS}$ low pulse width	55	10000	65	10000	75	10000	85	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	18	10000	20	10000	25	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	55		65		75		85		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	18		20		25		25		ns
t_{RAL}	Column address to $\overline{RAS}$ hold time	30		35		40		45		ns
t_{OCH}	$\overline{CAS}$ hold time after $\overline{OE}$ low	18		20		25		25		ns
t_{ORH}	$\overline{RAS}$ hold time after $\overline{OE}$ low	18		20		25		25		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RWC}	Read Write/read modify write cycle time (Note 22)	131		155		180		200		ns
t_{RAS}	$\overline{RAS}$ low pulse width	91	10000	100	10000	120	10000	130	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	54	10000	55	10000	70	10000	70	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	91		100		120		130		ns
t_{RSH}	$\overline{RAS}$ hold time $\overline{CAS}$ low	54		55		70		70		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note 23)	40		40		45		45		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note 23)	78		85		95		105		ns
t_{AWD}	Delay time, address to $\overline{W}$ low (Note 23)	53		55		60		65		ns

Fast-Page Mode Cycle (Read, Write, Read-Write, and Read-Modify-Write Cycles) (Note 24)

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode read/write cycle time	40		45		50		55		ns
t_{PRWC}	Fast page mode read write/read modify write cycle time	76		80		100		105		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle	90	100000	110	100000	125	100000	145	100000	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		45		50		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note 23)	35		40		45		50		ns

Test Mode Set Cycle

Symbol	Parameter	Limits								Unit
		M5M44400B-5, -5S		M5M44400B-6, -6S		M5M44400B-7, -7S		M5M44400B-8, -8S		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WSR}	Write setup time before $\overline{RAS}$ low	10		10		10		10		ns
t_{WHR}	Write hold time after $\overline{RAS}$ low	10		10		15		15		ns

Note 29. Self refresh sequence

Two refreshing ways shoud be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$

1.1 Distriduted refresh during Read/Write operation

(A) Timing Diagrams

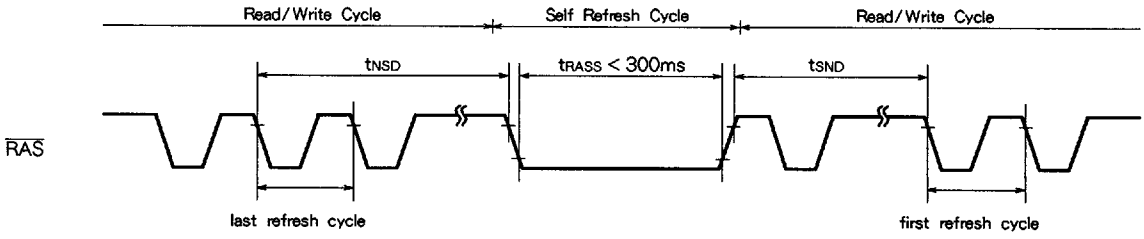


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of nine row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

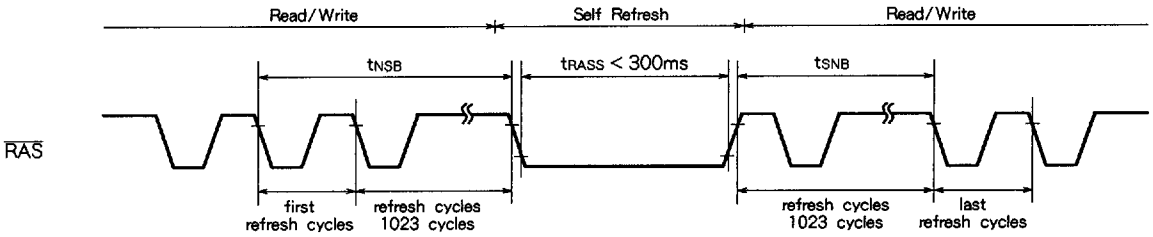


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

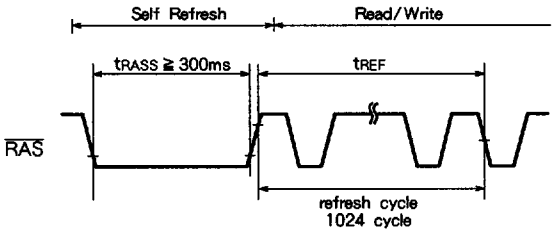


Table 4

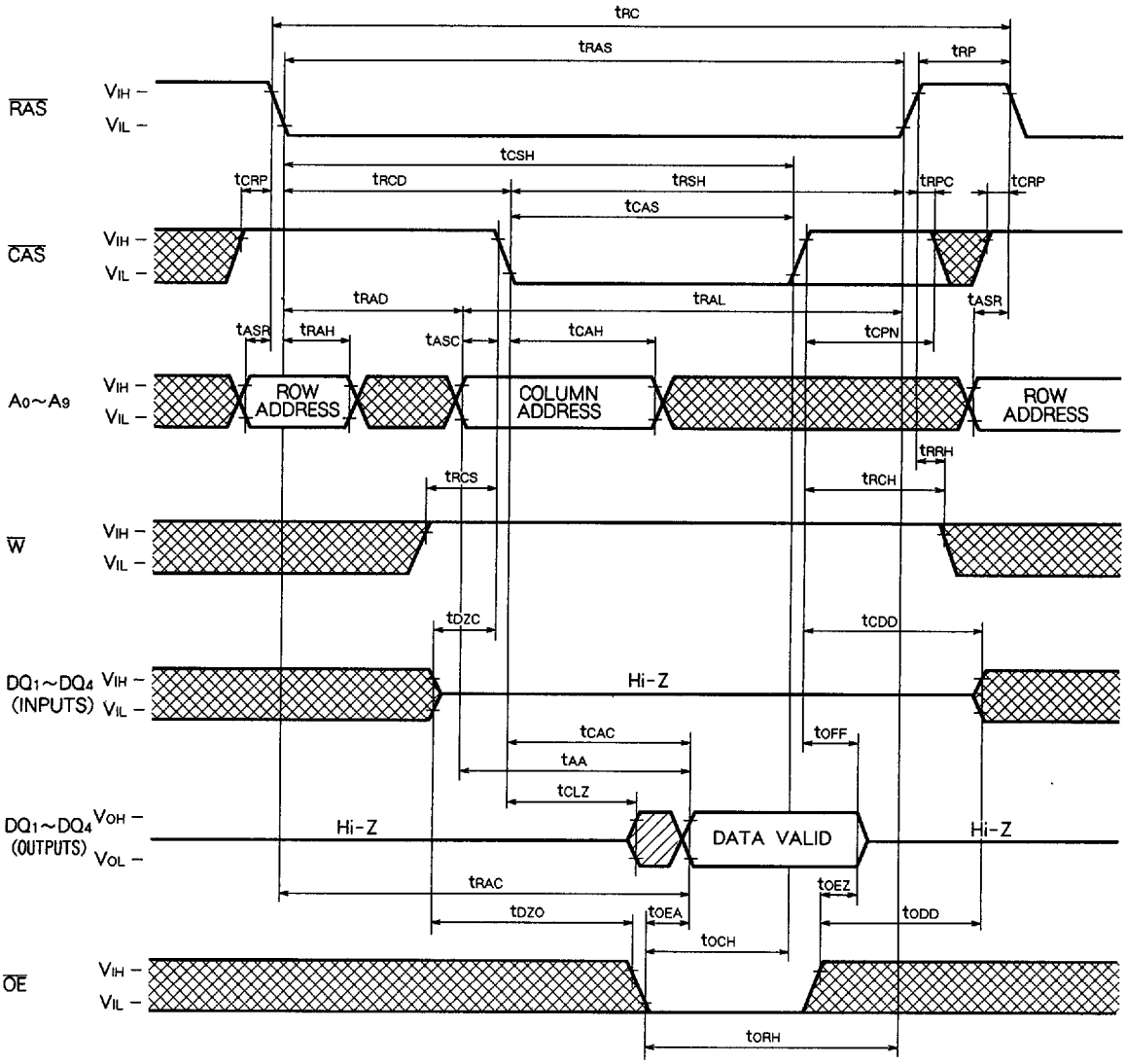
Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.

Timing Diagrams (Note 30)

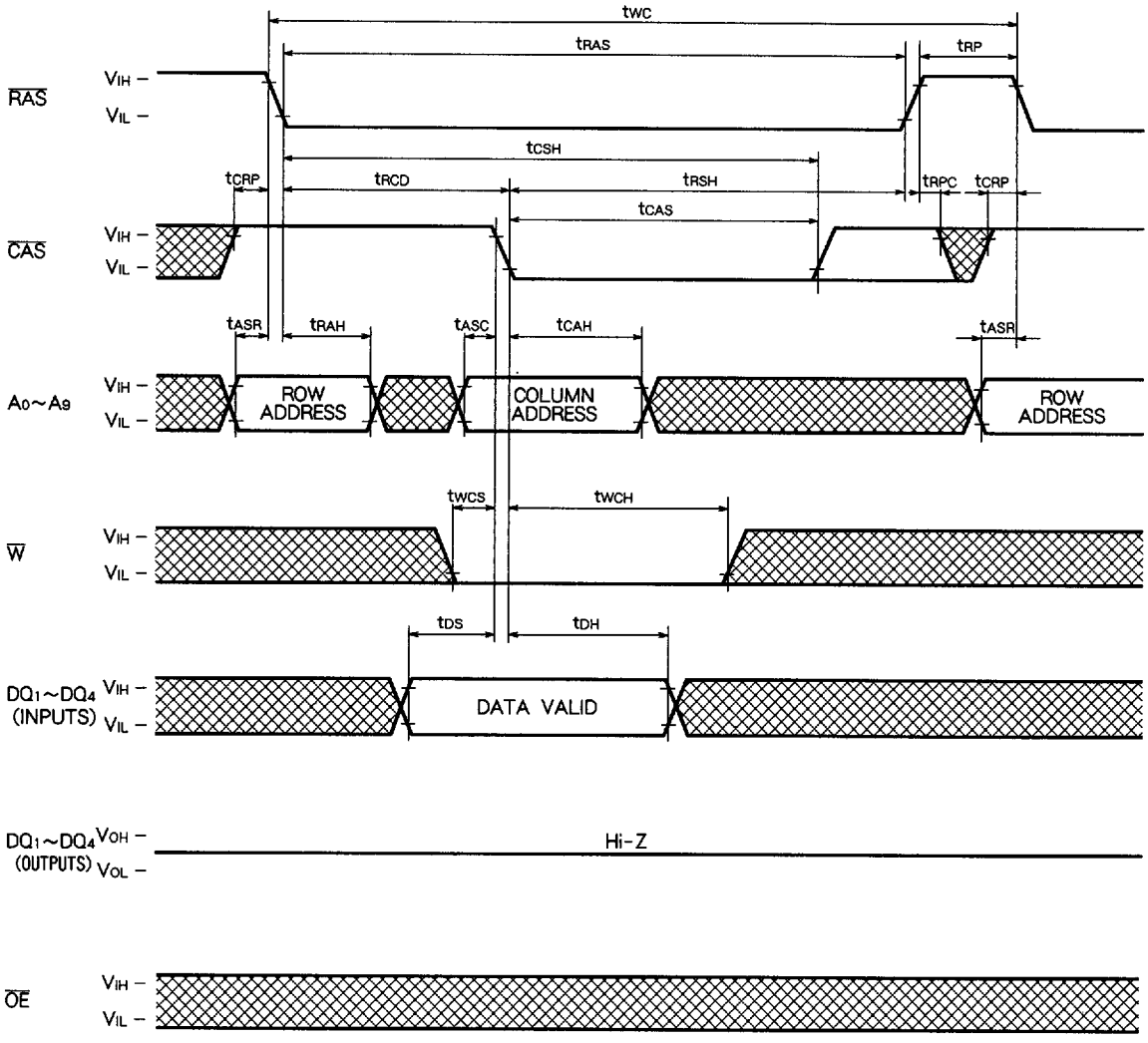
Read Cycle



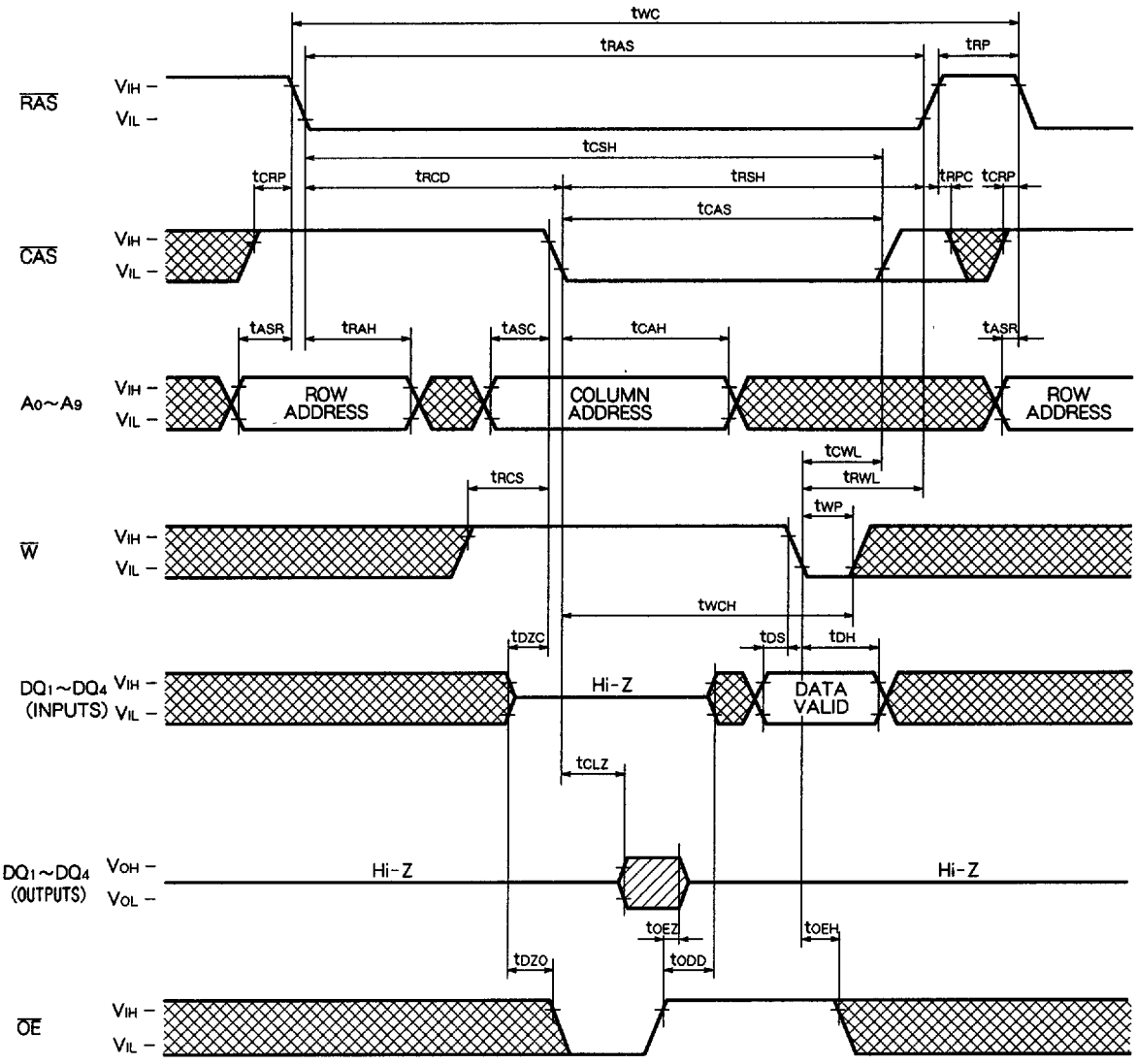
Note 30. Indicates the don't care input.
V_{IH} (min) ≦ V_{IN} ≦ V_{IH} (max) or V_{IL} (min) ≦ V_{IN} ≦ V_{IL} (max)

Indicates the invalid output.

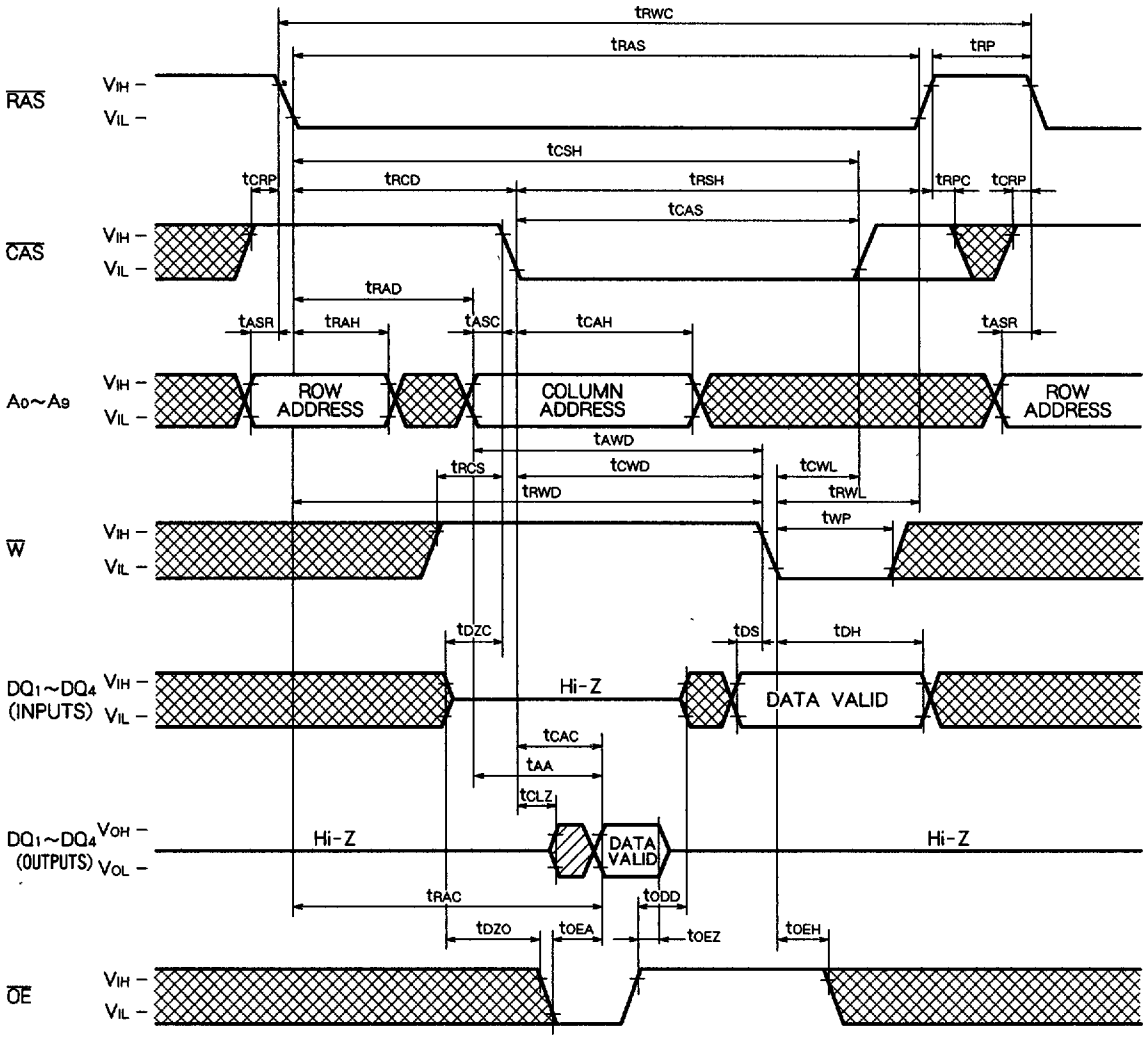
Write Cycle (Early write)



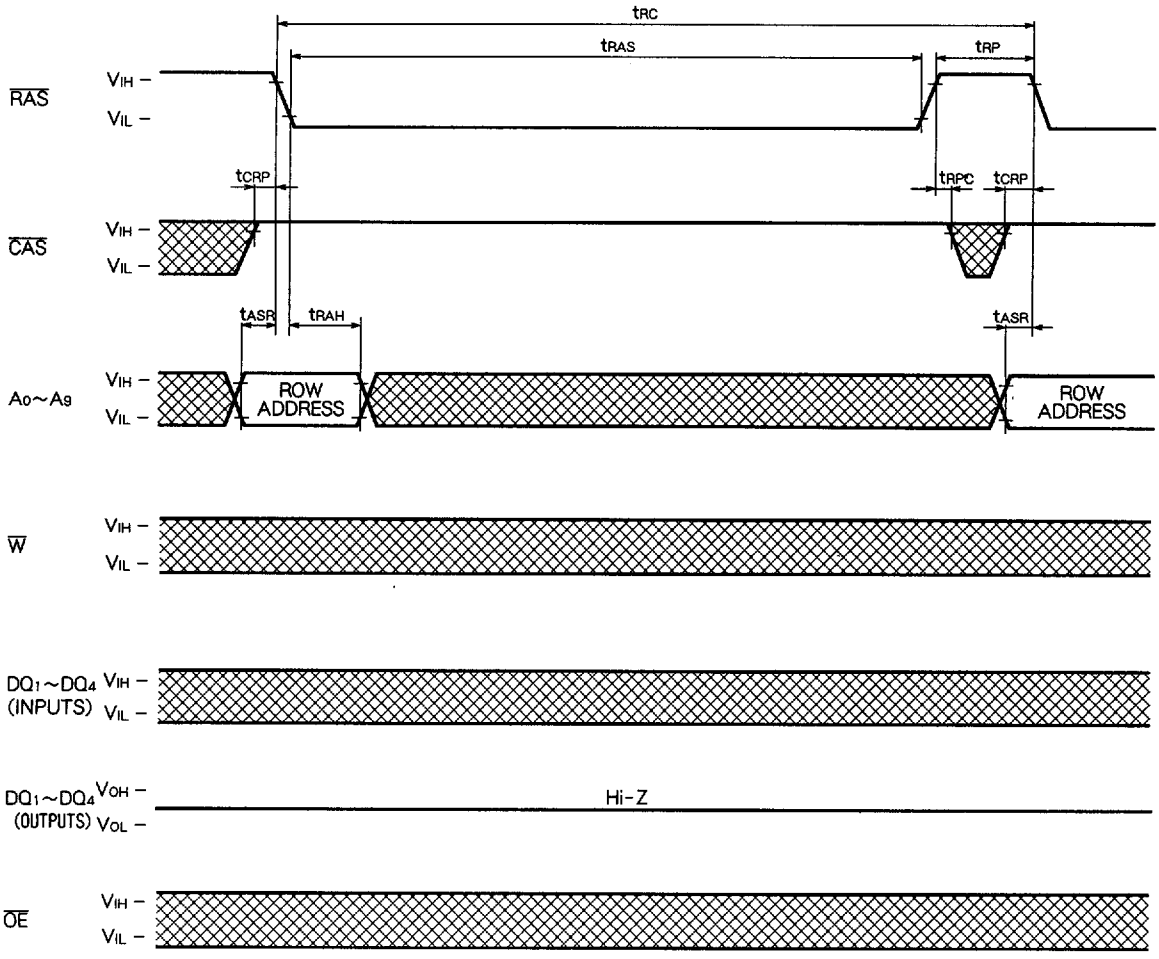
Write Cycle (Delayed Write)



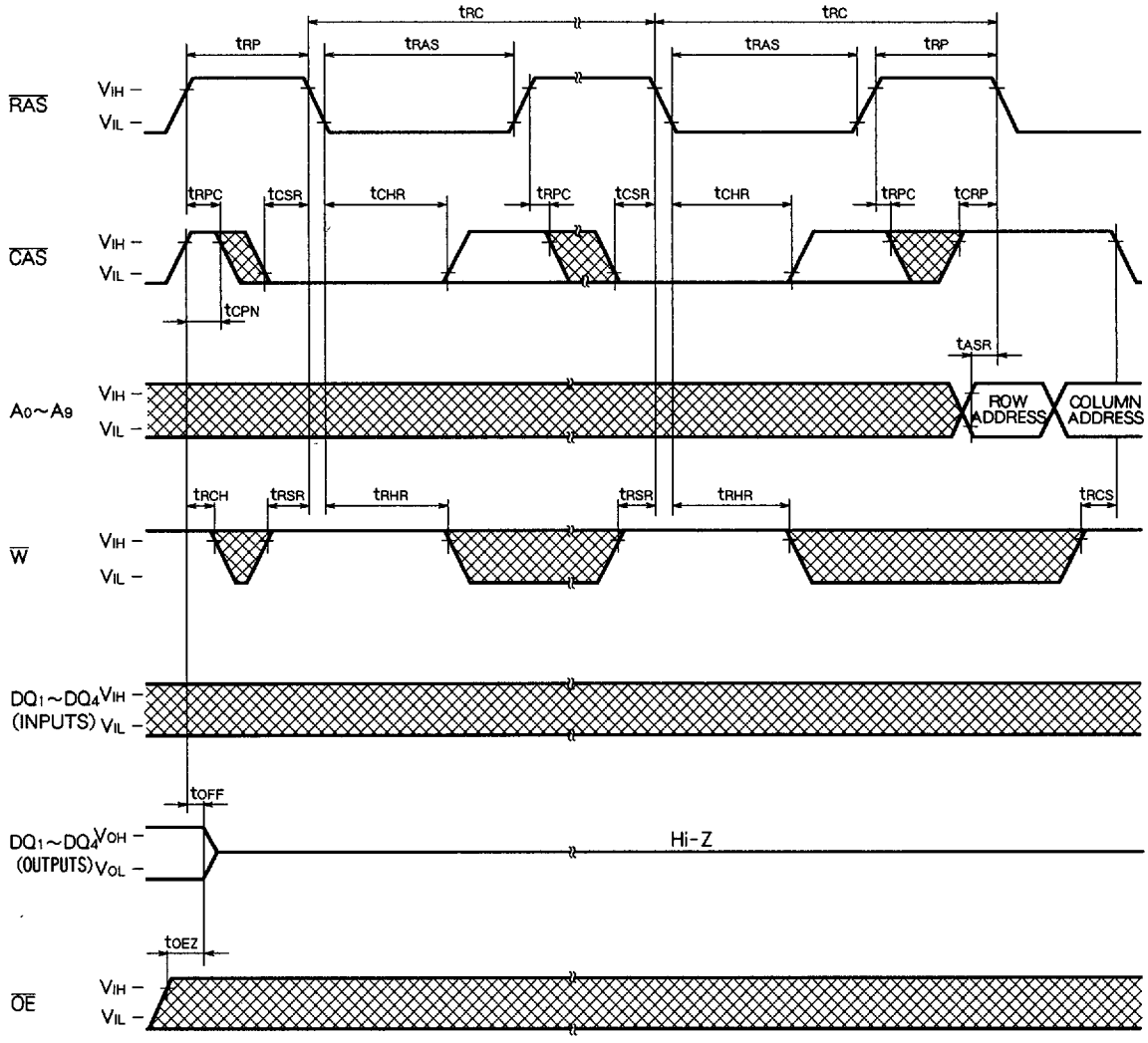
Read - Write, Read - Modify - Write Cycle



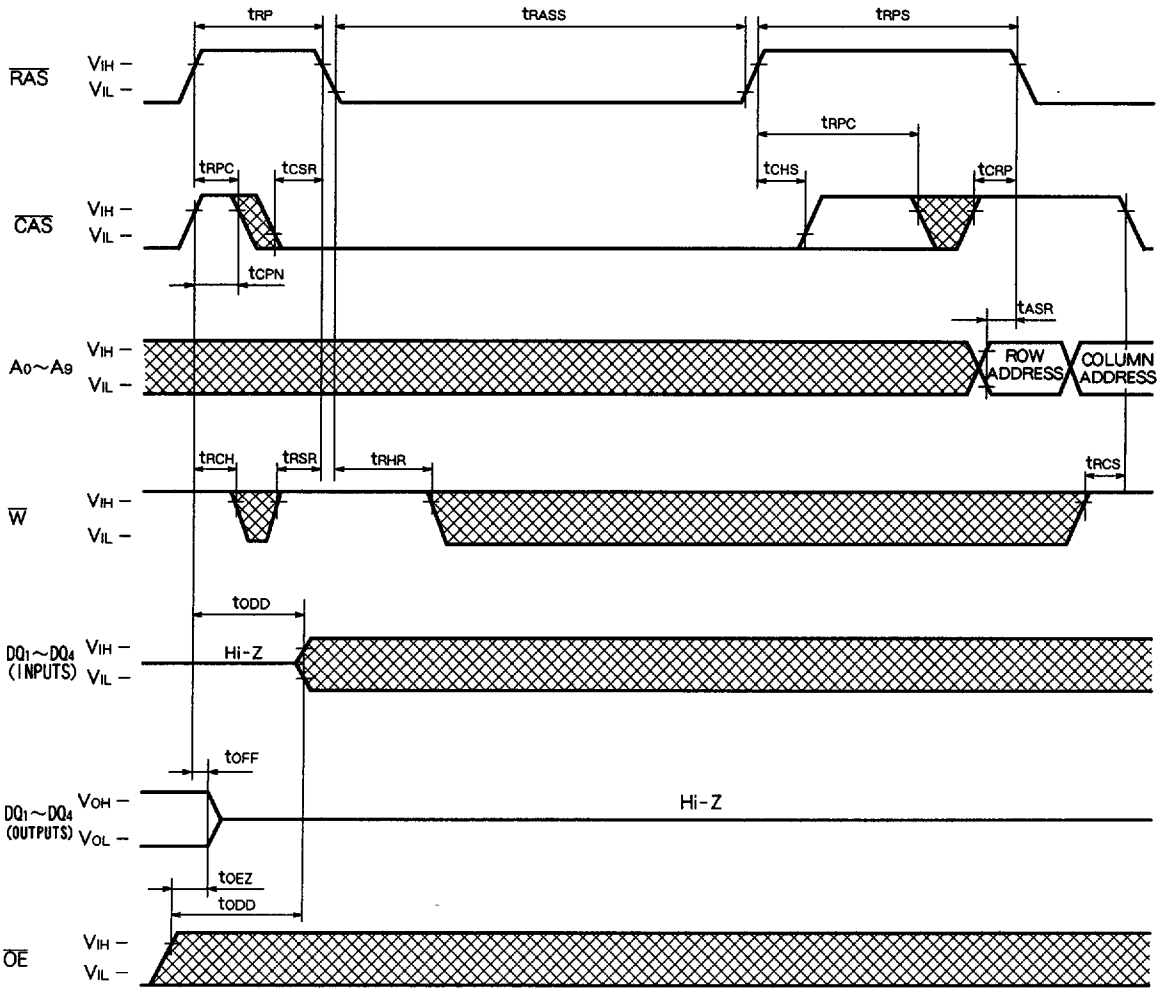
$\overline{RAS}$-only Refresh Cycle



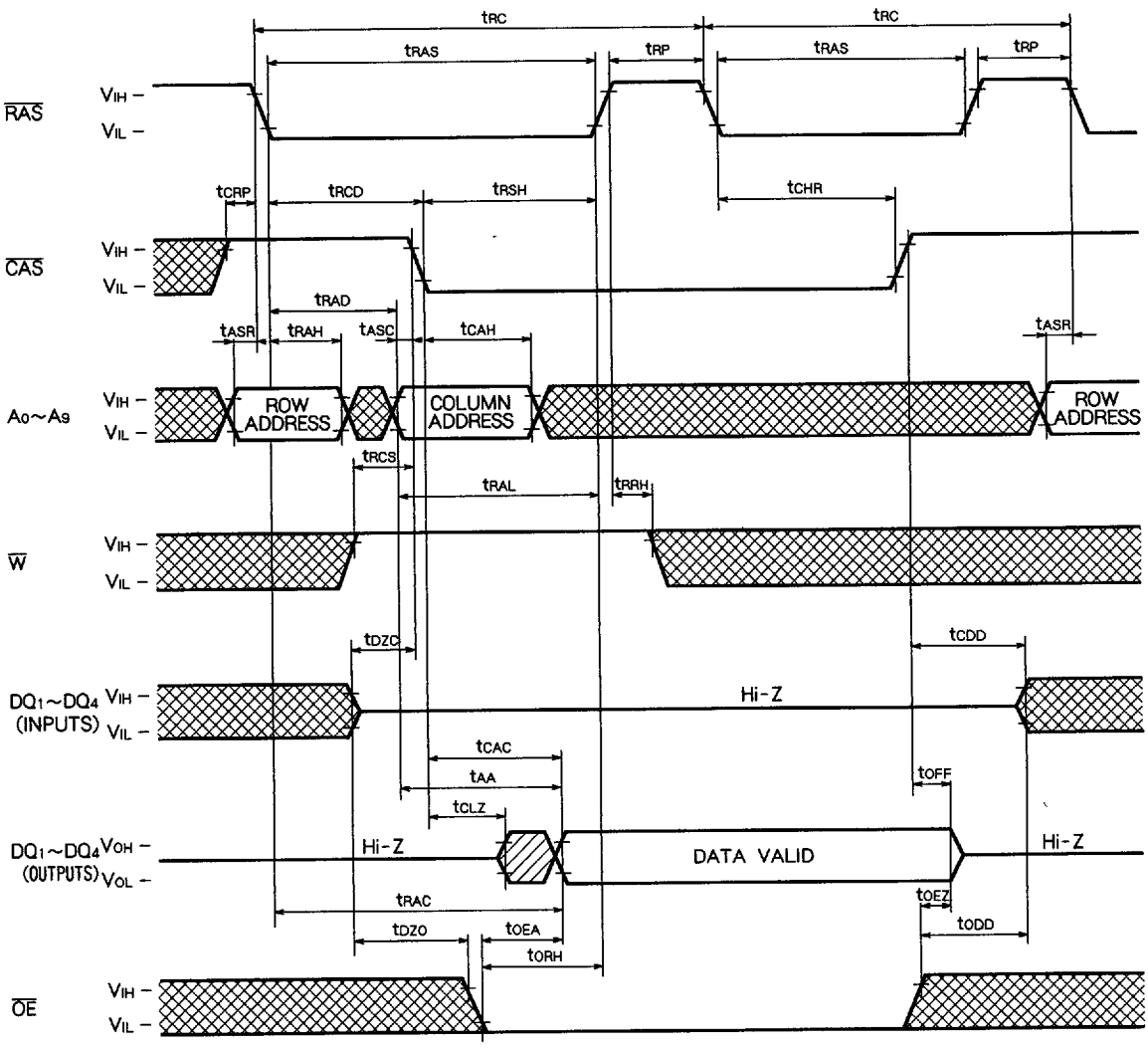
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



Self Refresh Cycle* (Note 29)

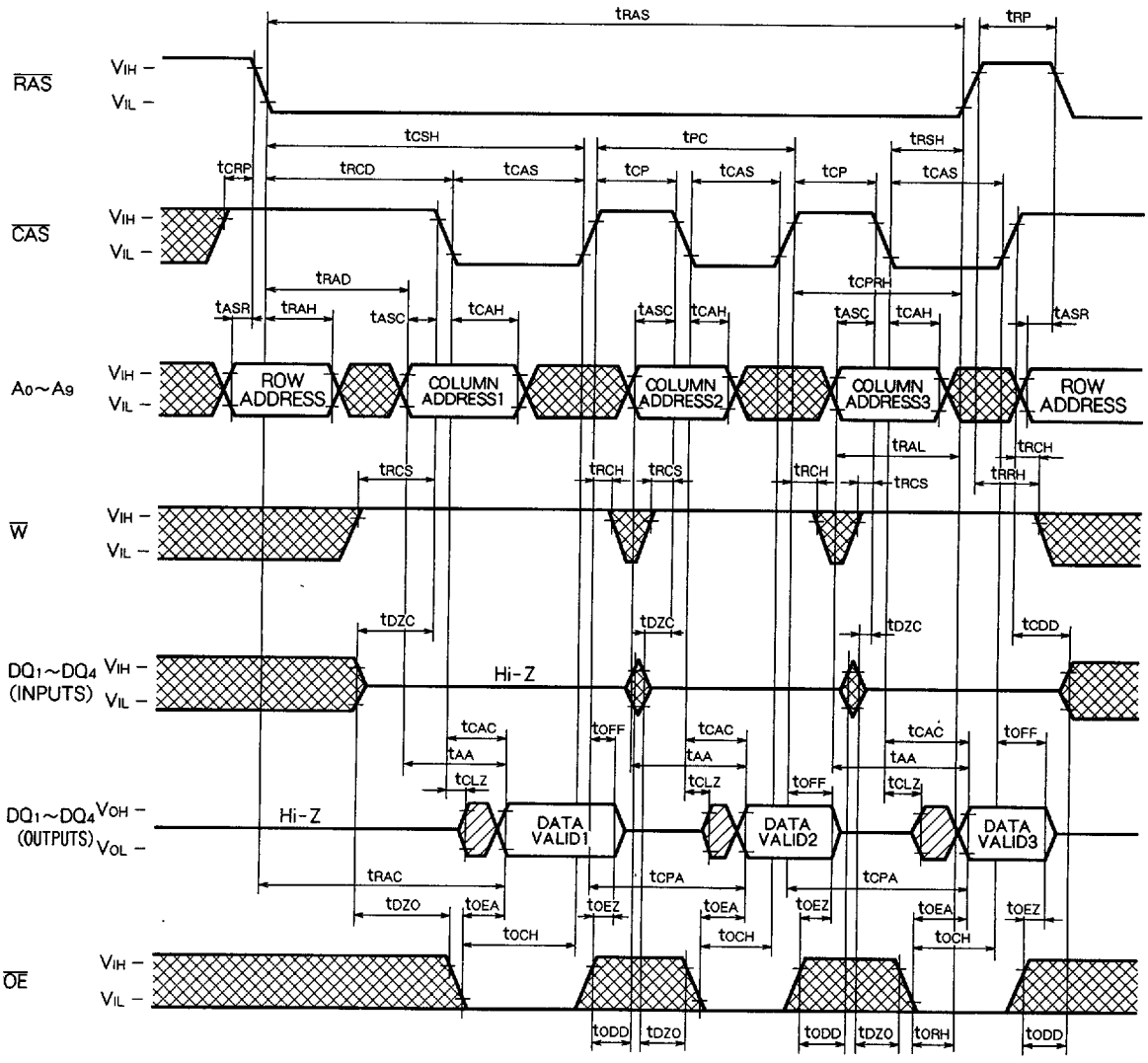


Hidden Refresh Cycle (Read) (Note 31)

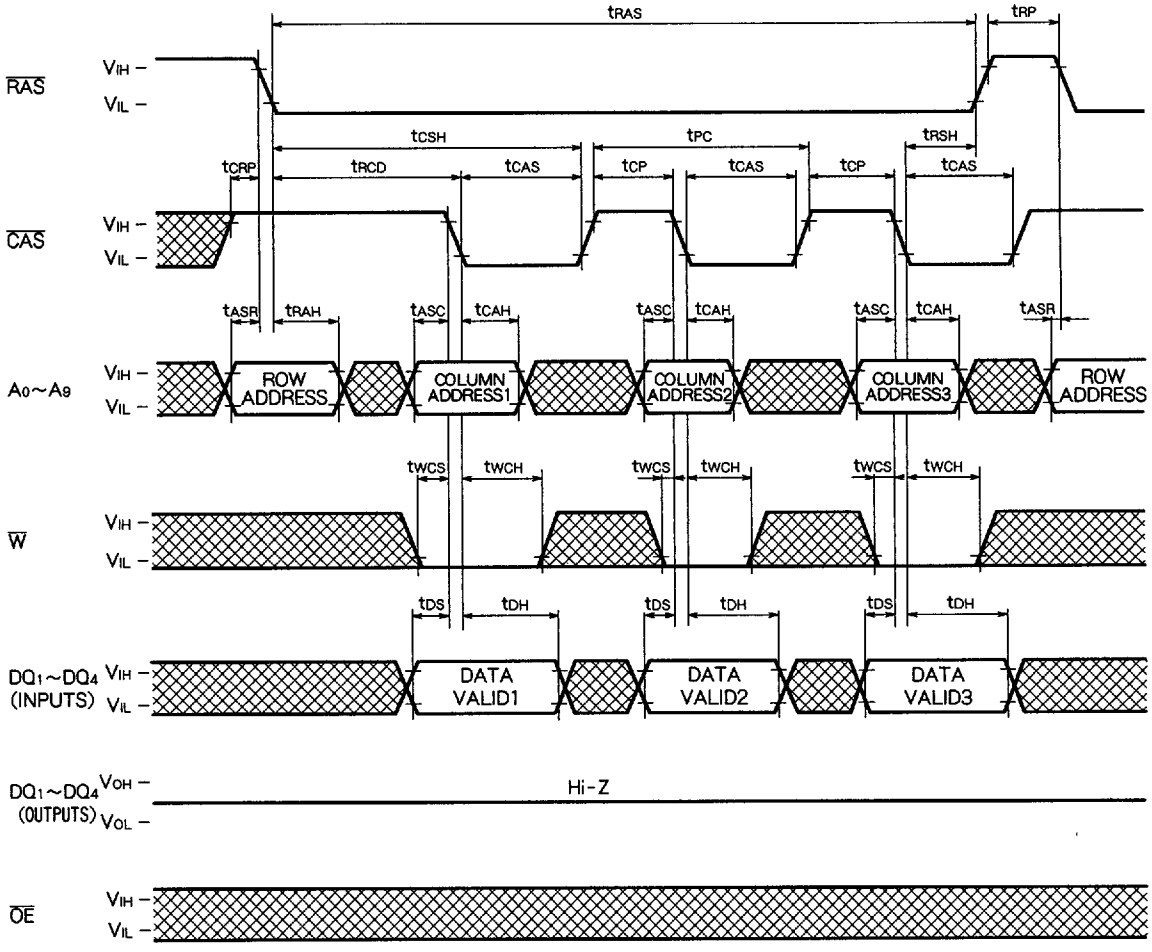


Note 31. Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

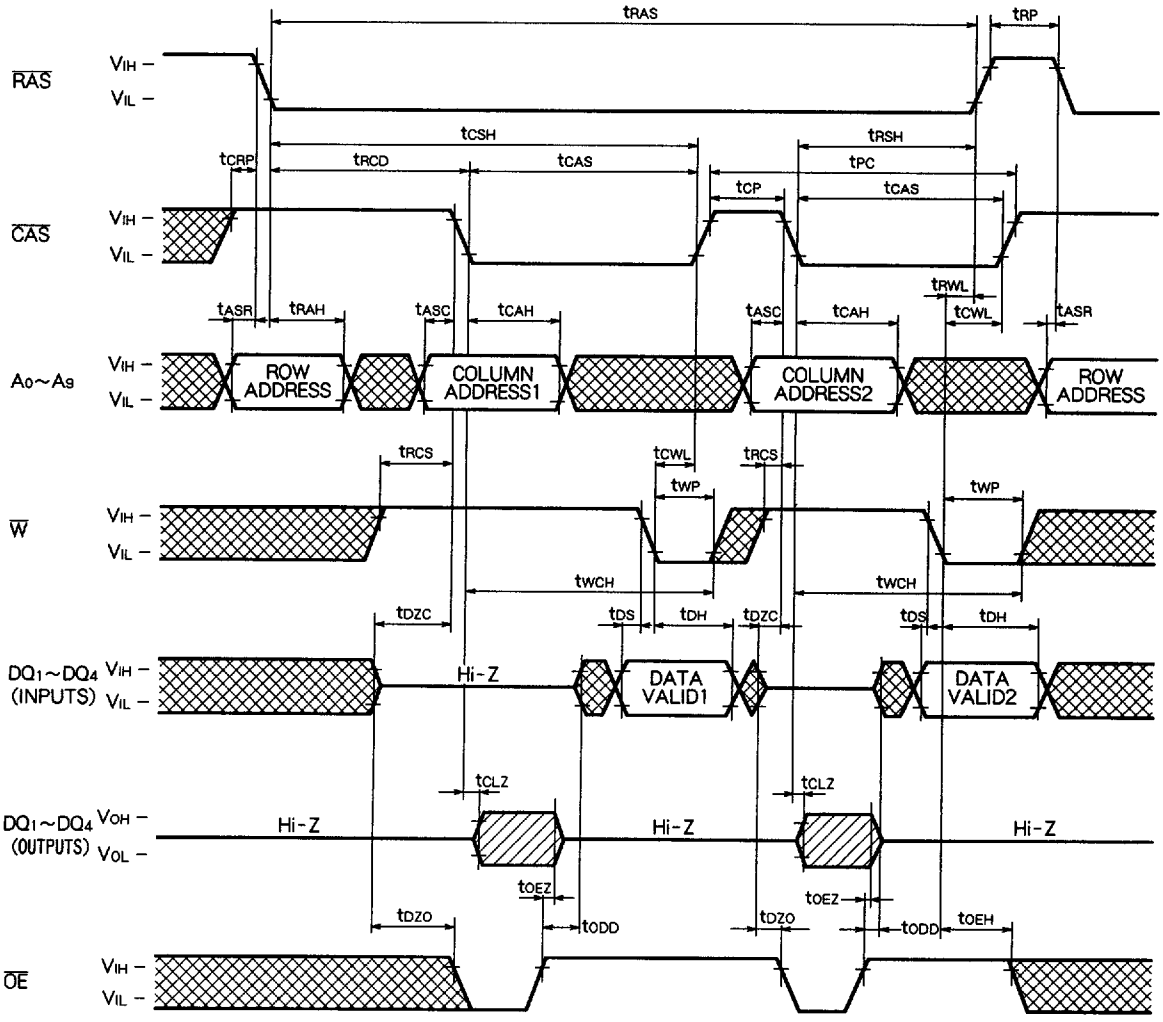
Fast Page Mode Read Cycle



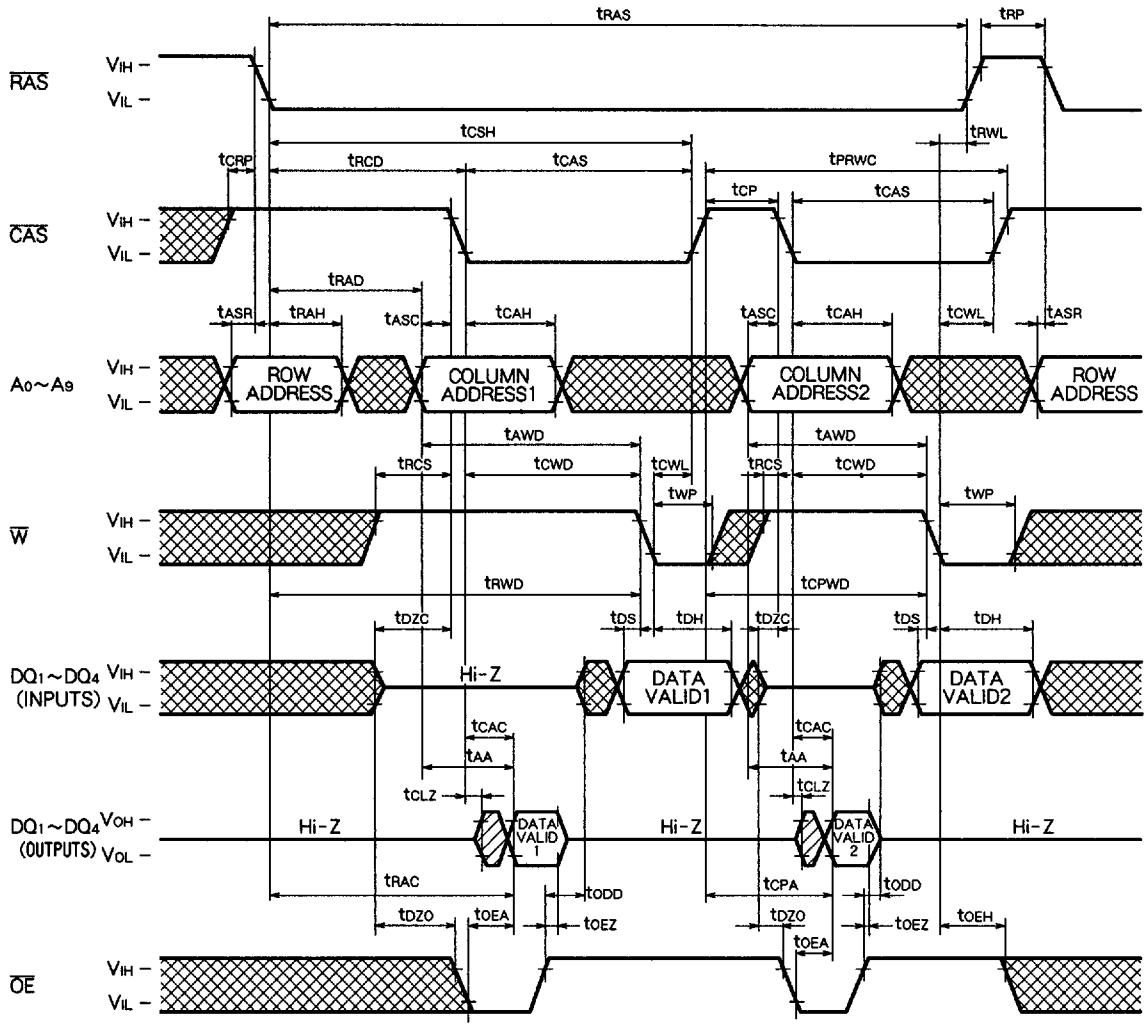
Fast Page Mode Write Cycle (Early Write)



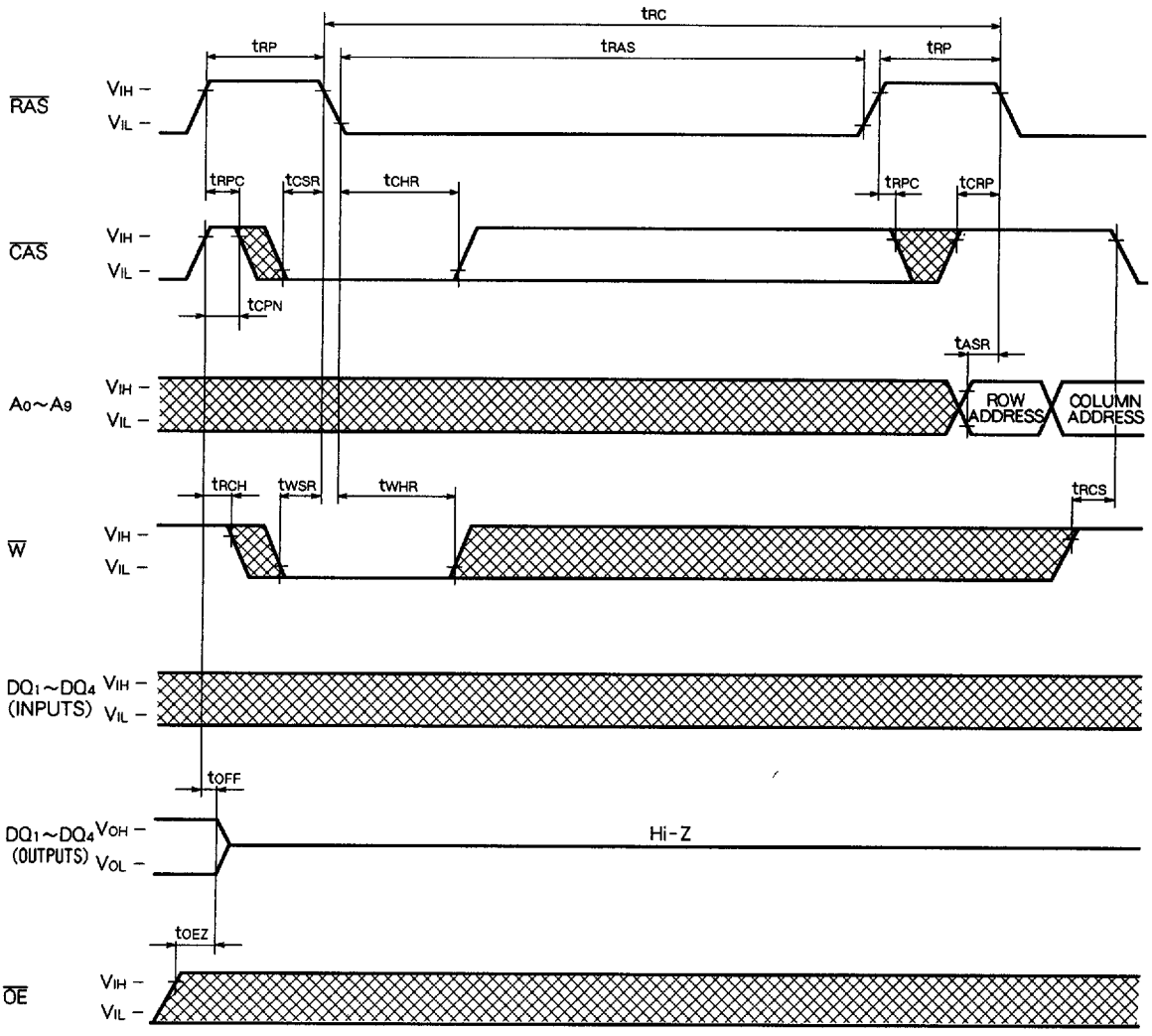
Fast Page Mode Write Cycle (Delayed Write)



Fast Page Mode Read-Write, Read-Modify-Write Cycle



Test Mode Set Cycle (Note 32)



Note 32. The cycle is also available for the initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ (CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 4 bits wide (256 kilobytes deep) for each DQ (input/output) port.
No addressing of A0, A1 (column only) is required.
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4 bits for each DQ port and can be written independently for each DQ port.
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4 bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.