TISP4165H4BJ THRU TISP4200H4BJ, TISP4265H4BJ THRU TISP4360H4BJ
BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

 NOVEMBER 1997 - REVISED MARCH 1999

HIGH HOLDING CURRENT 100 A 10/1000 OVERVOLTAGE PROTECTORS

- **8 kV 10/700, 200 A 5/310 ITU-T K20/21 rating**
- **High Holding Current . . . . . 225 mA min.**
- **Ion-Implanted Breakdown Region**
  Precise and Stable Voltage
  Low Voltage Overshoot under Surge

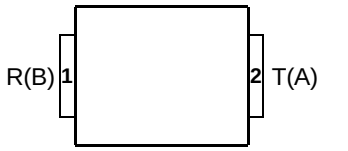
DEVICE	V_{DRM} MINIMUM V	$V_{(BO)}$ MAXIMUM V
‘4165	135	165
‘4180	145	180
‘4200	155	200
‘4265	200	265
‘4300	230	300
‘4360	270	360

- **Rated for International Surge Wave Shapes**

WAVE SHAPE	STANDARD	I_{TSP} A
2/10 µs	GR-1089-CORE	500
8/20 µs	IEC 61000-4-5	300
10/160 µs	FCC Part 68	250
10/700 µs	ITU-T K20/21	200
10/560 µs	FCC Part 68	160
10/1000 µs	GR-1089-CORE	100

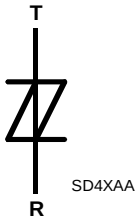
- **Low Differential Capacitance . . . 39 pF max.**

SMBJ PACKAGE
(TOP VIEW)



MDXXBG

device symbol



SD4XAA

Terminals T and R correspond to the alternative line designators of A and B

description

These devices are designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring and Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current prevents d.c. latchup as the diverted current subsides.

This TISP4xxxH4BJ range consists of six voltage variants to meet various maximum system voltage levels (135 V to 270 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These high (H) current protection devices are in a plastic package SMBJ (JEDEC DO-214AA with J-bend leads) and supplied in embossed carrier reel pack. For alternative voltage and holding current values, consult the factory. For lower rated impulse currents in the SMB package, the 50 A 10/1000 TISP4xxxM3BJ series is available.

absolute maximum ratings, T_A = 25°C (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Repetitive peak off-state voltage, (see Note 1)	'4165	V_{DRM}	±135	V
	'4180		±145	
	'4200		±155	
	'4265		±200	
	'4300		±230	
	'4360		±270	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)		I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)			500	
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage, 8/20 current combination wave generator)			300	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)			250	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)			220	
0.2/310 µs (I3124, 0.5/700 µs voltage wave shape)			200	
5/310 µs (ITU-T K20/21, 10/700 µs voltage wave shape)			200	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)			200	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)			160	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)			100	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)		I_{TSM}		A
20 ms (50 Hz) full sine wave			55	
16.7 ms (60 Hz) full sine wave			60	
1000 s 50 Hz/60 Hz a.c.			2.1	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A		di_T/dt	400	A/µs
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-65 to +150	°C

NOTES: 1. See Applications Information and Figure 10 for voltage values at lower temperatures.
2. Initially the TISP4xxxH4BJ must be in thermal equilibrium with T_J = 25°C.
3. The surge may be repeated after the TISP4xxxH4BJ returns to its initial conditions.
4. See Applications Information and Figure 11 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 8 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C

electrical characteristics for the T and R terminals, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DRM}	Repetitive peak off-state current	$V_D = \pm V_{DRM}$	T_A = 25°C			±5	µA
			T_A = 85°C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	'4165			±165	V
			'4180			±180	
			'4200			±200	
			'4265			±265	
			'4300			±300	
			'4360			±360	
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A	'4165			±174	V
			'4180			±189	
			'4200			±210	
			'4265			±276	
			'4300			±311	
			'4360			±373	
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.8	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 µs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.225		±0.8	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/µs
I_D	Off-state current	V_D = ±50 V	T_A = 85°C			±10	µA
C_{off}	Off-state capacitance	f = 100 kHz, V_d = 1 V rms, V_D = 0,	'4165 thru '4200		80	90	pF
			'4265 thru '4360		70	84	
		f = 100 kHz, V_d = 1 V rms, V_D = -1 V	'4165 thru '4200		71	79	
			'4265 thru '4360		60	67	
		f = 100 kHz, V_d = 1 V rms, V_D = -2 V	'4165 thru '4200		65	74	
			'4265 thru '4360		55	62	
		f = 100 kHz, V_d = 1 V rms, V_D = -50 V	'4165 thru '4200		30	35	
			'4265 thru '4360		24	28	
		f = 100 kHz, V_d = 1 V rms, V_D = -100 V	'4165 thru '4200		28	33	
			'4265 thru '4360		22	26	

thermal characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 6)			113	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C		50		

NOTE 6: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

PARAMETER MEASUREMENT INFORMATION

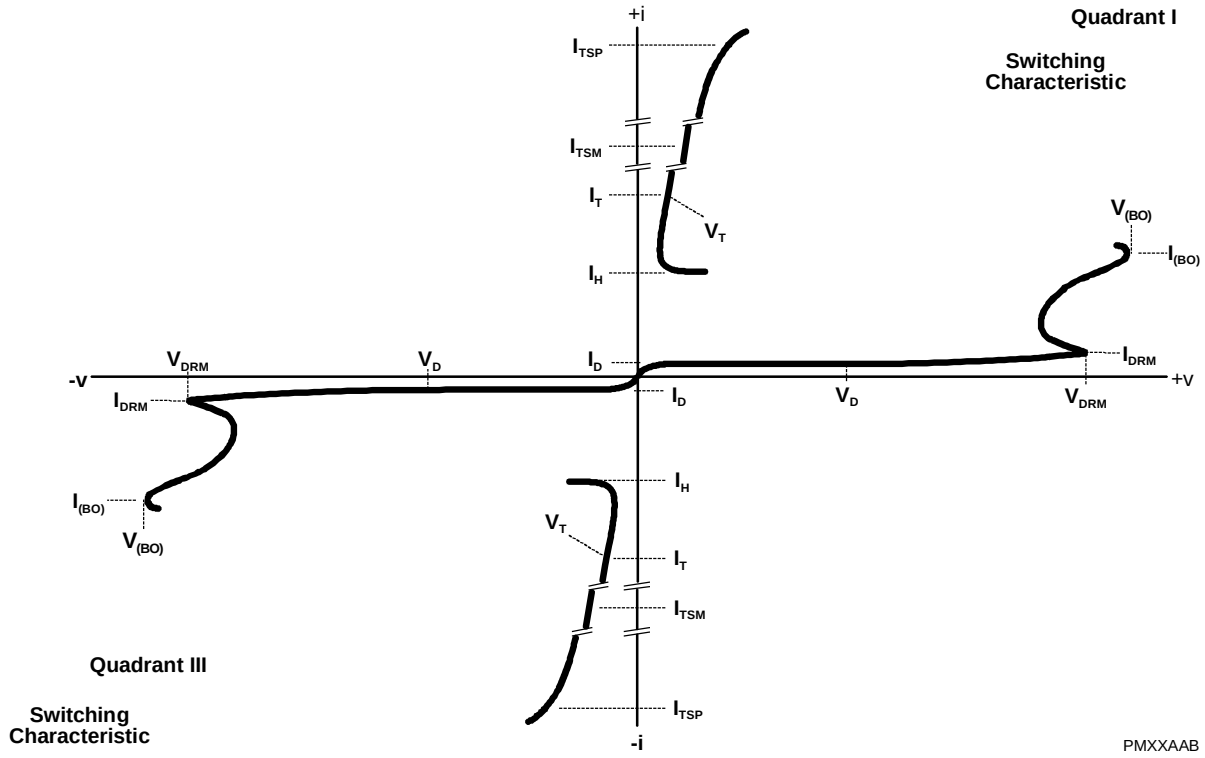


Figure 1. VOLTAGE-CURRENT CHARACTERISTIC FOR T AND R TERMINALS
ALL MEASUREMENTS ARE REFERENCED TO THE R TERMINAL

TYPICAL CHARACTERISTICS

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

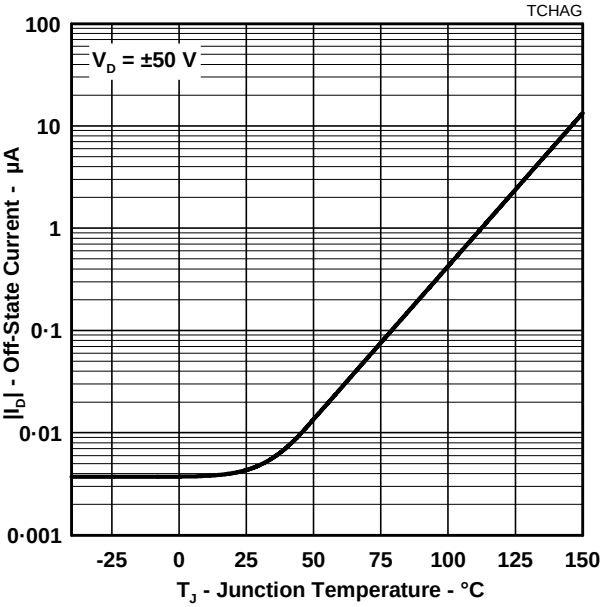


Figure 2.

NORMALISED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

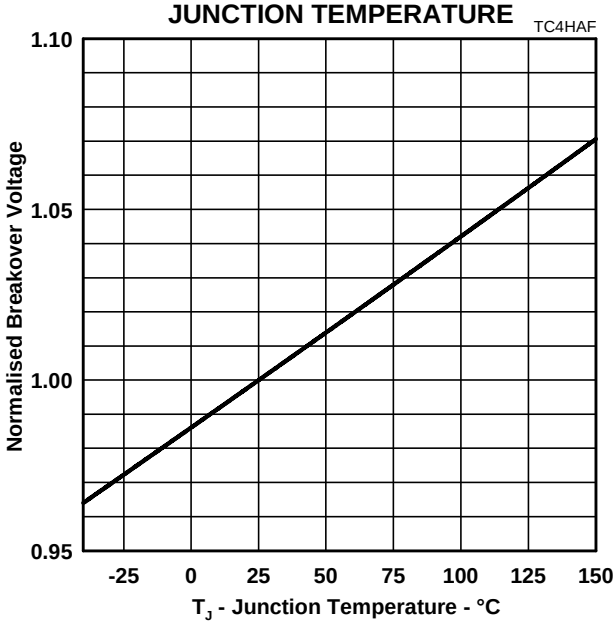


Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

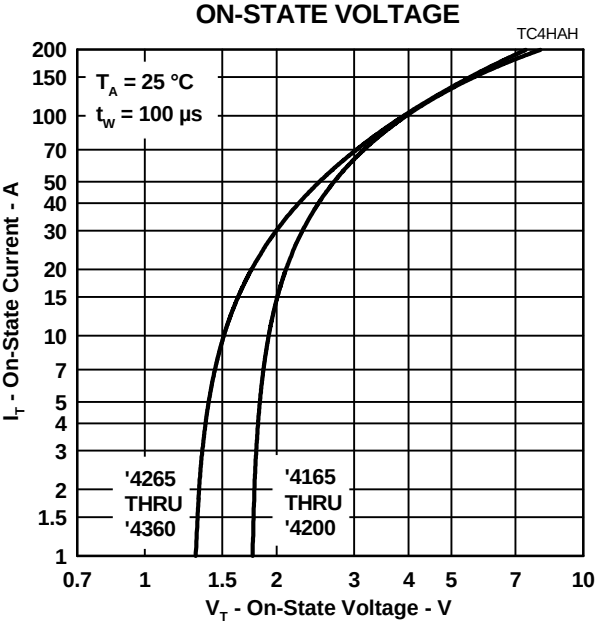


Figure 4.

NORMALISED HOLDING CURRENT vs JUNCTION TEMPERATURE

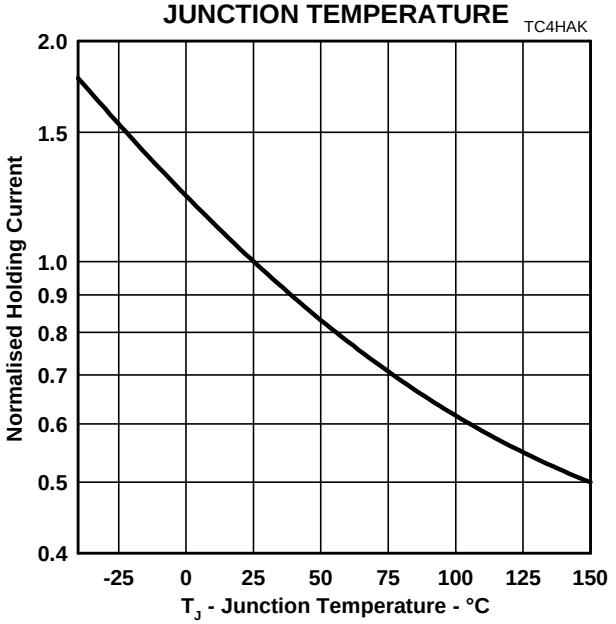


Figure 5.

TYPICAL CHARACTERISTICS

NORMALISED CAPACITANCE vs OFF-STATE VOLTAGE

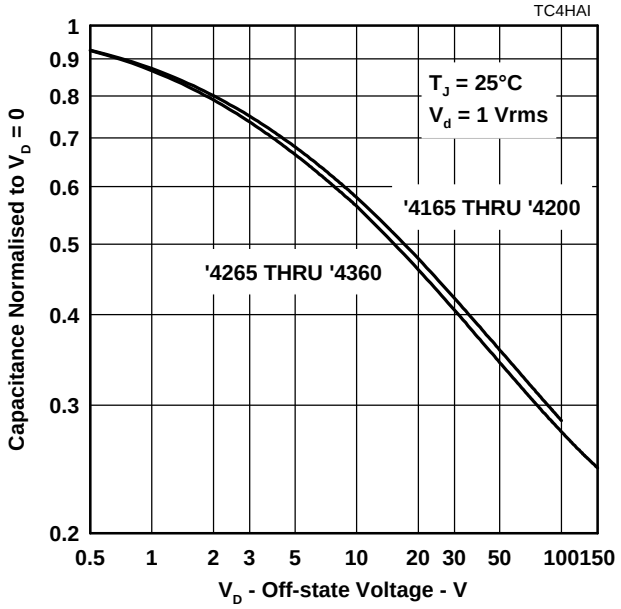


Figure 6.

DIFFERENTIAL OFF-STATE CAPACITANCE vs RATED REPETITIVE PEAK OFF-STATE VOLTAGE

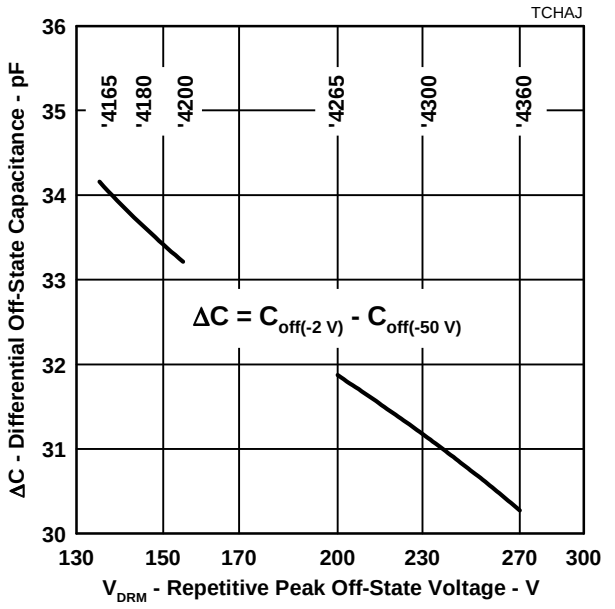


Figure 7.

RATING AND THERMAL INFORMATION

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

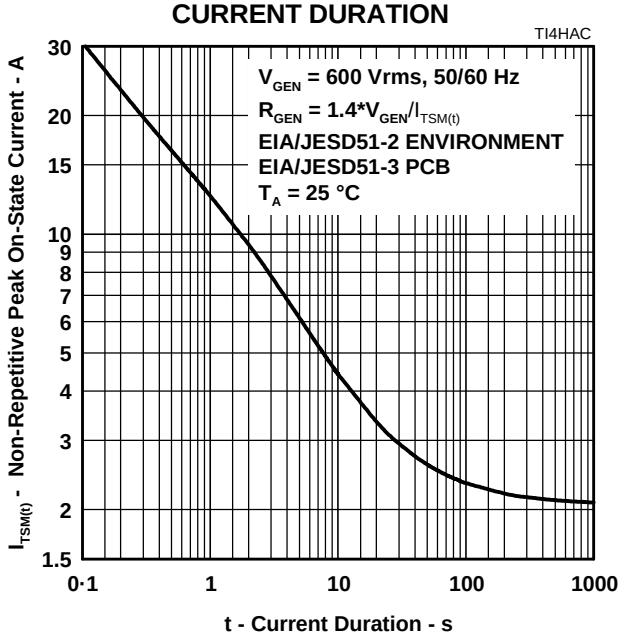


Figure 8.

THERMAL IMPEDANCE vs POWER DURATION

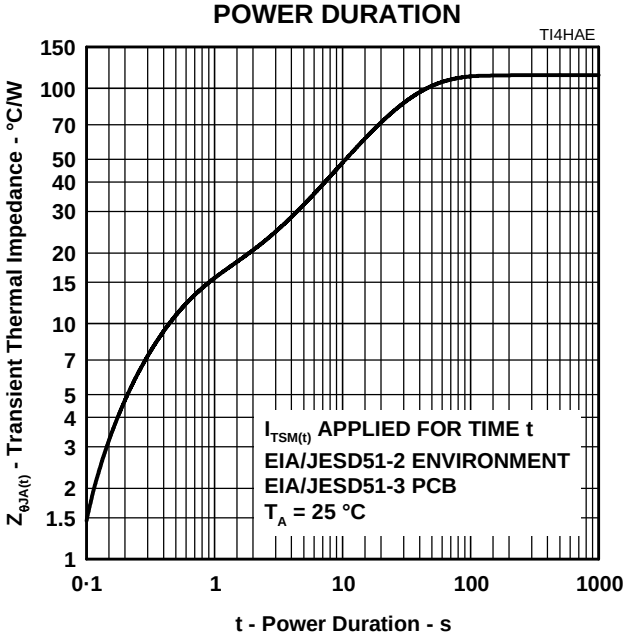


Figure 9.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

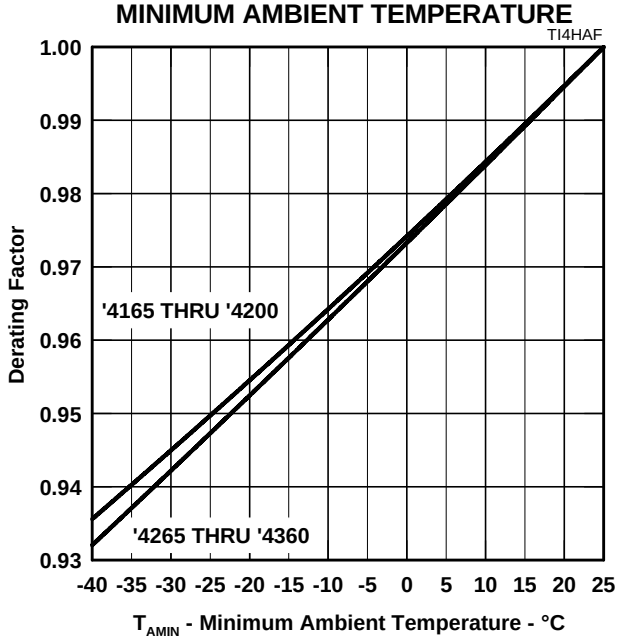


Figure 10.

IMPULSE RATING vs AMBIENT TEMPERATURE

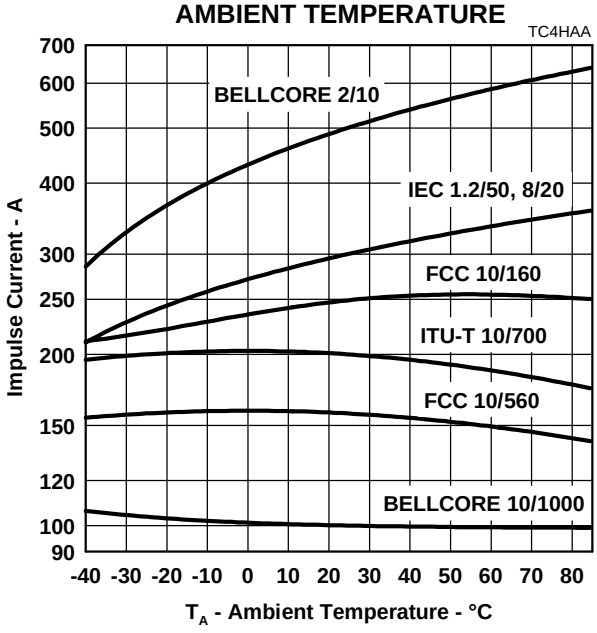


Figure 11.

APPLICATIONS INFORMATION

deployment

These devices are two terminal overvoltage protectors. They may be used either singly to limit the voltage between two conductors (Figure 12) or in multiples to limit the voltage at several points in a circuit (Figure 13).

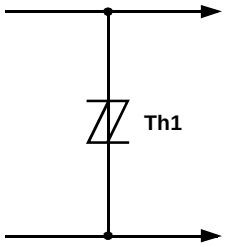


Figure 12. TWO POINT PROTECTION

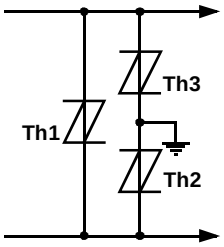


Figure 13. MULTI-POINT PROTECTION

In Figure 12, protector Th1 limits the maximum voltage between the two conductors to $\pm V_{(BO)}$. This configuration is normally used to protect circuits without a ground reference, such as modems. In Figure 13, protectors Th2 and Th3 limit the maximum voltage between each conductor and ground to the $\pm V_{(BO)}$ of the individual protector. Protector Th1 limits the maximum voltage between the two conductors to its $\pm V_{(BO)}$ value. If the equipment being protected has all its vulnerable components connected between the conductors and ground, then protector Th1 is not required.

impulse testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

STANDARD	PEAK VOLTAGE SETTING V	VOLTAGE WAVE FORM µs	PEAK CURRENT VALUE A	CURRENT WAVE FORM µs	TISP4xxxH4 25 °C RATING A	SERIES RESISTANCE Ω
GR-1089-CORE	2500	2/10	500	2/10	500	0
	1000	10/1000	100	10/1000	100	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	250	0
	800	10/560	100	10/560	160	0
	1500	9/720 †	37.5	5/320 †	200	0
	1000	9/720 †	25	5/320 †	200	0
I3124	1500	0.5/700	37.5	0.2/310	200	0
ITU-T K20/K21	1500 4000	10/700	37.5 100	5/310	200	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K21 10/700 impulse generator

If the impulse generator current exceeds the protectors current rating then a series resistance can be used to reduce the current to the protectors rated value and so prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generators peak voltage by the protectors rated current. The impulse generators fictive impedance (generators peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance. In some cases the equipment will require verification over a temperature range. By using the rated waveform values from Figure 11, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

a.c. power testing

The protector can withstand currents applied for times not exceeding those shown in Figure 8. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) resistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 8. In some cases there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, V_D, values of 0, -1 V, -2 V and -50 V. Where possible values are also given for -100 V. Values for other voltages may be calculated by multiplying the V_D = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz the capacitance is essentially independent of frequency. Above 10 MHz the effective capacitance is strongly dependent on connection inductance. In many applications, such as Figure 15 and Figure 17, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

normal system voltage levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition about 10 V of clipping is normally possible without activating the ring trip circuit.

Figure 10 allows the calculation of the protector V_{DRM} value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP4265H4BJ, with a V_{DRM} of 200 V, can be used for the protection of ring generators producing 100 V rms of ring on a battery voltage of -58 V (Th2 and Th3 in Figure 17). The peak ring voltage will be 58 + 1.414*100 = 199.4 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage. In the extreme case of an unconnected line, clipping the peak voltage to 190 V should not activate the ring trip. This level of clipping would occur at the temperature when the V_{DRM} has reduced to 190/200 = 0.95 of its 25 °C value. Figure 10 shows that this condition will occur at an ambient temperature of -22 °C. In this example, the TISP4265H4BJ will allow normal equipment operation provided that the minimum expected ambient temperature does not fall below -22 °C.

JESD51 thermal measurement method

To standardise thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the centre. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm on a side and the other for packages up to 48 mm. The SMBJ measurements used the smaller 76.2 mm x 114.3 mm (3.0 “ x 4.5 “) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worse case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance and so can dissipate higher power levels than indicated by the JESD51 values.

typical circuits

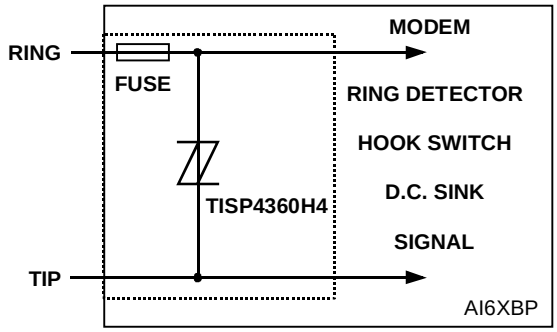


Figure 14. MODEM INTER-WIRE PROTECTION

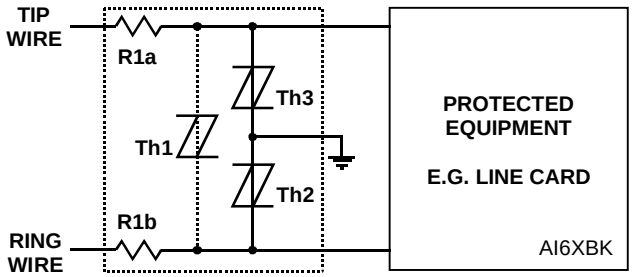


Figure 15. PROTECTION MODULE

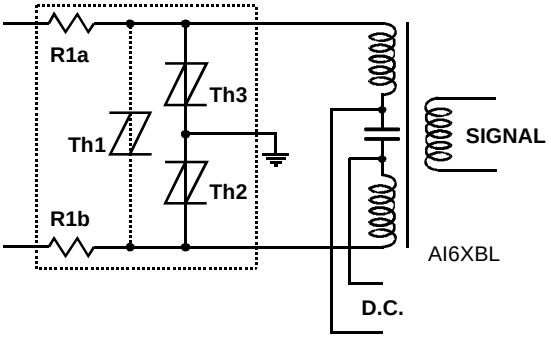


Figure 16. ISDN PROTECTION

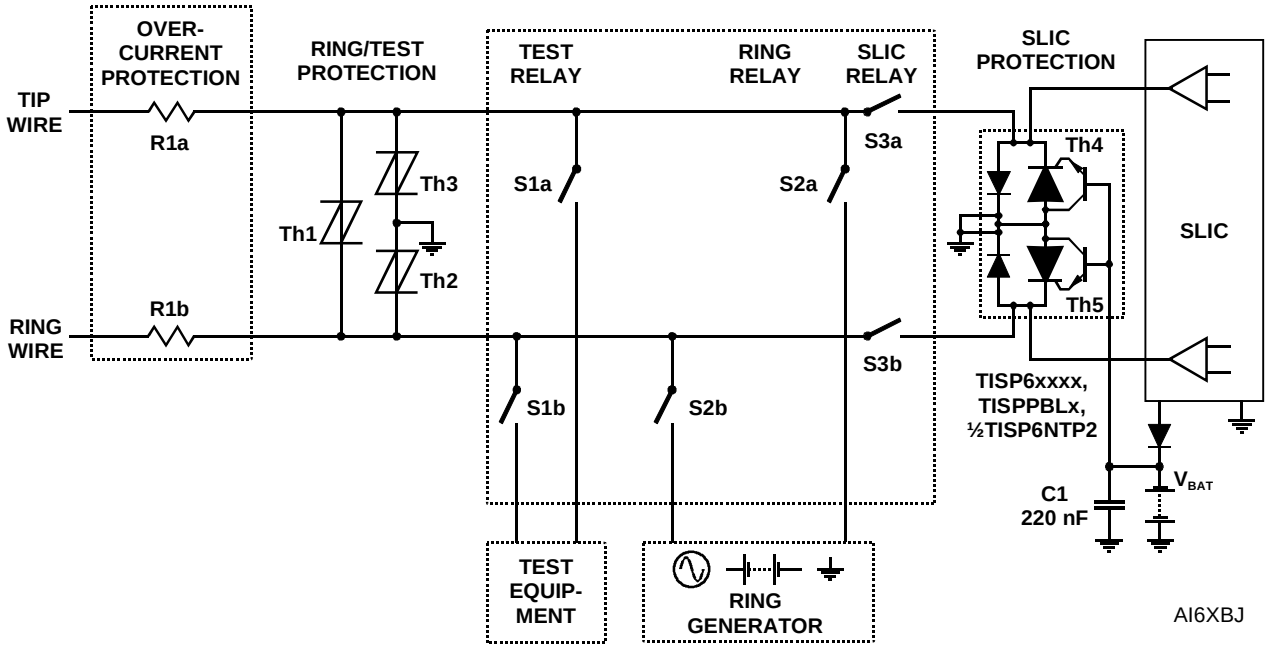


Figure 17. LINE CARD RING/TEST PROTECTION

PRODUCT INFORMATION

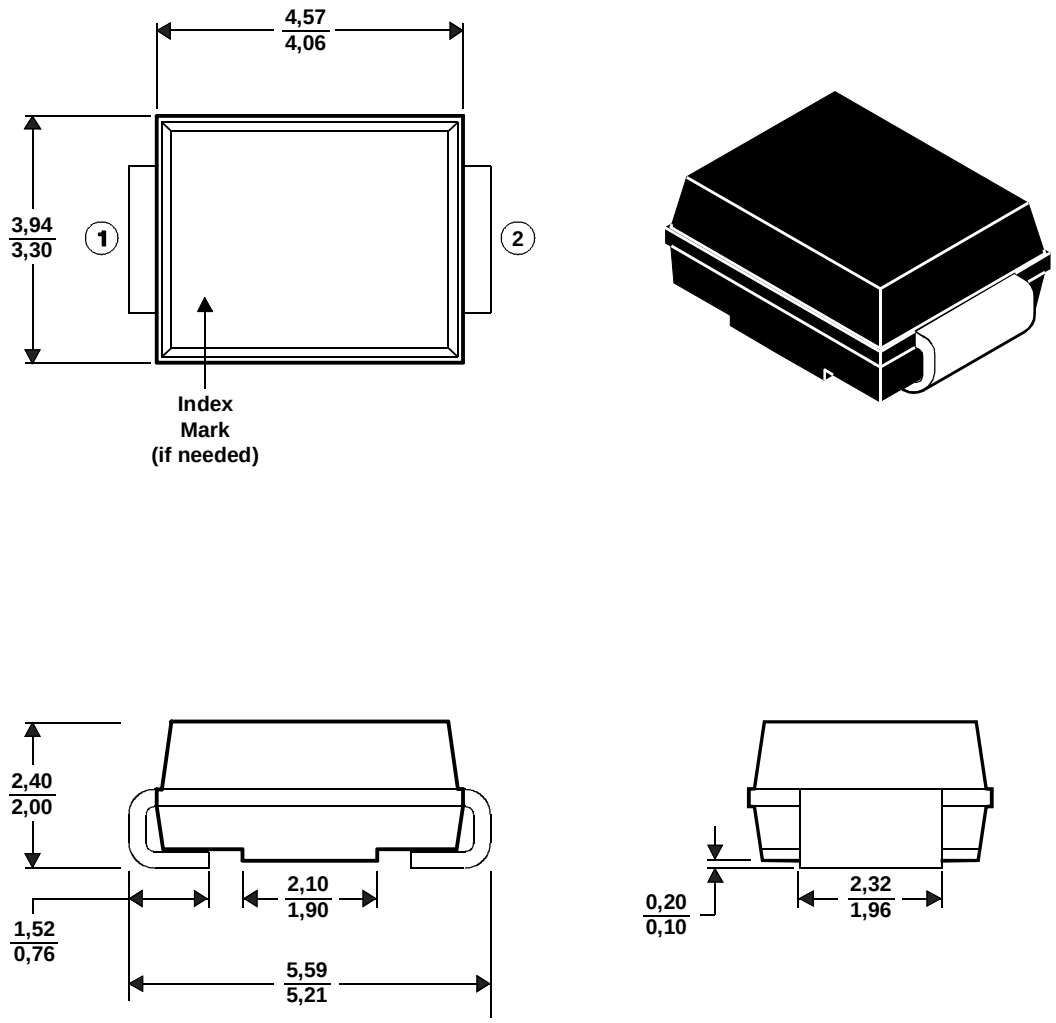
MECHANICAL DATA

SMBJ (DO-214AA)

plastic surface mount diode package

This surface mount package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

SMB



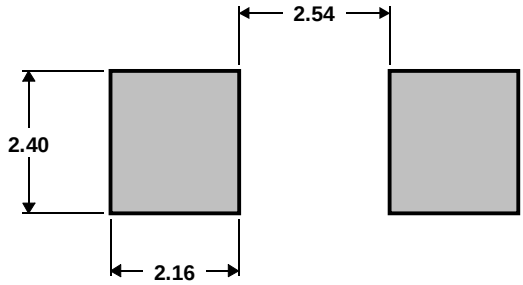
ALL LINEAR DIMENSIONS IN MILLIMETERS

MDXXBHA

MECHANICAL DATA

recommended printed wiring footprint.

SMB Pad Size



ALL LINEAR DIMENSIONS IN MILLIMETERS

MDXXBI

device symbolization code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

DEVICE	SYMOBLIZATION CODE
TISP4165H4BJ	4165H4
TISP4180H4BJ	4180H4
TISP4200H4BJ	4200H4
TISP4265H4BJ	4265H4
TISP4300H4BJ	4300H4
TISP4360H4BJ	4360H4

carrier information

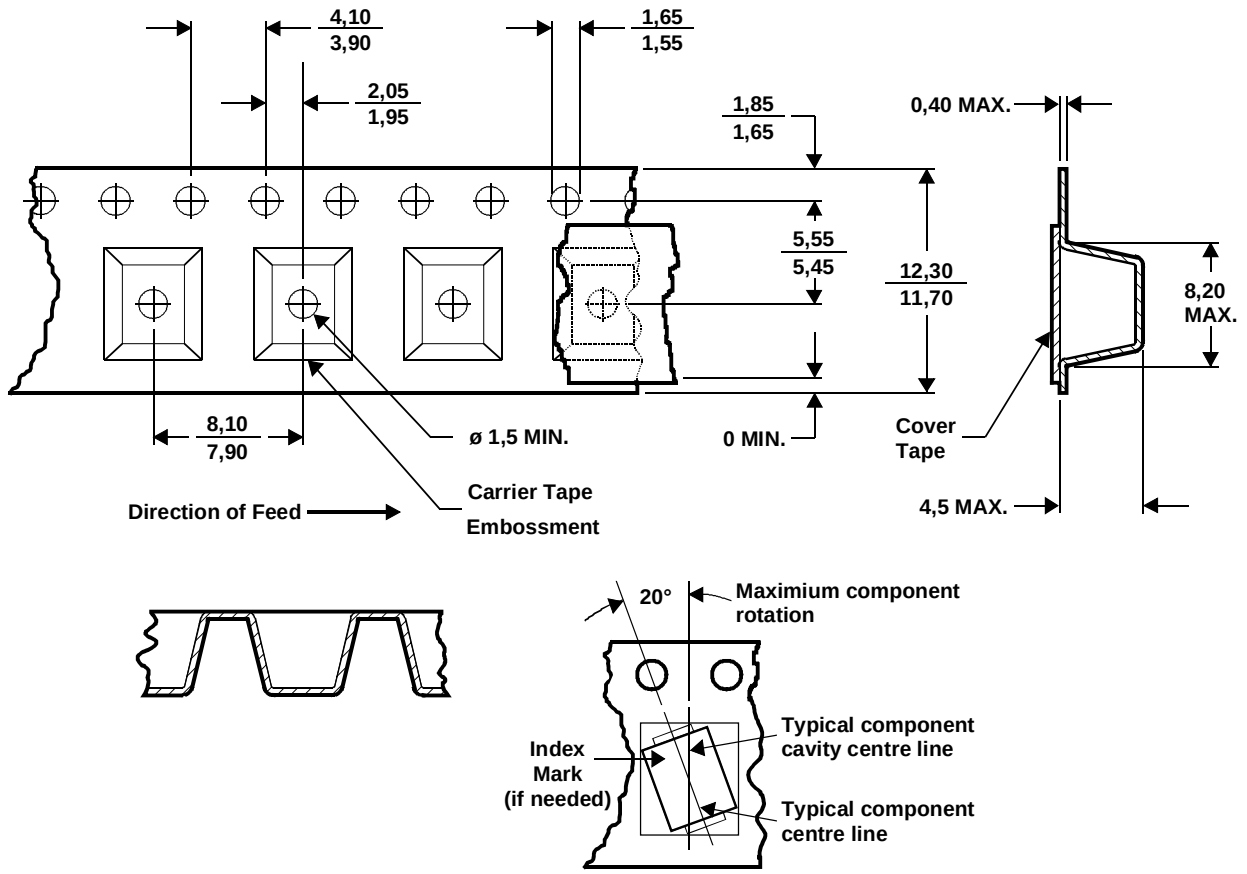
Devices are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer, devices will be shipped in the most practical carrier. For production quantities the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

CARRIER	ORDER #
Embossed Tape Reel Pack	TISP4xxxH4BJR
Bulk Pack	TISP4xxxH4BJ

MECHANICAL DATA

tape dimensions

SMB Package Single-Sprocket Tape



ALL LINEAR DIMENSIONS IN MILLIMETERS

NOTES: A. The clearance between the component and the cavity must be within 0,05 mm MIN. to 0,65 mm MAX. so that the component cannot rotate more than 20° within the determined cavity. MDXXBJ

B. Taped devices are supplied on a reel of the following dimensions:-

Reel diameter:	330 ±3,0 mm
Reel hub diameter	75 mm MIN.
Reel axial hole:	13,0 ±0,5 mm

C. 3000 devices are on a reel.

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