16 V 5 + 1-Channel Operational Amplifier

ADD8706

FEATURES

Single-supply operation: 4.5 V to 16.5 V
Upper/lower buffers swing to V_S/GND
Continuous output current: 35 mA
V_{COM} peak output current: 250 mA
Offset voltage: 15 mV
Slew rate: 6 V/µs
Unity gain stable with large capacitive loads
Supply current: 750 µA per amplifier

APPLICATIONS

TFT LCD monitor panels
TFT LCD notebook panels
Communications equipment
Portable instrumentation
Electronic games
ADC/DAC buffer

GENERAL DESCRIPTION

The ADD8706 is a single-supply, 5-channel buffer with a separate V_{COM} amplifier that has been optimized for today's low cost TFT LCD notebook and monitor panels. The top and bottom channels swing to the top/bottom rails, respectively, and can be used as end-point gamma references. The middle channels are ideal for midpoint gamma references. The V_{COM} amplifier provides very high continuous and peak currents. All channels have excellent transient response as well as high slew rate and capacitive load drive capability. The ADD8706 is specified over the –40°C to +85°C temperature range. The ADD8706 is available in a 16-lead TSSOP package.

Table 1. Input Output Characteristics

Channel	V_{IH}	V_{IL}	I_O (mA)	I_{SC} (mA)
A	V_S	GND + 1.7 V	15	150
B	V_S – 1.7 V	GND	15	150
C	V_S – 1.7 V	GND	15	150
D	V_S – 1.7 V	GND	15	150
E	V_S – 1.7 V	GND	15	150
F	V_S – 1.7 V	GND	35	250

PIN CONFIGURATION

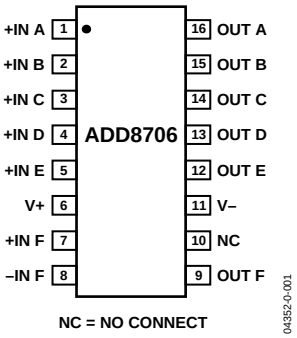

Figure 1. 16-Lead TSSOP

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REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

Table 2. V_S = 16 V, V_{CM} = V_S/2, T_A @ 25 °C, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SUPPLY CHARACTERISTICS						
Supply Voltage	V_S		4.5		16	V
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 17 V, –40°C ≤ T_A ≤ +85°C	70	90		dB
Total Supply Current	I_{SY}	V_O = V_S/2, No Load		4.5	5.4	mA
		–40°C ≤ T_A ≤ +85°C			6	mA
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			2	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +85°C		10		µV/°C
Input Bias Current	I_B			400	1100	nA
		–40°C ≤ T_A ≤ +85°C			1500	nA
Input Offset Current	I_{OS}			10	100	nA
Amplifier F		–40°C ≤ T_A ≤ +85°C			250	nA
Common-Mode Rejection Ratio	CMRR	–40°C ≤ T_A ≤ +85°C				
Amplifier F		V_{CM} = 0 to (V_S – 1.7 V)	54	95		dB
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
OUTPUT CHARACTERISTICS						
Output Voltage High (A)	V_{OH}	V_{IN} = 16 V, I_L = 100 µA		15.99		V
Optimized for High Swing		V_{IN} = 16 V, I_L = 5 mA	15.75	15.85		V
		–40°C ≤ T_A ≤ +85°C	15.65			V
Output Voltage High (B to D)	V_{OH}	V_{IN} = 14 V, I_L = 100 µA		14		V
Optimized for Midrange		V_{IN} = 14 V, I_L = 5 mA	13.90	13.985		V
		–40°C ≤ T_A ≤ +85°C	13.85			V
Output Voltage High (E)	V_{OH}	V_{IN} = 14 V, I_L = 100 µA		14		V
Optimized for Low Swing		V_{IN} = 14 V, I_L = 5 mA	13.9	13.99		V
		–40°C ≤ T_A ≤ +85°C	13.85			V
Output Voltage High (F)	V_{OH}	V_{IN} = 16 V, I_L = 100 µA		15.995		V
Optimized for V_{COM}		V_{IN} = 16 V, I_L = 5 mA	15.8	15.9		V
		–40°C ≤ T_A ≤ +85°C	15.75			V
Output Voltage Low (A)	V_{OL}	V_{IN} = 1.7 V, I_L = 100 µA		1.70		V
Optimized for High Swing		V_{IN} = 1.7 V, I_L = 5 mA		1.71	1.730	V
		–40°C ≤ T_A ≤ +85°C			1.725	V
Output Voltage Low (B–D)	V_{OL}	V_{IN} = 0 V, I_L = 100 µA		5		mV
Optimized for Midrange		V_{IN} = 0 V, I_L = 5 mA		200	300	mV
		–40°C ≤ T_A ≤ +85°C			350	mV
Output Voltage Low (E)	V_{OL}	V_{IN} = 0 V, I_L = 100 µA		5		mV
Optimized for Low Swing		V_{IN} = 0 V, I_L = 5 mA		80	200	mV
		–40°C ≤ T_A ≤ +85°C			300	mV
Output Voltage Low (F)	V_{OL}	V_{IN} = 0 V, I_L = 100 µA		5		mV
Optimized for V_{COM}		V_{IN} = 0 V, I_L = 5 mA		50	150	mV
		–40°C ≤ T_A ≤ +85°C			250	mV
Continuous Output Current (A to E)	I_{OUT}	V_S = 16 V		15		mA
Continuous Output Current (F)	I_{OUT}	V_S = 16 V		35		mA
Peak Output Current (A to E)	I_{PK}	V_S = 16 V		50		mA
Peak Output Current (F)	I_{PK}	V_S = 16 V		200		mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS						
Amplifier Gain	A_{VO}	R_L = 2 kΩ, V_O = 0.5 to (V_S – 2 V)	1	10		V/mV
Buffer Gain	A_{VCL}	R_L = 2 kΩ	0.995	0.9985	1.005	V/V
		–40°C ≤ T_A ≤ +85°C	0.995	0.9980	1.005	V/V
Buffer Gain Linearity	NL	R_L = 2kΩ, V_O = 0.5 to (V_S – 0.5 V)		0.01		%
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, C_L = 200 pF	4	6		V/µs
Bandwidth	BW	–3 dB, R_L = 2 kΩ, C_L = 40 pF		6		MHz
Phase Margin	Øo	R_L = 2 kΩ, C_L = 40 pF		55		Degrees
Channel Separation				75		dB
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		26		nV/√Hz
		f = 10 kHz		25		nV/√Hz
Current Noise Density	i_n	f = 10 kHz		0.8		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3. ADD8706 Stress Ratings*

Parameter	Rating
Supply Voltage (V_S)	18 V
Input Voltage	−0.5 V to V_S + 0.5 V
Differential Input Voltage	V_S
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range	300°C
ESD Tolerance (HBM)	±1500 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

Package Type	θ_{JA}[1]	θ_{JC}	Unit
16-Lead TSSOP (RU)	180	35	°C/W

[1] θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for devices soldered onto a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

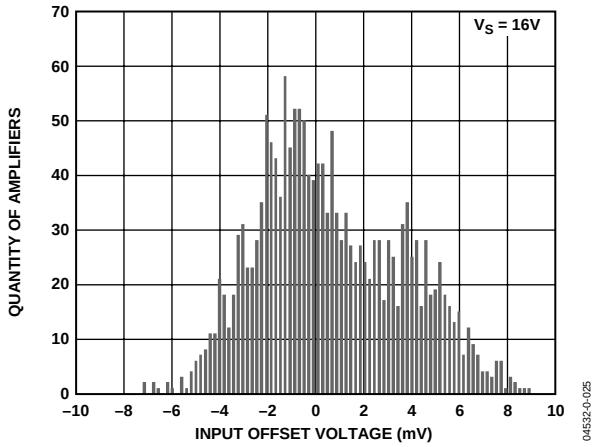

Figure 2. Input Offset Voltage, V_S = 16 V

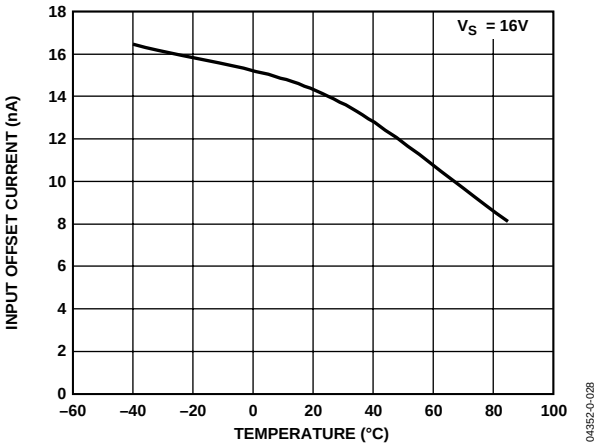

Figure 5. Input Offset Current vs. Temperature

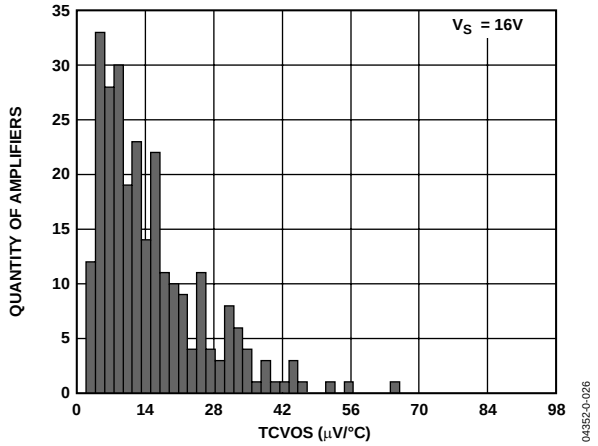

Figure 3. Input Offset Voltage Drift, V_S = 16 V

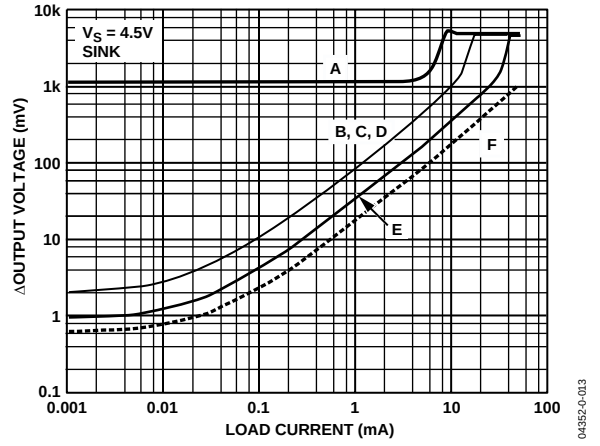

Figure 6. Output Sink Voltage vs. Load Current, All Channels

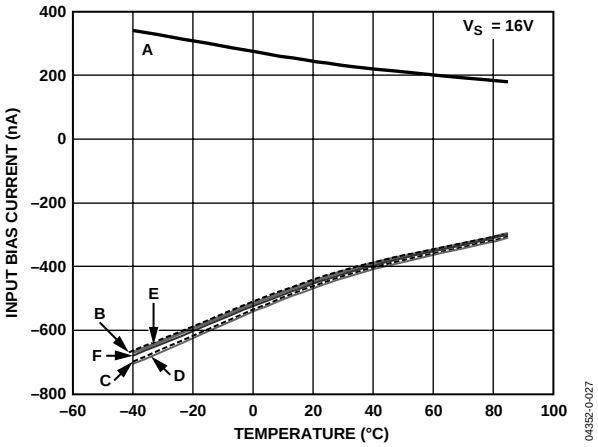

Figure 4. Input Bias Current vs. Temperature

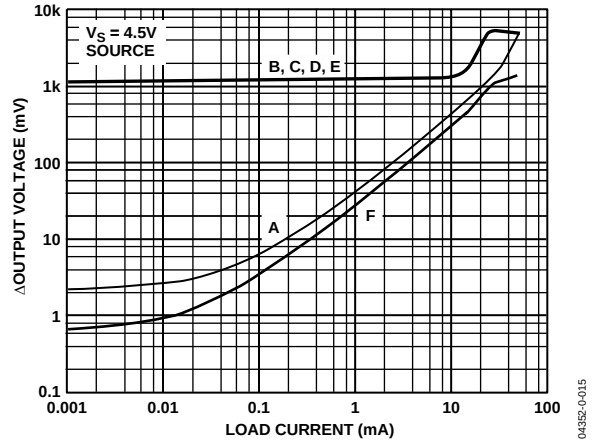

Figure 7. Output Source Voltage vs. Load Current, All Channels

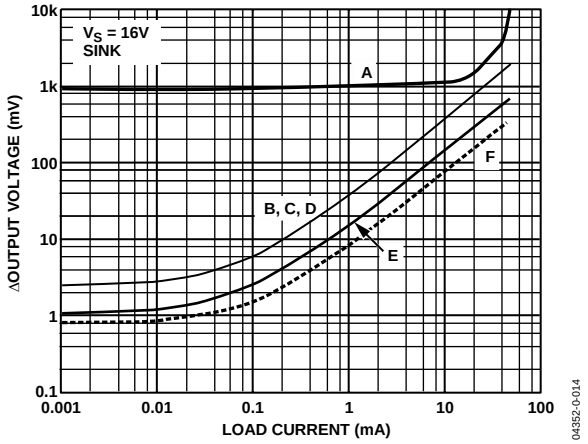

Figure 8. Output Sink Voltage vs. Load Current, All Channels

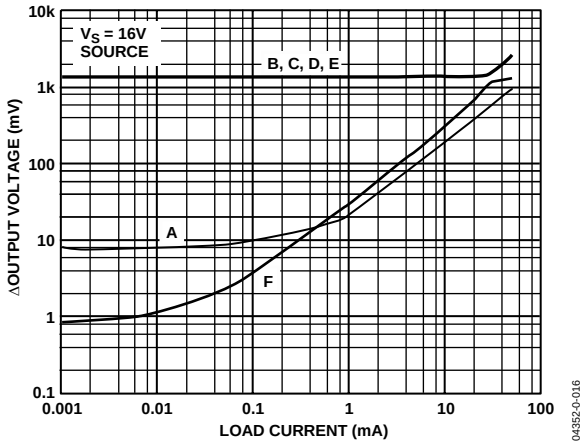

Figure 9. Output Source Voltage vs. Load Current, All Channels

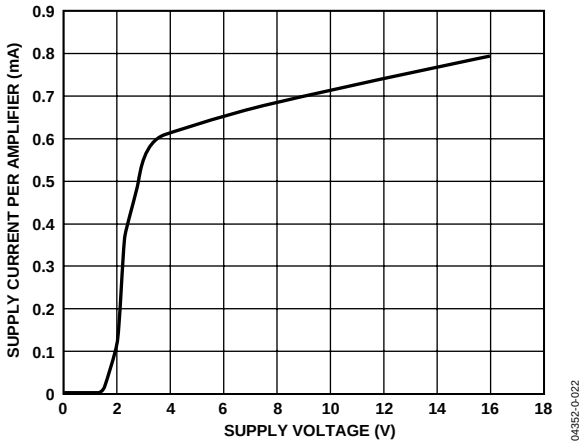

Figure 10. Supply Current vs. Supply Voltage

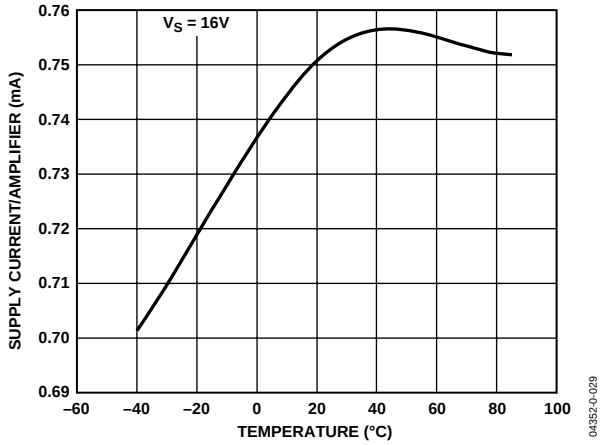

Figure 11. Supply Current vs. Temperature

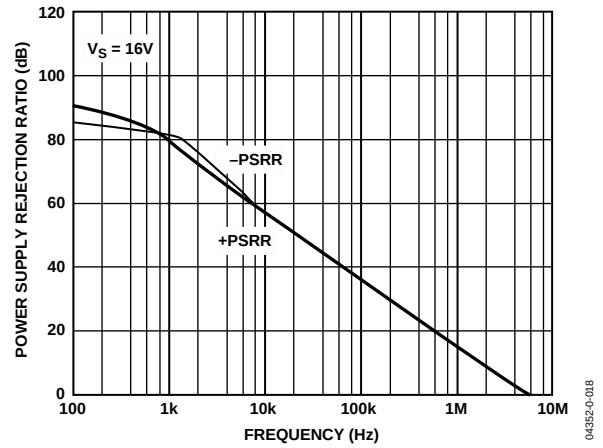

Figure 12. PSRR vs. Frequency

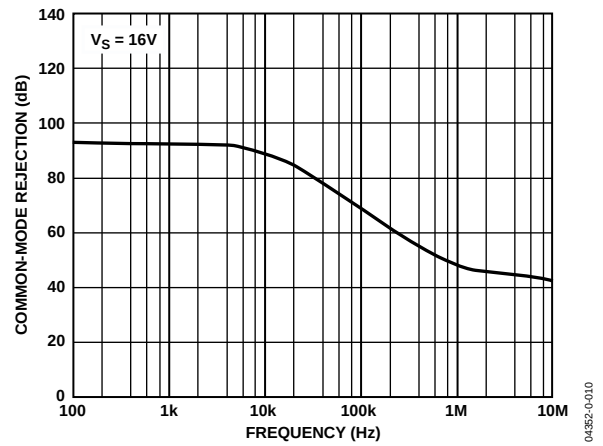

Figure 13. CMRR vs. Frequency

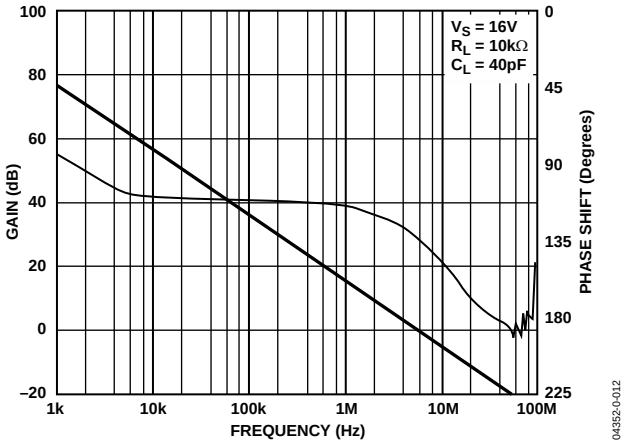

Figure 14. Frequency vs. Gain and Shift

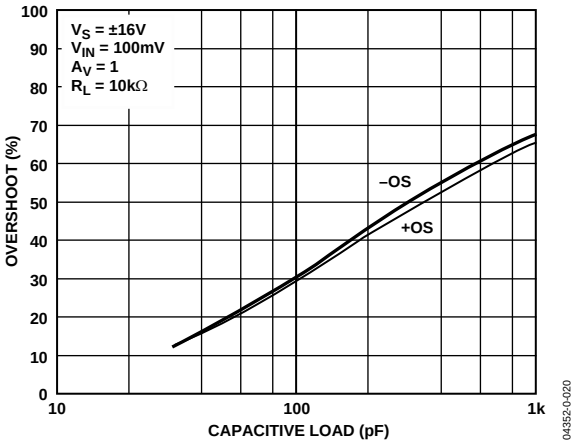

Figure 17. Overshoot vs. Capacitive Load

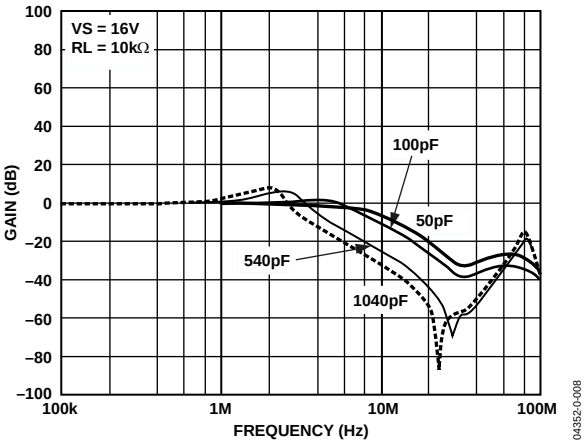

Figure 15. Gain vs. Capacitive Load

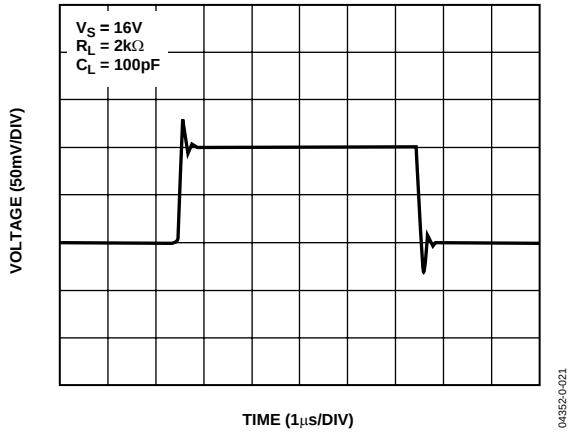

Figure 18. Small-Signal Transient Response

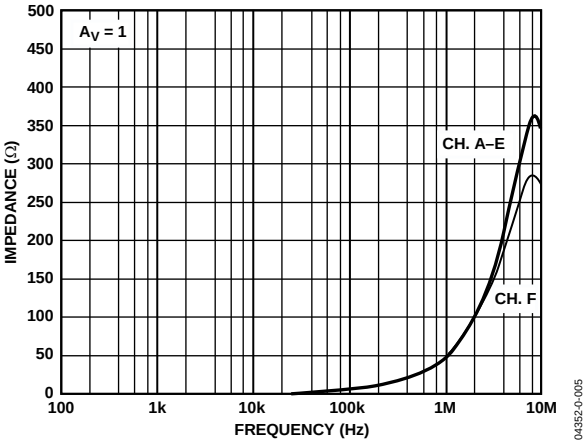

Figure 16. Impedance vs. Frequency

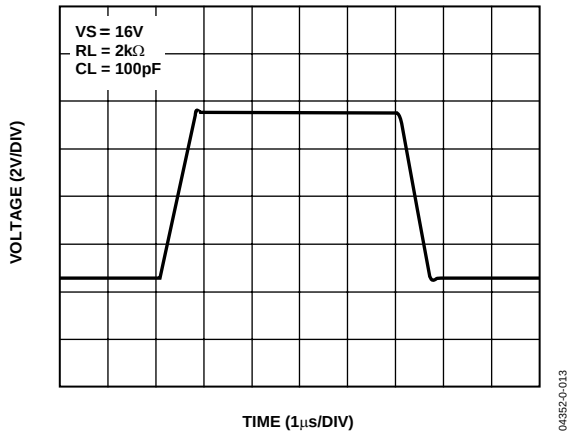

Figure 19. Large Signal Transient Response

APPLICATION INFORMATION

THEORY

The ADD8706 is designed for use in LCD gamma correction circuits. This is an ideal on-chip solution for low-end panels. It provides five gamma voltages and a V_{COM} output. These gamma voltages provide the reference voltages for the column driver RDACs. Due to the capacitive nature of LCD panels, it is necessary for these drivers to provide high capacitive load drive.

The V_{COM} output is the center voltage common to all the LCD pixels. The V_{COM} circuit is common to all the pixels in the panel. This requires the V_{COM} driver to supply continuous currents up to 35 mA.

INPUT/OUTPUT CHARACTERISTICS

The ADD8706 has five buffers specifically designed for the needs of an LCD panel. Figure 20 shows a typical gamma correction curve for a normally white twisted nematic LCD panel. The symmetric curve comes from the need to reverse the polarity on the LC pixels to avoid "burning" in the image. Therefore, the application requires gamma voltages that come close to both supply rails. To accommodate this transfer function, the five ADD8706 buffers have been designed with three different buffer designs in one package.

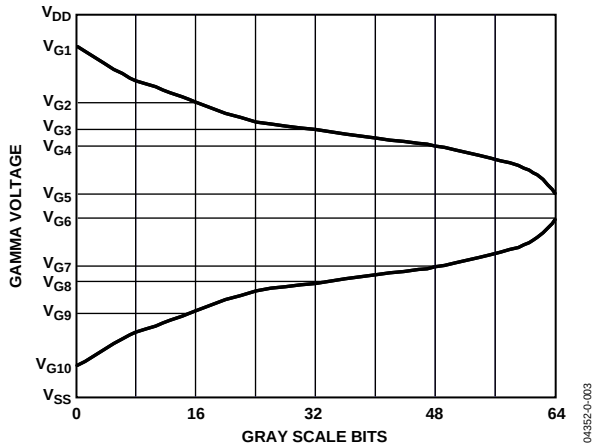

Figure 20. LCD Gamma Correction Curve

The nature of LCD panels introduces a large amount of parasitic capacitance from the column drivers as well as the capacitance associated with the liquid crystals via the common plane. This makes capacitive drive capability an important factor when designing the gamma correction circuit.

The outputs of the buffers and amplifier have been designed to match the performance needs of the gamma correction and V_{COM} circuits. All have rail-to-rail outputs, but the current drive capabilities differ. The difference in current drive and input voltage range determine the buffer and amplifier use.

Buffer A has an NPN emitter-follower input stage, which provides an input range that includes the top rail, but is limited to 1.7 V away from the bottom rail. It is designed to source 15 mA of continuous current, making this buffer ideal for providing the top voltage on the RDAC string.

Buffers B, C, and D use a single-supply PNP input stage with an intermediate common-mode voltage range. The output was designed to sink or source up to 15 mA of continuous current. The limited input range and equivalent sink and source current make these buffers suitable for the middle voltage ranges on the RDAC string.

Buffer E also uses a single-supply PNP input stage, but the output is designed to sink only up to 15 mA of continuous current. This buffer is designed for the RDAC's lower range.

Amplifier F is designed with an input range limited to midscale applications. It is capable of delivering 35 mA of continuous current. These qualities make Amplifier F suitable for V_{COM} applications.

IMPORTANT NOTE

Because of the asymmetric nature of Buffers A and E, care must be taken to connect an input that forces the amplifiers to operate in their most productive output states. Buffer A has very limited sink capabilities, while Buffer E does not source well. Set the Buffer A input to enable the amplifier output to source current and set the Buffer E input to force a sinking output current. This means making sure the input is above the midpoint of the common-mode input range for Buffer A and below the midpoint for Buffer E. Mathematically speaking, make sure $V_{IN} > V_S/2$ for Buffer A and $V_{IN} < V_S/2$ for Buffer E.

Figure 21 shows an application using the ADD8706 to generate 10 gamma outputs. Note that the five outputs are routed through another resistor network to generate the extra five output voltages, which feed into the column driver.

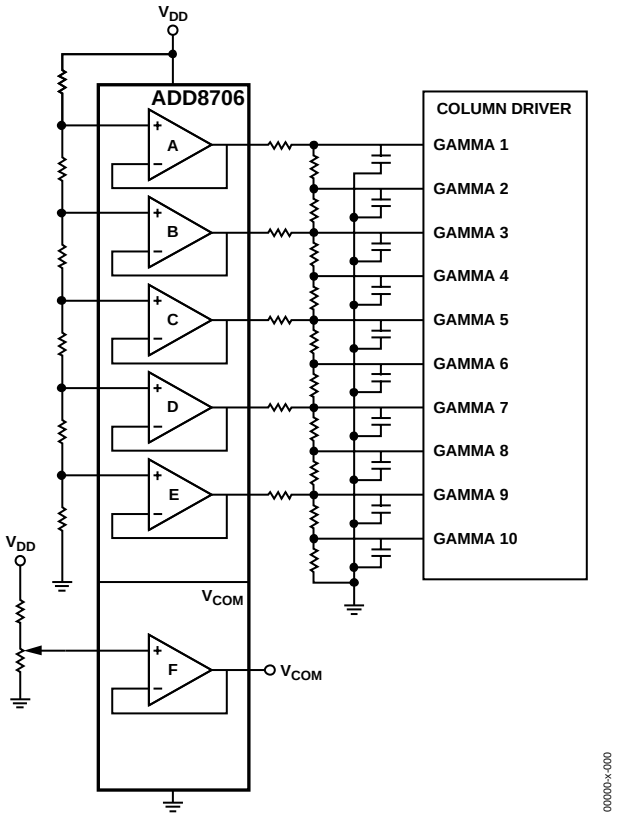

Figure 21. ADD8706 Application Circuit

OUTLINE DIMENSIONS

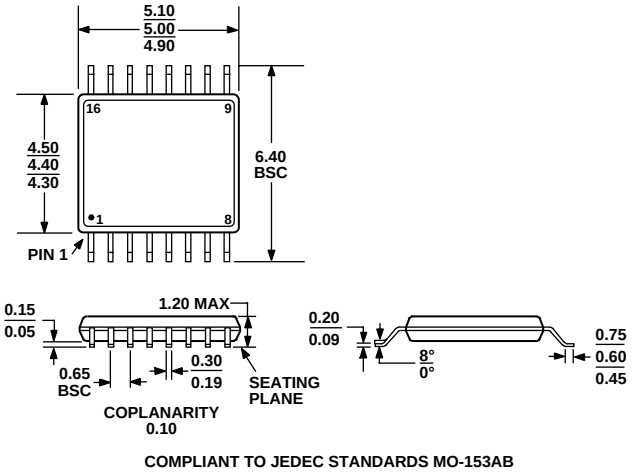

Figure 22. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADD8706ARUZ	−40°C to +85°C	16-Lead TSSOP	RU-16
ADD8706ARUZ-REEL	−40°C to +85°C	16-Lead TSSOP	RU-16

[1] Z = Pb-free part.

NOTES

C04352–0–10/03(0)