ANALOG DEVICES

High Performance, ISM Band, FSK/ASK Transceiver IC

Preliminary Technical Data

ADF7020-1

FEATURES

Low power, low IF transceiver
Frequency bands:
   135 MHz to 650 MHz
Data rates supported
   0.15 kbps to 200 kbps, FSK
   0.15 kbps to 64 kbps, ASK
2.3 V to 3.6 V power supply
Programmable output power
   −16 dBm to +13 dBm in 0.3 dBm steps
Receiver sensitivity
   −119 dBm at 1 kbps, FSK
   −112 dBm at 9.6 kbps, FSK
   −106.5 dBm at 9.6 kbps, ASK
Low power consumption
   18 mA in receive mode
   27 mA in transmit mode (10 dBm output)

On-chip VCO and fractional-N PLL
On-chip 7-bit ADC and temperature sensor
Fully automatic frequency control loop (AFC) compensates
   for lower tolerance crystals
Digital RSSI
Integrated TRx switch
Leakage current <1 µA in power-down mode

APPLICATIONS

Low cost wireless data transfer
Remote control/security systems
Wireless metering
Keyless entry
Home automation
Process and building control
Wireless voice

FUNCTIONAL BLOCK DIAGRAM

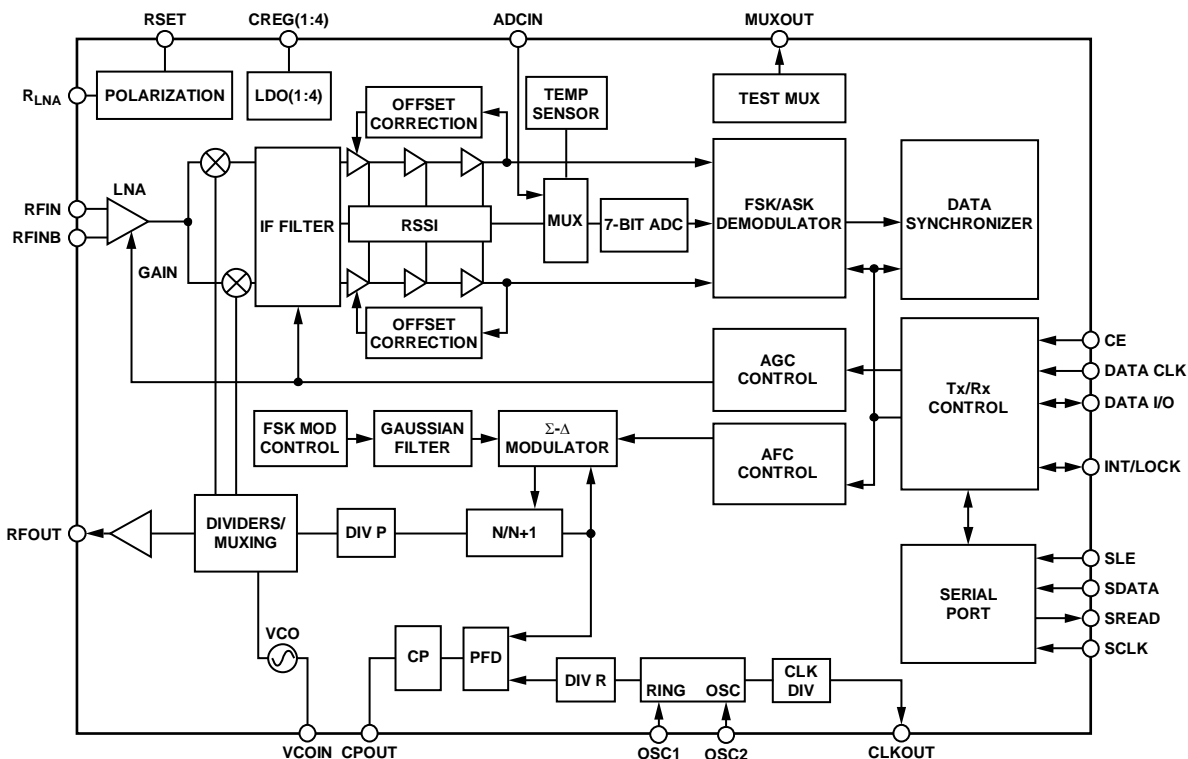*Figure 1.*

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REVISION HISTORY

9/05—PrE: Initial Version

GENERAL DESCRIPTION

The ADF7020-1 is a low power, highly integrated FSK/GFSK/ASK/OOK/GOOK transceiver designed for operation in the low UHF and VHF bands. The ADF7020-1 uses an external VCO inductor which allows you to set the operating frequency anywhere between 135MHz and 650MHz. Typical range of the VCO is about 10% of the operating frequency. A complete transceiver can be built using a small number of external discrete components, making the ADF7020-1 very suitable for price-sensitive and area-sensitive applications.

The transmit section contains a VCO and low noise fractional-N PLL with output resolution of <1 ppm. This frequency agile PLL allows the ADF7020-1 to be used in frequency hopping spread spectrum (FHSS) systems. The VCO operates at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 0.3 dB steps from −16 dBm to +13 dBm. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (200 kHz), minimizing power consumption and the external component count and avoiding interference problems at low frequencies. The ADF7020-1 supports a wide variety of programmable features including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patent-pending automatic frequency control (AFC) loop, allowing the PLL to track out the frequency error in the incoming signal.

An on-chip ADC provides readback of an integrated temperature sensor, an external analog input, the battery voltage, or the RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±10°C over the full operating temperature range of −40°C to +85°C. This accuracy can be improved by doing a 1-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C.
All measurements are performed using the EVAL-ADF7020-1-DBX using PN9 data sequence, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges (Direct Output)	300		650	MHz	VCO adjust = 0, VCO bias = 6
Frequency Ranges (Divide-by-2 Mode)	135		325	MHz	See conditions for Direct Output.
Phase Frequency Detector Frequency	RF/256		20.96	MHz	PFD must be less than Direct Output Frequency/31
TRANSMISSION PARAMETERS					
Data Rate					
FSK/GFSK	0.15		200	kbps	
OOK/ASK	0.15		64[1]	kbps	
OOK/ASK	0.3		100	kbaud	Using Manchester encoding
Frequency Shift Keying					
GFSK/FSK Frequency Deviation[2, 3]	1		110	kHz	PFD = 3.625 MHz
	4.88		620	kHz	PFD = 20 MHz
Deviation Frequency Resolution	100			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Amplitude Shift Keying					
ASK Modulation Depth			30	dB	
OOK–PA Off Feedthrough		−50		dBm	
Transmit Power[4]	−20		+13	dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temp.		±1		dB	From −40°C to +85°C
Transmit Power Variation vs. VDD		±1		dB	From 2.3 V to 3.6 V at 315 MHz, T_A = 25°C
Transmit Power Flatness		TBD		dB	
Programmable Step Size					
−20 dBm to +13 dBm		0.3125		dB	
Integer Boundary		−55		dBc	50 kHz loop BW
Reference		−65		dBc	
Harmonics					
Second Harmonic		−27		dBc	Unfiltered conductive
Third Harmonic		−21		dBc	
All Other Harmonics		−35		dBc	
VCO Frequency Pulling, OOK Mode		30		kHz rms	DR = 9.6 kbps
Optimum PA Load Impedance[5]		TBD		Ω	FRF = 135 MHz
		TBD		Ω	FRF = 315 MHz
		TBD		Ω	FRF = 615 MHz
RECEIVER PARAMETERS					
FSK/GFSK Input Sensitivity					At BER = 1E − 3, FRF = 315 MHz, LNA and PA matched separately[6]
Sensitivity at 1 kbps		−119.2		dBm	FDEV= 5 kHz, high sensitivity mode[7]
Sensitivity at 9.6 kbps		−112.8		dBm	FDEV = 10 kHz, high sensitivity mode
Sensitivity at 200 kbps		−100		dBm	FDEV = 50 kHz, high sensitivity mode
OOK Input Sensitivity					At BER = 1E − 3, FRF = 315 MHz
Sensitivity at 1 kbps		−116		dBm	High sensitivity mode
Sensitivity at 9.6 kbps		−106.5		dBm	High sensitivity mode
LNA and Mixer, Input IP3[7]					
Enhanced Linearity Mode		6.8		dBm	Pin = −20 dBm, 2 CW interferers

Parameter	Min	Typ	Max	Unit	Test Conditions
Low Current Mode		−3.2		dBm	FRF = 315 MHz, F1 = FRF + 3 MHz
High Sensitivity Mode		−35		dBm	F2 = FRF + 6 MHz, maximum gain
Rx Spurious Emissions[8]			−57	dBm	<1 GHz at antenna input
			−47	dBm	>1 GHz at antenna input
AFC					
Pull-In Range		±50		kHz	IF_BW = 200 kHz
Response Time		48		Bits	Mod index = 0.875
Accuracy		1		kHz	
CHANNEL FILTERING					
Adjacent Channel Rejection (Offset = ±1 × IF Filter BW Setting)		27		dB	IF filter BW settings = 100 kHz, 150 kHz, 200 kHz
Second Adjacent Channel Rejection (Offset = ±2 × IF Filter BW Setting)		50		dB	Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until
Third Adjacent Channel Rejection (Offset = ±3 × IF Filter BW Setting)		55		dB	BER = 10^{-3}, image channel excluded
Image Channel Rejection		35		dB	Image at FRF-400 kHz
CO-CHANNEL REJECTION		−2		dB	
Wideband Interference Rejection		70		dB	Swept from 100 MHz to 2 GHz, measured as channel rejection
BLOCKING					Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until BER = 10^{-2}
±1 MHz		60		dB	
±5 MHz		68		dB	
±10 MHz		65		dB	
±10 MHz (High Linearity Mode)		72		dB	
Saturation (Maximum Input Level)		12		dBm	FSK mode, BER = 10^{-3}
LNA Input Impedance		TBD		Ω	FRF = 135 MHz, RFIN to GND
		TBD		Ω	FRF = 315 MHz
		TBD		Ω	FRF = 615 MHz
RSSI					
Range at Input		−100 to −36		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
Response Time		150		μs	See the RSSI/AGC section
PHASE-LOCKED LOOP					
VCO Gain		TBD		MHz/V	315 MHz band, VCO adjust = 0, VCO_BIAS_SETTING = 6
		TBD		MHz/V	135 MHz, VCO adjust = 0
		TBD		MHz/V	433 MHz, VCO adjust = 0
Phase Noise (In-Band)		−89		dBc/Hz	PA = 0 dBm, V_{DD} = 3.0 V, PFD = 10 MHz, FRF = 315 MHz, VCO_BIAS_SETTING = 8
Phase Noise (Out-of-Band)		−110		dBc/Hz	1 MHz offset
Residual FM		128		Hz	From 200 Hz to 20 kHz, FRF = 315 MHz
PLL Settling		40		μs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 20 MHz, LBW = 50 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions
REFERENCE INPUT					
Crystal Reference	3.625		24	MHz	
External Oscillator	3.625		24	MHz	
Load Capacitance		33		pF	See crystal specification sheet
Crystal Start-Up Time		2.1		ms	11.0592 MHz crystal, using 33 pF load capacitors
Crystal Start-Up Time		1.0		ms	Using 16 pF load capacitors
Input Level				CMOS levels	See the Reference Input section
ADC PARAMETERS					
INL		±1		LSB	From 2.3 V to 3.6 V, T_A = 25°C
DNL		±1		LSB	From 2.3 V to 3.6 V, T_A = 25°C
TIMING INFORMATION					
Chip Enabled to Regulator Ready		10		µs	C_{REG} = 100 nF
Chip Enabled to RSSI Ready		3.0		ms	See Table 11 for more details
Tx to Rx Turnaround Time		150 µs + ($5 \times T_{BIT}$)			Time to synchronized data out, includes AGC settling. See AGC Information and Timing section for more details.
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$DV_{DD} - 0.4$			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLK$_{OUT}$ Rise/Fall			5	ns	
CLK$_{OUT}$ Load			10	pF	
TEMPERATURE RANGE—T_A	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply					
V_{DD}	2.3		3.6	V	All V_{DD} pins must be tied together
Transmit Current Consumption					FRF = 315 MHz, V_{DD} = 3.0 V, PA is matched in to 50 Ω
−20 dBm		13.8		mA	
−10 dBm		14.9		mA	VCO_BIAS_SETTING = 6
0 dBm		18.1		mA	
10 dBm		27.5		mA	
Receive Current Consumption					
Low Current Mode		18		mA	
High Sensitivity Mode		20		mA	
Power-Down Mode					
Low Power Sleep Mode		0.1	1	µA	

[1] Higher data rates are achievable depending on local regulations.
[2] For definition of frequency deviation, see the Register 2—Transmit Modulation Register (FSK Mode) section.
[3] For definition of GFSK frequency deviation, see the Register 2—Transmit Modulation Register (GFSK/GOOK Mode) section.
[4] Measured as maximum unmodulated power. Output power varies with both supply and temperature.
[5] For matching details, see the LNA/PA Matching section and the AN-764 application note.
[6] Sensitivity for combined matching network case is typically 2 dB less than separate matching networks.
[7] See Table 5 for a description of different receiver modes.
[8] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING CHARACTERISTICS

$V_{DD} = 3\ V \pm 10\%$, VGND = 0 V, $T_A = 25°C$, unless otherwise noted. Guaranteed by design, but not production tested.

Table 2.

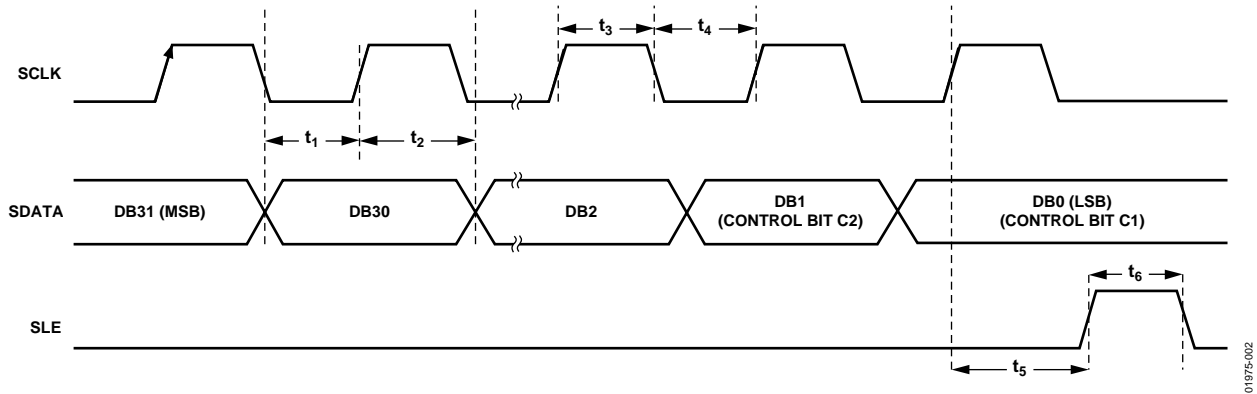| Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	<10	ns	SDATA to SCLK set-up time
t_2	<10	ns	SDATA to SCLK hold time
t_3	<25	ns	SCLK high duration
t_4	<25	ns	SCLK low duration
t_5	<10	ns	SCLK to SLE set-up time
t_6	<20	ns	SLE pulse width
t_8	<25	ns	SCLK to SREAD data valid, readback
t_9	<25	ns	SREAD hold time after SCLK, readback
t_{10}	<10	ns	SCLK to SLE disable time, readback

Figure 2. Serial Interface Timing Diagram
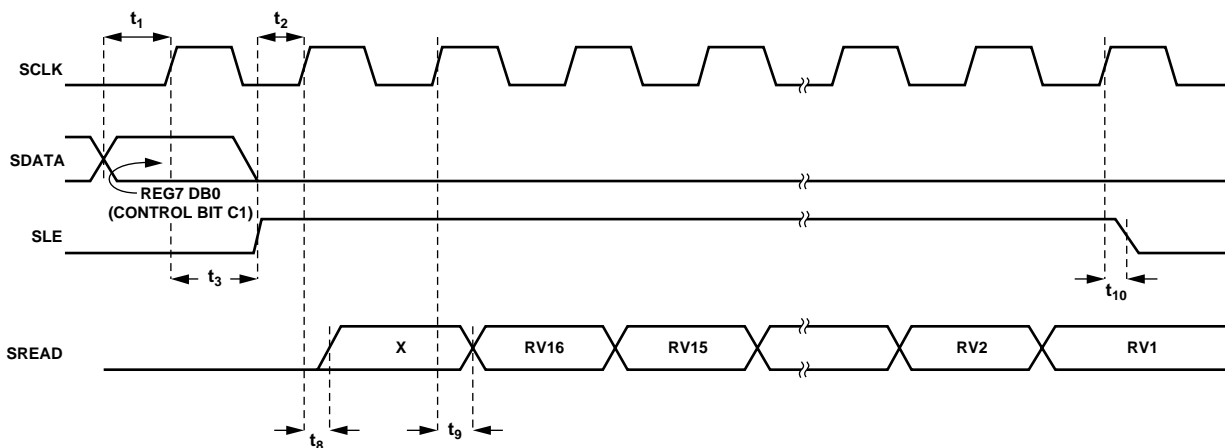

Figure 3. Readback Timing Diagram
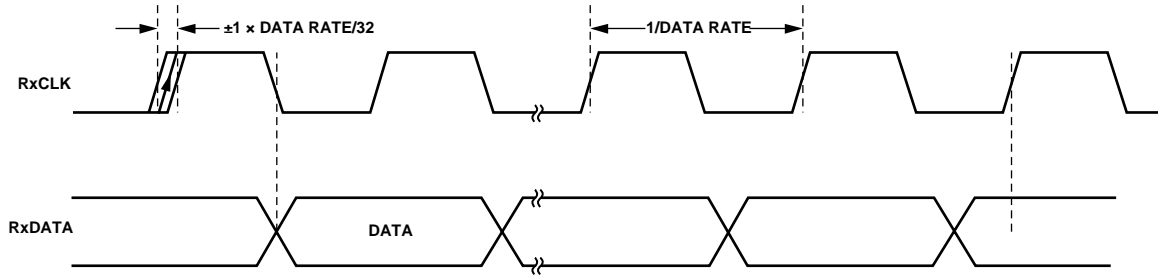
Figure 4. RxData/RxCLK Timing Diagram
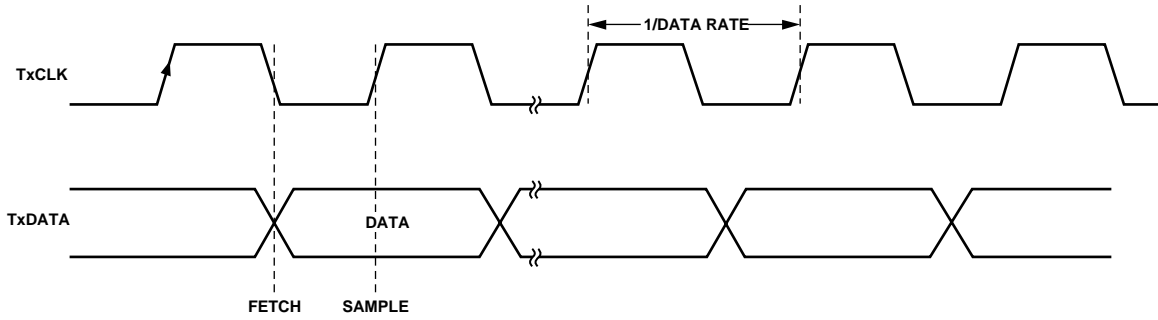
NOTE
1. TxCLK ONLY AVAILABLE IN GFSK MODE.

Figure 5. TxData/TxCLK Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = CPGND = RFGND = DGND = AGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

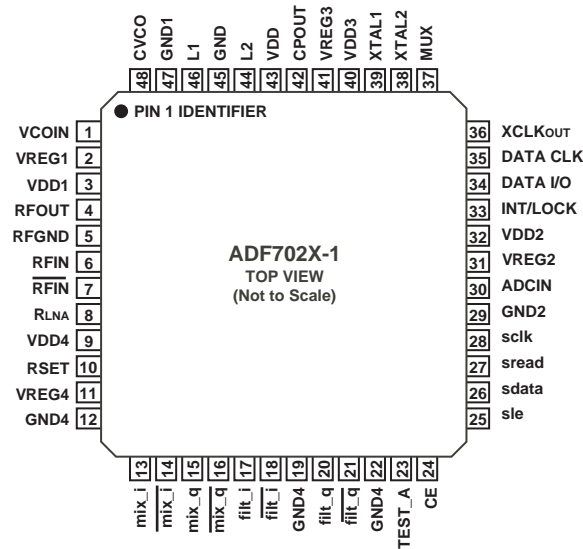| Pin No.	Mnemonic	Function
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	CREG1	Regulator Voltage for PA Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Decoupling capacitors of 0.1 μF and 10 pF should be placed as close as possible to this pin. All VDD pins should be tied together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −20 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components. See the Transmitter section.
5	RFGND	Ground for Output Stage of Transmitter. All GND pins should be tied together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer. See the LNA/PA Matching section.
7	RFINB	Complementary LNA Input. See the LNA/PA Matching section.
8	R_{LNA}	External bias resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/MIXER Block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor to Set Charge Pump Current and Some Internal Bias Currents. Use 3.6 kΩ with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/MIXER Block. A 100 nF capacitor should be placed between this pin and GND for regulator stability and noise rejection.
12	GND4	Ground for LNA/MIXER Block.
13–18	MIX/FILT	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
19, 22	GND4	Ground for LNA/MIXER Block.
20, 21, 23	FILT/TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7020-1 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This pin is a high impedance CMOS input.

Pin No.	Mnemonic	Function
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7020-1 to the microcontroller. The SCLK input is used to clock each readback bit (AFC, ADC readback) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 to 1.9 V. Readback is made using the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. A decoupling capacitor of 10 nF should be placed as close as possible to this pin.
33	INT/LOCK	Bidirectional Pin. In output mode (Interrupt mode), the ADF7020-1 asserts the INT/ LOCK pin when it has found a match for the preamble sequence. In input mode (lock mode), the microcontroller can be used to lock the demodulator threshold when a valid preamble has been detected. Once the threshold is locked, NRZ data can be reliably received. In this mode, a demod lock can be asserted with minimum delay.
34	DATA I/O	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply.
35	DATA CLK	In receive mode, the pin outputs the synchronized data clock. The positive clock edge is matched to the center of the received data. In GFSK transmit mode, the pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. See the Gaussian Frequency Shift Keying (GFSK) section.
36	CLKOUT	A Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio.
37	MUXOUT	This pin provides the Lock_Detect signal, which is used to determine if the PLL is locked to the correct frequency. Other signals include Regulator_Ready, which is an indicator of the status of the serial interface regulator.
38	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the crystal oscillator.
39	OSC1	The reference crystal should be connected between this pin and OSC2.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. This pin should be decoupled to ground with a 0.01 µF capacitor.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. This pin should be decoupled to ground with a 0.01 µF capacitor.
44, 46	L1, L2	External VCO Inductor Pins. A chip inductor should be connected across these pins to set the VCO operating frequency.
45, 47	GND, GND1	Grounds for VCO Block.
48	CVCO	A 22 nF capacitor should be placed between this pin and CREG1 to reduce VCO noise.

TYPICAL PERFORMANCE CHARACTERISTICS

CARRIER POWER –0.28dBm   ATTEN 0.00dB   MKR1   10.0000kHz
REF –70.00dBc/Hz   –87.80dBc/Hz
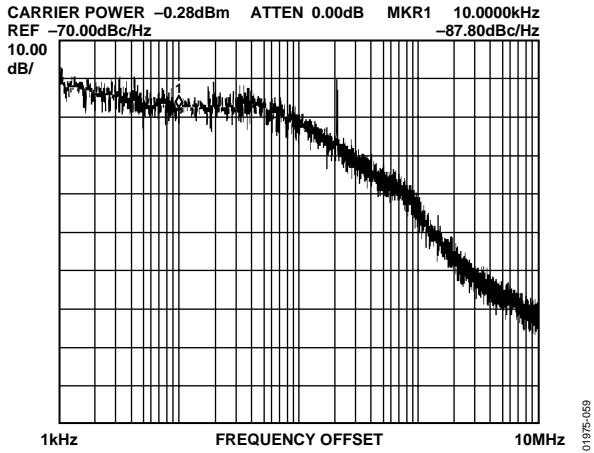
Figure 7. Phase Noise Response at 868.3 MHz, VDD = 3.0 V, ICP = 1.5 mA

MKR4 3.482GHz
REF 10dBm   ATTEN 20dB   SWEEP 16.52ms (601pts)
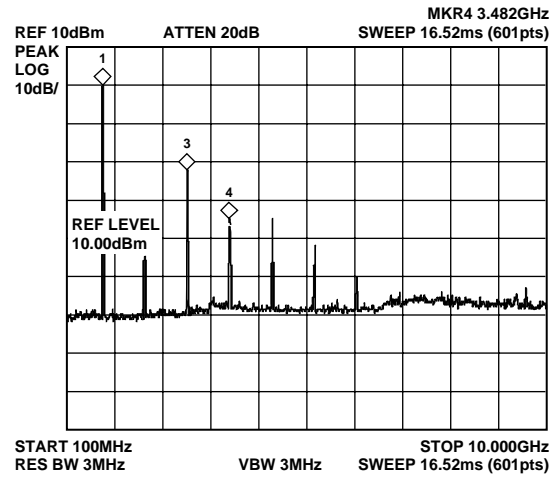
Figure 10. Harmonic Response, RF$_{OUT}$ Matched to 50 Ω, No Filter

TBD
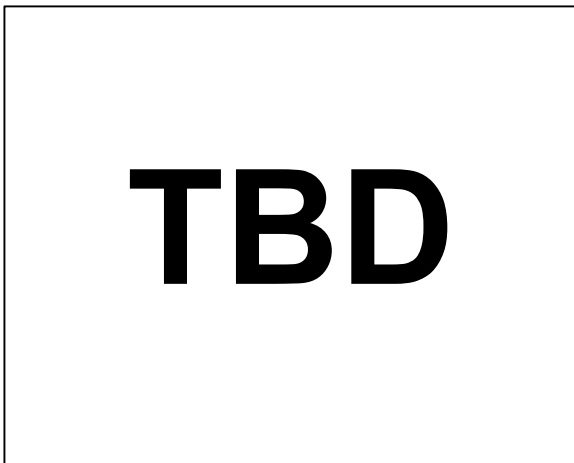
Figure 8. Output Spectrum in FSK and GFSK Modulation

Δ Mkr1 1.834GHz
REF 15dBm   ATTEN 30dB   –62.57dB

MARKER Δ
1.834000000GHz
–62.57dB

START 800MHz   STOP 5.000GHz
#RES BW 30kHz   VBW 30kHz   SWEEP 5.627s (601pts)
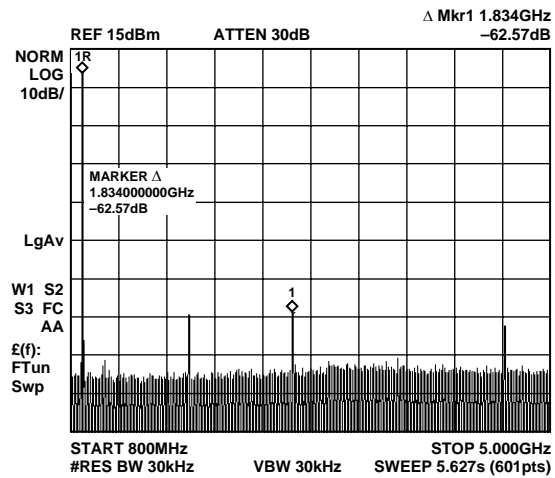
Figure 11. Harmonic Response, Murata Dielectric Filter
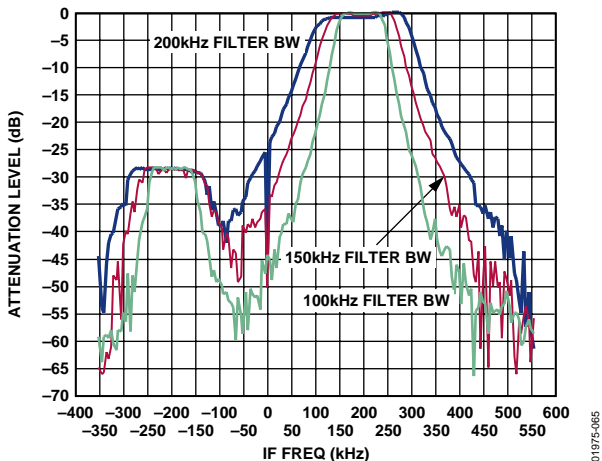
Figure 9. IF Filter Response

TBD
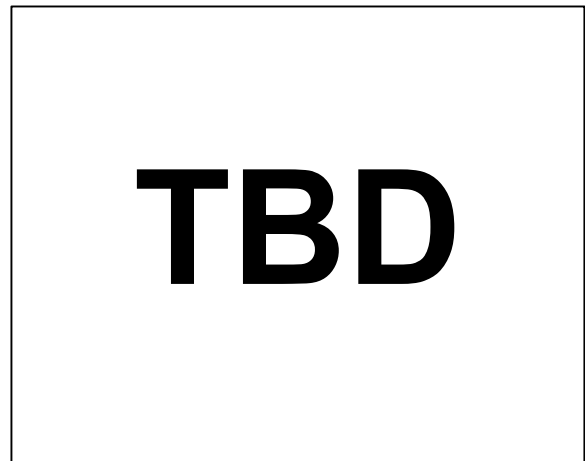
Figure 12. Output Spectrum in ASK, OOK and GOOK Modes, DR = 10 kbps
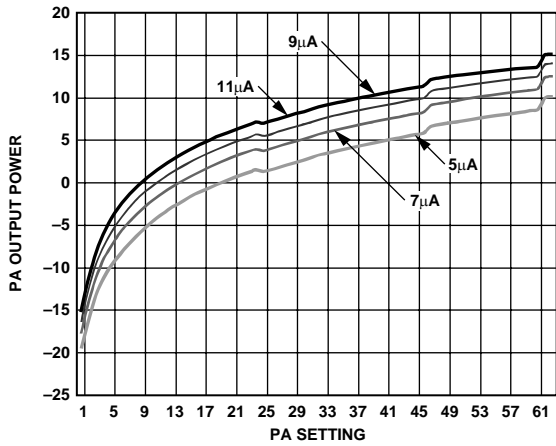
Figure 13. PA Output Power vs. Setting
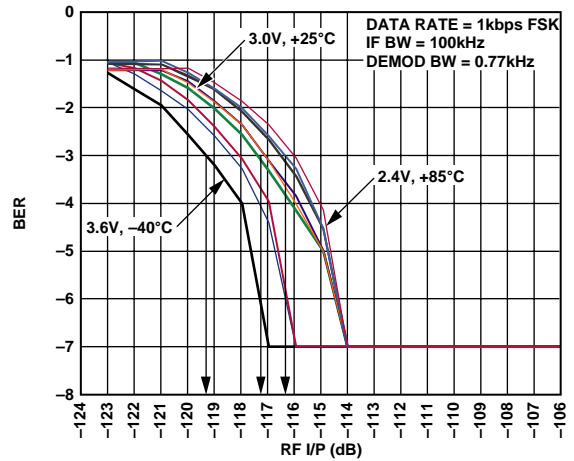
Figure 16. Sensitivity vs. VDD and Temperature
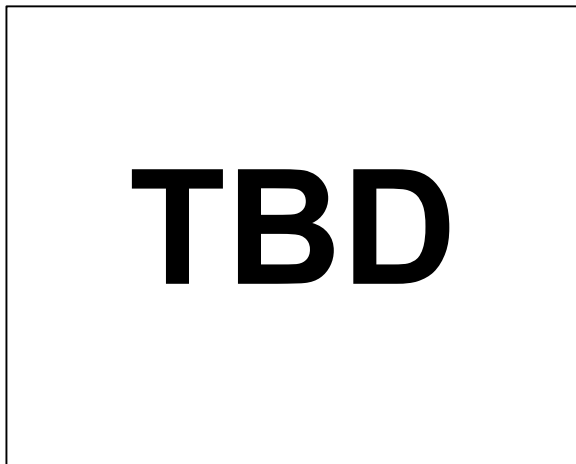
Figure 14. Wideband Interference Rejection. Wanted Signal (880 MHz) at 3 dB above Sensitivity Point Interferer = FM Jammer (9.76 kbps, 10 k Deviation)
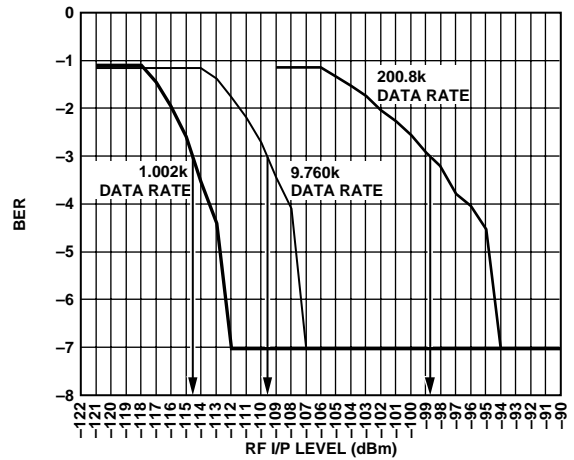
Figure 17. BER vs. Data-Rate (Combined Matching Network) Separate LNA and PA Matching Paths Typically Improve Performance by 2 dB
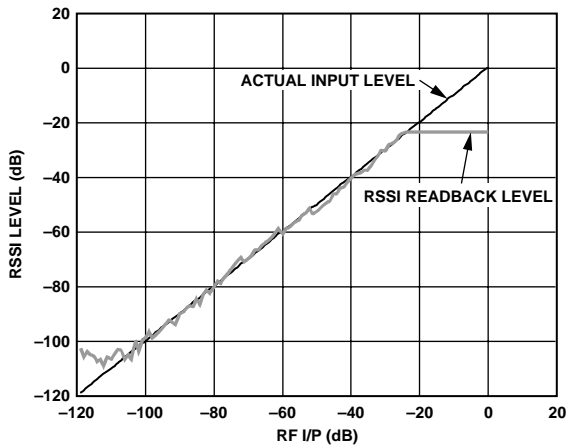
Figure 15. Digital RSSI Readback Linearity
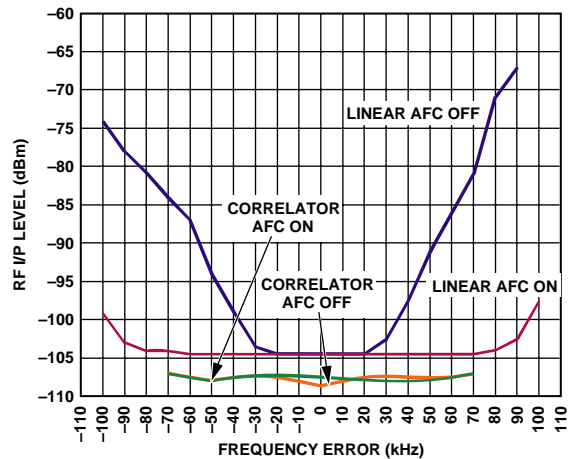
Figure 18. Sensitivity vs. Frequency Error with AFC On/Off

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 19) can use an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected using the automatic frequency control (see the AFC Section) feature or by adjusting the fractional-N value (see the N Counter section). A single-ended reference (TCXO, CXO) can also be used. The CMOS levels should be applied to OSC2 with R1_DB12 set low.
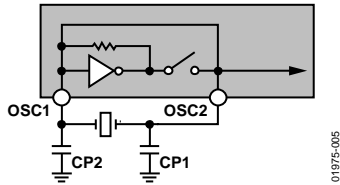
Figure 19. Oscillator Circuit on the ADF7020-1

Two parallel resonant capacitors are required for oscillation at the correct frequency; their values are dependent on the crystal specification. They should be chosen so that the series value of capacitance added to the PCB track capacitance adds up to the load capacitance of the crystal, usually 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. Where possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section (see Figure 19) and supplies a divided-down 50:50 mark-space signal to the CLKOUT pin. An even divide from 2 to 30 is available. This divide number is set in R1_DB (8:11). On power-up, the CLKOUT defaults to divide-by-8.
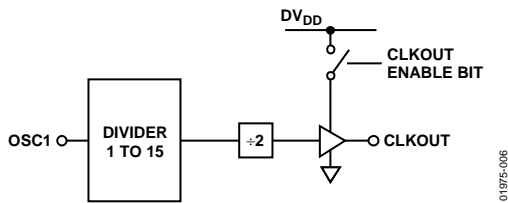
Figure 20. CLK$_{OUT}$ Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at F$_{CLK}$.

R Counter

The 3-bit R counter divides the reference input frequency by an integer from 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in Register 1. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output, as well as reducing occurrences of spurious components. The R Register defaults to R = 1 on power-up:

$$PFD \text{ [Hz]} = XTAL/R$$

MUXOUT and Lock Detect

The MUXOUT pin allows the user to access various digital points in the ADF7020-1. The state of MUXOUT is controlled by Bits R0_DB (29:31).

Regulator Ready

Regulator ready is the default setting on MUXOUT after the transceiver has been powered up. The power-up time of the regulator is typically 50 μs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7020-1 can be programmed. The status of the regulator can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7020-1 can begin.
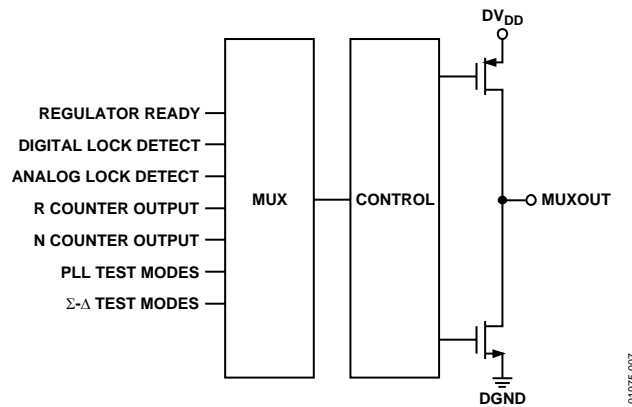
Figure 21. MUXOUT Circuit

Digital Lock Detect

Digital lock detect is active high. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until 25 ns phase error is detected at the PFD. Because no external components are needed for digital lock detect, it is more widely used than analog lock detect.

Analog Lock Detect

This N-channel open-drain lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low-going pulses.

Voltage Regulators

The ADF7020-1 contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Each regulator should have a 100 nF capacitor connected between CREG and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the chip-enable pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates off a regulator supply; therefore, to write to the part, the user must have CE high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the regulator ready signal from muxout.

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 22.
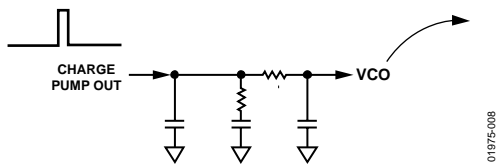
Figure 22. Typical Loop Filter Configuration

In FSK, the loop should be designed so that the loop bandwidth (LBW) is approximately five times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies, but can cause insufficient spurious attenuation.

For ASK systems, a wider LBW is recommended. The sudden large transition between two power levels might result in VCO pulling and can cause a wider output spectrum than is desired. By widening the LBW to more than 10 times the data rate, the amount of VCO pulling is reduced, because the loop settles quickly back to the correct frequency. The wider LBW might restrict the output power and data rate of ASK-based systems compared with FSK-based systems.

Narrow-loop bandwidths can result in the loop taking long periods of time to attain lock. Careful design of the loop filter is critical to obtaining accurate FSK/GFSK modulation.

For GFSK, it is recommended that an LBW of 2.0 to 2.5 times the data rate be used to ensure that sufficient samples are taken of the input data while filtering system noise. The free design tool ADIsimPLL can be used to design loop filters for the ADF7020-1.

N Counter

The feedback divider in the ADF7020-1 PLL consists of an 8-bit integer counter and a 15-bit Σ-Δ fractional-N divider. The integer counter is the standard pulse-swallow type common in PLLs. This sets the minimum integer divide value to 31. The fractional divide value gives very fine resolution at the output, where the output frequency of the PLL is calculated as

$$F_{OUT} = \frac{XTAL}{R} \times (Integer - N + \frac{Fractional - N}{2^{15}})$$
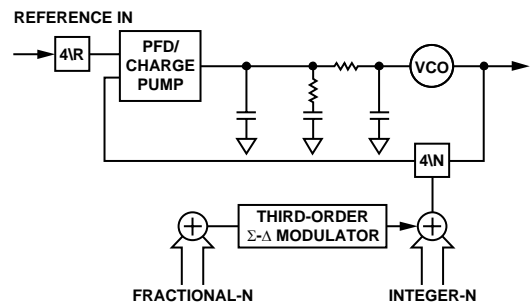
Figure 23. Fractional-N PLL

The combination of the integer-N (maximum = 255) and the fractional-N (maximum = 16383/16384) give a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

PFD_{MIN} [Hz] = *Maximum Required Output Frequency*/(255 + 1)

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz.

Voltage Controlled Oscillator (VCO)

The ADF7020-1 features an on-chip VCO with external tank inductor, which is used to set the frequency range. The center frequency of the VCO is set by the internal varactor capacitance and the combined inductance of the external chip inductor, bondwire and PCB track. A plot of VCO operating range versus total external inductance (chip inductor + PCB track) is shown in Figure 24. The inductance for a PCB track using FR4 material is approximately 0.57nH/mm. This should be subtracted from the total value to give you the correct chip inductor value.

A further frequency divide-by-2 is included to allow operation from 135MHz to 325MHz. To enable the divide-by-2 set R1_DB13 to 1.

The VCO can be recentered, depending on the required frequency of operation, by programming the VCO adjust bits R1_DB (20:21).

The VCO is enabled as part of the PLL by the PLL-enable bit, R0_DB28.

The VCO needs an external 22 nF between the VCO and the regulator to reduce internal noise.

Figure 24.

VCO Bias Current

VCO bias current can be adjusted using Bits R1_DB19 to R1_DB16. To ensure VCO oscillation, the minimum bias current setting under all conditions is 0x8.
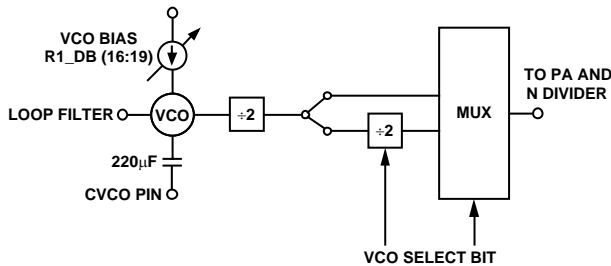
Figure 25. Voltage Controlled Oscillator (VCO)

CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

The fractional-N PLL allows the selection of any channel within 868 MHz to 956 MHz (and 433 MHz using divide-by-2) to a resolution of <300 Hz. This also facilitates frequency hopping systems.

Careful selection of the RF transmit channels must be made to achieve best spurious performance. The architecture of fractional-N results in some level of the nearest integer channel moving through the loop to the RF output. These beat-note spurs are not attenuated by the loop, if the desired RF channel and the nearest integer channel are separated by a frequency of less than the LBW.

The occurrence of beat-note spurs is rare, because the integer frequencies are at multiples of the reference, which is typically >10 MHz.

Beat-note spurs can be significantly reduced in amplitude by avoiding very small or very large values in the fractional register, using the frequency doubler. By having a channel 1 MHz away from an integer frequency, a 100 kHz loop filter can reduce the level to <−45 dBc.

TRANSMITTER

RF OUTPUT STAGE

The PA of the ADF7020-1 is based on a single-ended, controlled current, open-drain amplifier that has been designed to deliver up to 13 dBm into a 50 Ω load at a maximum frequency of 650 MHz.

The PA output current and, consequently, the output power are programmable over a wide range. The PA configurations in FSK/GFSK and ASK/OOK modulation modes are shown in Figure 26 and Figure 27, respectively. In FSK/GFSK modulation mode, the output power is independent of the state of the DATA_IO pin. In ASK/OOK modulation mode, it is dependent on the state of the DATA_IO pin and Bit R2_DB29, which selects the polarity of the TxData input. For each transmission mode, the output power can be adjusted as follows:

- FSK/GFSK: The output power is set using bits R2_DB (9:14).

- ASK: The output power for the inactive state of the TxData input is set by Bits R2_DB (15:20). The output power for the active state of the TxData input is set by Bits R2_DB (9:14).

- OOK: The output power for the active state of the TxData input is set by Bits R2_DB (9:14). The PA is muted when the TxData input is inactive.

The PA is equipped with overvoltage protection, which makes it robust in severe mismatch conditions. Depending on the application, one can design a matching network for the PA to exhibit optimum efficiency at the desired radiated output power level for a wide range of different antennas, such as loop or monopole antennas. See the LNA/PA Matching section for details.

PA Bias Currents

Control Bits R2_DB (30:31) facilitate an adjustment of the PA bias current to further extend the output power control range, if necessary. If this feature is not required, the default value of 7 μA is recommended. The output stage is powered down by resetting Bit R2_DB4. To reduce the level of undesired spurious emissions, the PA can be muted during the PLL lock phase by toggling this bit.

MODULATION SCHEMES

Frequency Shift Keying (FSK)

Frequency shift keying is implemented by setting the N value for the center frequency and then toggling this with the TxData line. The deviation from the center frequency is set using Bits R2_DB(15:23). The deviation from the center frequency in Hz is

$$FSK_{DEVIATION}\ [\text{Hz}] = \frac{PFD \times Modulation\ Number}{2^{14}}$$

where Modulation Number is a number from 1 to 511 (R2_DB (15:23)).

Select FSK using Bits R2_DB (6:8).

Figure 26. PA Configuration in FSK/GFSK Mode
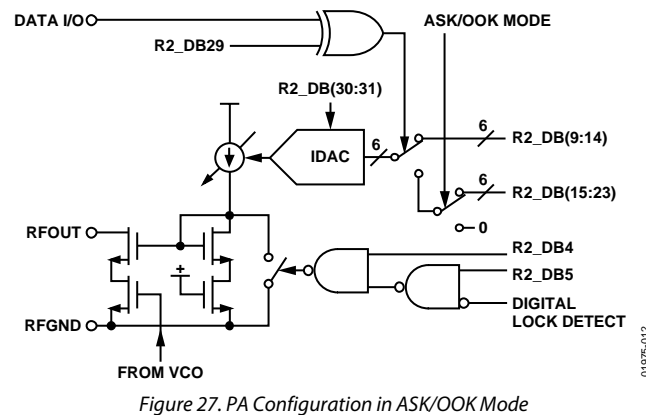
Figure 27. PA Configuration in ASK/OOK Mode
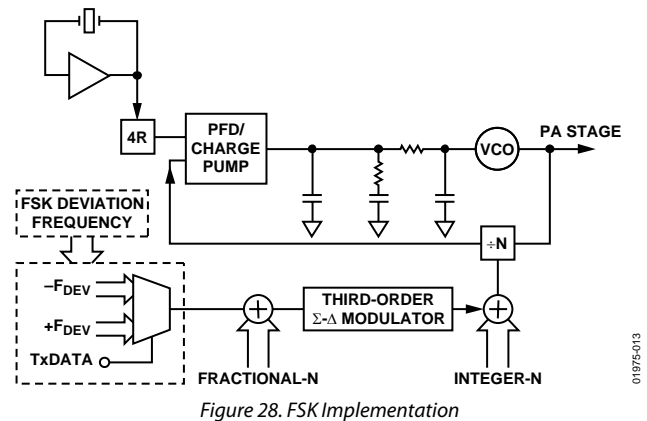
Figure 28. FSK Implementation

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the TxData. A TxCLK output line is provided from the ADF7020-1 for synchronization of TxData from the micro-controller. The TxCLK line can be connected to the clock input of a shift register that clocks data to the transmitter at the exact data rate.

Setting Up the ADF7020-1 for GFSK

To set up the frequency deviation, set the PFD and the mod control bits:

$$GFSK_{DEVIATION} \; [\text{Hz}] = \frac{PFD \times 2^m}{2^{12}}$$

where m is GFSK_MOD_CONTROL set using R2_DB (24:26).

To set up the GFSK data rate:

$$DR[\text{bps}] = \frac{PFD}{DIVIDER\_FACTOR \times INDEX\_COUNTER}$$

For further information, see the application note, Using GFSK on the ADF7010, in the EVAL-ADF7010EB1 Technical Note.

Amplitude Shift Keying (ASK)

Amplitude shift keying is implemented by switching the output stage between two discrete power levels. This is accomplished by toggling the DAC, which controls the output level between two 6-bit values set up in Register 2. A 0 TxData bit sends Bits R2_DB (15:20) to the DAC. A high TxData bit sends Bits R2_DB (9:14) to the DAC. A maximum modulation depth of 30 dB is possible.

On-Off Keying (OOK)

On-off keying is implemented by switching the output stage to a certain power level for a high TxData bit and switching the output stage off for a zero. For OOK, the transmitted power for a high input is programmed using Bits R2_DB (9:14).

Gaussian On-Off Keying (GOOK)

Gaussian on-off keying represents a prefiltered form of OOK modulation. The usually sharp symbol transitions are replaced with smooth Gaussian filtered transitions, the result being a reduction in frequency pulling of the VCO. Frequency pulling of the VCO in OOK mode can lead to a wider than desired BW, especially if it is not possible to increase the loop filter BW > 300 kHz. The GOOK sampling clock samples data at the data rate. (See the Setting Up the ADF7020-1 for GFSK section.)

RECEIVER SECTION

RF FRONT END

The ADF7020-1 is based on a fully integrated, low IF receiver architecture. The low IF architecture facilitates a very low external component count and does not suffer from power-line-induced interference problems.

Figure 29 shows the structure of the receiver front end. The many programming options allow users to trade off sensitivity, linearity, and current consumption against each other in the way best suitable for their applications. To achieve a high level of resilience against spurious reception, the LNA features a differential input. Switch SW2 shorts the LNA input when transmit mode is selected (R0_DB27 = 0). This feature facilitates the design of a combined LNA/PA matching network, avoiding the need for an external Rx/Tx switch. See the LNA/PA Matching section for details on the design of the matching network.
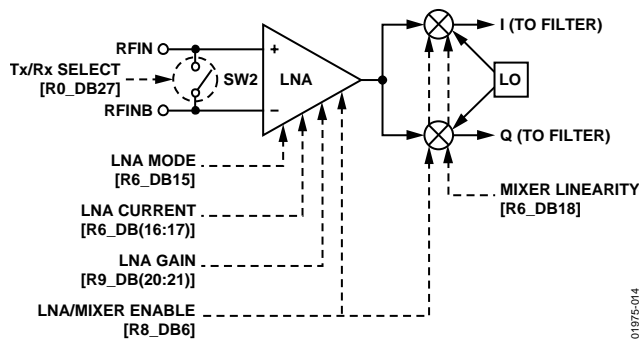
Figure 29. ADF7020-1 RF Front End

The LNA is followed by a quadrature down conversion mixer, which converts the RF signal to the IF frequency of 200 kHz. It is important to consider that the output frequency of the synthesizer must be programmed to a value 200 kHz below the center frequency of the received channel.

The LNA has two basic operating modes: high gain/low noise mode and low gain/low power mode. To switch between these two modes, use the LNA_mode bit, R6_DB15. The mixer is also configurable between a low current and an enhanced linearity mode using the mixer_linearity bit, R6_DB18.

Based on the specific sensitivity and linearity requirements of the application, it is recommended to adjust control bits LNA_mode (R6_DB15) and mixer_linearity (R6_DB18) as outlined in Table 5.

The gain of the LNA is configured by the LNA_gain field, R9_DB (20:21), and can be set by either the user or the automatic gain control (AGC) logic.

IF Filter Settings/Calibration

Out-of-band interference is rejected by means of a fourth-order Butterworth polyphase IF filter centered around a frequency of 200 kHz. The bandwidth of the IF filter can be programmed between 100 kHz and 200 kHz by means of Control Bits R1_DB (22:23), and should be chosen as a compromise between interference rejection, attenuation of the desired signal, and the AFC pull-in range.

To compensate for manufacturing tolerances, the IF filter should be calibrated once after power-up. The IF filter calibration logic requires that the IF filter divider in Bits R6_DB (20:28) be set dependent on the crystal frequency. Once initiated by setting Bit R6_DB19, the calibration is performed automatically without any user intervention. The calibration time is 200 μs, during which the ADF7020-1 should not be accessed. It is important not to initiate the calibration cycle before the crystal oscillator has fully settled. If the AGC loop is disabled, the gain of IF filter can be set to three levels using the filter_gain field, R9_DB (20:21). The filter gain is adjusted automatically, if the AGC loop is enabled.

Table 5. LNA/Mixer Modes

Receiver Mode	LNA Mode (R6_DB15)	LNA Gain Value R9_DB (21:20)	Mixer Linearity (R6_DB18)	Sensitivity (DR = 9.6 kbps, f_{DEV} = 10 kHz)	Rx Current Consumption (mA)	Input IP3 (dBm)
High Sensitivity Mode (default)	0	30	0	−110.5	21	−35
RxMode2	1	10	0	−104	20	−15.9
Low Current Mode	1	3	0	−91	19	−3.2
Enhanced Linearity Mode	1	3	1	−101	19	+6.8
RxMode5	1	10	1	−98	20	−8.25
RxMode6	0	30	1	−105	21	−28.8

RSSI/AGC

The RSSI is implemented as a successive compression log amp following the base-band channel filtering. The log amp achieves ±3 dB log linearity. It also doubles as a limiter to convert the signal-to-digital levels for the FSK demodulator. The RSSI itself is used for amplitude shift keying (ASK) demodulation. In ASK mode, extra digital filtering is performed on the RSSI value. Offset correction is achieved using a switched capacitor integrator in feedback around the log amp. This uses the BB offset clock divide. The RSSI level is converted for user readback and digitally controlled AGC by an 80-level (7-bit) flash ADC. This level can be converted to input power in dBm.
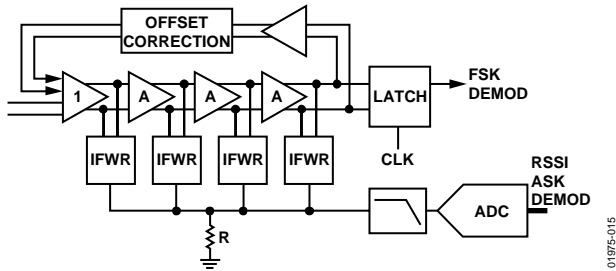
Figure 30. RSSI Block Diagram

RSSI Thresholds

When the RSSI is above AGC_HIGH_THRESHOLD, the gain is reduced. When the RSSI is below AGC_LOW_THRESHOLD, the gain is increased. A delay (AGC_DELAY) is programmed to allow for settling of the loop. The user programs the two threshold values (recommended defaults, 30 and 70) and the delay (default, 10). The default AGC setup values should be adequate for most applications. The threshold values must be chosen to be more than 30 apart for the AGC to operate correctly.

Offset Correction Clock

In Register 3, the user should set the BB offset clock divide bits R3_DB(4:5) to give an offset clock between 1 MHz and 2 MHz, where:

$$BBOS\_CLK \text{ (Hz)} = XTAL/(BBOS\_CLK\_DIVIDE)$$

BBOS_CLK_DIVIDE can be set to 4, 8, or 16.

AGC Information and Timing

AGC is selected by default, and operates by selecting the appropriate LNA and filter gain settings for the measured RSSI level. It is possible to disable AGC by writing to Register 9 if you want to enter one of the modes listed in Table 5, for example. The time for the AGC circuit to settle and hence the time it takes to take an accurate RSSI measurement is typically 150 μs although this depends on how many gain settings the AGC circuit has to cycle through. After each gain change the AGC loop waits for a programmed time to allow transients to settle. This wait time can be adjusted to speed up this settling by adjusting the appropriate parameters.

$$AGC\_Wait\_Time = \frac{AGC\_DELAY \times SEQ\_CLK\_DIVIDE}{XTAL}$$

$$AGC\ Settling = AGC\_Wait\_Time \times Number\ of\ Gain\ Changes$$

Thus, in the worst case, if the AGC loop has to go through all 5 gain changes, AGC delay =10, SEQ_CLK = 200 kHz, then AGC settling = 10 × 5 μs × 5 = 250 μs. Minimum AGC_Wait_Time needs to be at least 25 μs.

RSSI Formula (Converting to dBm)

Input_Power [dBm] = −115 dBm + (Readback_Code + Gain_Mode_Correction) × 0.5

where:
Readback_Code is given by Bits RV7 to RV1 in the readback register (see Readback Format section).
Gain_Mode_Correction is given by the values in Table 6. LNA gain and filter gain (LG2/LG1, FG2/FG1) are also obtained from the readback register.

Table 6. Gain Mode Correction

LNA Gain (LG2, LG1)	Filter Gain (FG2, FG1)	Gain Mode Correction
H (1,1)	H (1,0)	0
M (1,0)	H (1,0)	24
M (1,0)	M (0,1)	45
M (1,0)	L (0,0)	61
L (0,1)	L (0,0)	85
EL (0,0)	L (0,0)	103

An additional factor should be introduced to account for losses in the front end matching network/antenna.

FSK DEMODULATORS ON THE ADF7020-1

The two FSK demodulators on the ADF7020-1 are

- FSK correlator/demodulator

- Linear demodulator

Select these using the demodulator select bits, R4_DB (4:5).

FSK CORRELATOR/DEMODULATOR

The quadrature outputs of the IF filter are first limited and then fed to a pair of digital frequency correlators that perform band-pass filtering of the binary FSK frequencies at (IF + F_{DEV}) and (IF − F_{DEV}). Data is recovered by comparing the output levels from each of the two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of AWGN.
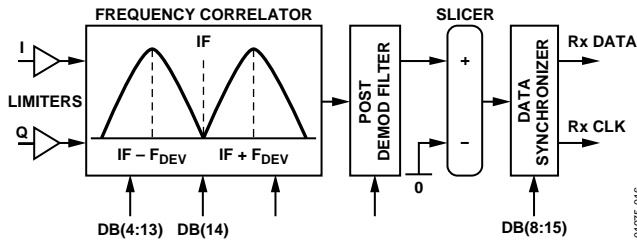
Figure 31. FSK Correlator/Demodulator Block Diagram

Postdemodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this postdemodulator filter is programmable and must be optimized for the user's data rate. If the bandwidth is set too narrow, performance is degraded due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the receiver's performance. Typically, the 3 dB bandwidth of this filter is set at approximately 0.75 times the user's data rate, using Bits R4_DB (6:15).

Bit Slicer

The received data is recovered by threshold detecting the output of the postdemodulator low-pass filter. In the correlator/demodulator, the binary output signal levels of the frequency discriminator are always centered on zero. Therefore, the slicer threshold level can be fixed at zero and the demodulator performance is independent of the run-length constraints of the transmit data bit stream. This results in robust data recovery, which does not suffer from the classic baseline wander problems that exist in the more traditional FSK demodulators.

Frequency errors are removed by an internal AFC loop that measures the average IF frequency at the limiter output and applies a frequency correction value to the fractional-N synthesizer. This loop should be activated when the frequency errors are greater than approximately 40% of the transmit frequency deviation (see the AFC Section).

Data Synchronizer

An oversampled digital PLL is used to resynchronize the received bit stream to a local clock. The oversampled clock rate of the PLL (CDR_CLK) must be set at 32 times the data rate. See the notes for the Register 3—Receiver Clock Register section for a definition of how to program. The clock recovery PLL can accommodate frequency errors of up to ±2%.

FSK Correlator Register Settings

To enable the FSK correlator/demodulator, Bits R4_DB (5:4) should be set to [01]. To achieve best performance, the bandwidth of the FSK correlator must be optimized for the specific deviation frequency that is used by the FSK transmitter.

The discriminator BW is controlled in Register 6 by R6_DB (4:13) and is defined as

$$Discriminator \_ BW = (DEMOD \_ CLK \times K)/(800 \times 10^3)$$

where:
$DEMOD\_CLK$ is as defined in the Register 3—Receiver Clock Register section, Note 2.
K = Round(200e3/FSK Deviation)

To optimize the coefficients of the FSK correlator, two additional bits, R6_DB14 and R6_DB29, must be assigned. The value of these bits depends on whether K (as defined above) is odd or even. These bits are assigned according to Table 7 and Table 8.

Table 7. When K Is Even

K	K/2	R6_DB14	R6_DB29
Even	Even	0	0
Even	Odd	0	1

Table 8. When K Is Odd

K	(K + 1)/2	R6_DB14	R6_DB29
Odd	Even	1	0
Odd	Odd	1	1

Postdemodulator Bandwidth Register Settings

The 3 dB bandwidth of the postdemodulator filter is controlled by Bits R4_ DB (6:15) and is given by

$$Post \_ De \bmod\_ BW \_ Setting = \frac{2^{10} \times 2\pi \times F_{CUTOFF}}{DEMOD \_ CLK}$$

where F_{CUTOFF} is the target 3 dB bandwidth in Hz of the post-demodulator filter. This should typically be set to 0.75 times the data rate (DR).

Some sample settings for the FSK correlator/demodulator are

$DEMOD\_CLK$ = 5 MHz
DR = 9.6 kbps
F_{DEV} = 20 kHz

Therefore

F_{CUTOFF} = 0.75 × 9.6 × 10^3 Hz
$Post\_Demod\_BW$ = 2^{11} π 7.2 × 10^3 Hz/(5 MHz)
$Post\_Demod\_BW$ = Round(9.26) = 9

and

K = Round(200 kHz)/20 kHz) = 10
$Discriminator\_BW$ = (5 MHz × 10)/(800 × 10^3) = 62.5 = 63 (rounded to nearest integer)

Table 9. Register Settings

Setting Name	Register Address	Value
Post_Demod_BW	R4_DB (6:15)	0x09
Discriminator BW	R6_DB (4:13)	0x3F
Dot Product	R6_DB14	0
Rx Data Invert	R6_DB29	1

LINEAR FSK DEMODULATOR

Figure 32 shows a block diagram of the linear FSK demodulator.
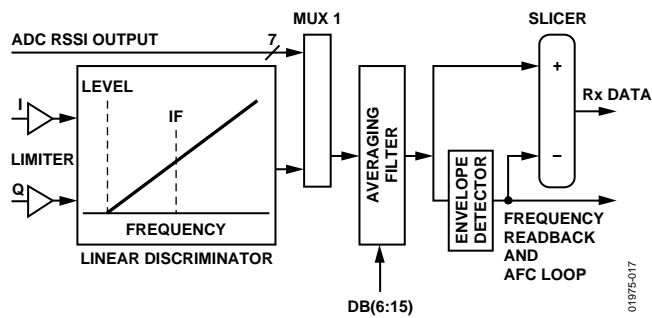
Figure 32. Block Diagram of Frequency Measurement System and ASK.OOK/Linear FSK Demodulator

This method of frequency demodulation is useful when very short preamble length is required and the system protocol cannot support the overhead of the settling time of the internal feedback AFC loop settling.

A digital frequency discriminator provides an output signal that is linearly proportional to the frequency of the limiter outputs. The discriminator output is then filtered and averaged using a combined averaging filter and envelope detector. The demodulated FSK data is recovered by threshold-detecting the output of the averaging filter, as shown in Figure 32. In this mode, the slicer output shown in Figure 32 is routed to the data synchronizer PLL for clock synchronization. To enable the linear FSK demodulator, set Bits R4_DB (4:5) to [00].

The 3 dB bandwidth of the postdemodulation filter is set in the same way as the FSK correlator/demodulator, which is set in R4_DB (6:15) and is defined as

$$Post\_Demod\_BW\_Setting = \frac{2^{10} \times 2\pi \times F_{CUTOFF}}{DEMOD\_CLK}$$

where:
F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter. DEMOD_CLK is as defined in the Register 3—Receiver Clock Register section, Note 2.

ASK/OOK Operation

ASK/OOK demodulation is activated by setting Bits R4_DB (4:5) to [10].

Digital filtering and envelope detecting the digitized RSSI input via MUX 1, as shown in Figure 32, performs ASK/OOK demodulation. The bandwidth of the digital filter must be optimized to remove any excess noise without causing ISI in the received ASK/OOK signal.

The 3 dB bandwidth of this filter is typically set at approximately 0.75 times the user data rate and is assigned by R4 _DB (6:15) as

$$Post\_Demod\_BW\_Setting = \frac{2^{10} \times 2\pi \times F_{CUTOFF}}{DEMOD\_CLK}$$

where F_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter.

It is also recommended to adjust the peak response factor to 6 in Register 10 for robust operation over the full input range. This also improves the receiver's AM immunity performance.

AFC SECTION

The ADF7020-1 supports a real-time AFC loop, which is used to remove frequency errors that can arise due to mismatches between the transmit and receive crystals. This uses the frequency discrim-inator block, as described in the Linear FSK Demodulator section (see Figure 32). The discriminator output is filtered and averaged to remove the FSK frequency modulation using a combined averaging filter and envelope detector. In FSK mode, the output of the envelope detector provides an estimate of the average IF frequency.

Two methods of AFC, external and internal, are supported on the ADF7020-1 (in FSK mode only).

External AFC

The user reads back the frequency information through the ADF7020-1 serial port and applies a frequency correction value to the fractional-N synthesizer's N divider.

The frequency information is obtained by reading the 16-bit signed AFC_readback, as described in the Readback Format section, and applying the following formula:

$$FREQ\_RB \text{ [Hz]} = (AFC\_READBACK \times DEMOD\_CLK)/2^{15}$$

Note that while the AFC_READBACK value is a signed number, under normal operating conditions it is positive. In the absence of frequency errors, the FREQ_RB value is equal to the IF frequency of 200 kHz.

Internal AFC

The ADF7020-1 supports a real-time internal automatic frequency control loop. In this mode, an internal control loop automatically monitors the frequency error and adjusts the synthesizer N divider using an internal PI control loop.

The internal AFC control loop parameters are controlled in Register 11. The internal AFC loop is activated by setting R11_DB20 to 1. A scaling coefficient must also be entered, based on the crystal frequency in use. This is set up in R11_DB (4:19) and should be calculated using

$$AFC\_Scaling\_Coefficient = (500 \times 2^{24})/XTAL$$

Therefore, using a 10 MHz XTAL yields an AFC scaling coefficient of 839.

Maximum AFC Range

The maximum AFC frequency range is ±100 kHz. This is set by the maximum IF filter bandwidth of 200 kHz. Using the minimum IF filter bandwidth of 100 kHz, the AFC range is ±50 kHz.

When AFC errors have been removed using either the internal or external AFC, further improvement in the receiver's sensitivity can be obtained by reducing the IF filter bandwidth using Bits R1_DB (22:23).

AUTOMATIC SYNC WORD RECOGNITION

The ADF7020-1 also supports automatic detection of the sync or ID fields. To activate this mode, the sync (or ID) word must be preprogrammed into the ADF7020-1. In receive mode, this preprogrammed word is compared to the received bit stream and, when a valid match is identified, the external pin INT/LOCK is asserted by the ADF7020-1.

This feature can be used to alert the microprocessor that a valid channel has been detected. It relaxes the computational requirements of the microprocessor and reduces the overall power consumption. The INT/LOCK is automatically deasserted again after nine data clock cycles.

The automatic sync/ID word detection feature is enabled by selecting demod mode 2 or 3 in the demodulator setup register. Do this by setting R4_DB (25:23) = [010] or [011]. Bits R5_DB (4:5) are used to set the length of the sync/ID word, which can be 12, 16, 20, or 24 bits long. The transmitter must transmit the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync byte detection hardware.

For systems using FEC, an error tolerance parameter can also be programmed that accepts a valid match when up to three bits of the word are incorrect. The error tolerance value is assigned in R5_DB (6:7).

APPLICATIONS

LNA/PA MATCHING

The ADF7020-1 exhibits optimum performance in terms of sensitivity, transmit power, and current consumption only if its RF input and output ports are properly matched to the antenna impedance. For cost-sensitive applications, the ADF7020-1 is equipped with an internal Rx/Tx switch, which facilitates the use of a simple combined passive PA/LNA matching network. Alternatively, an external Rx/Tx switch such as the Analog Devices ADG919 can be used, which yields a slightly improved receiver sensitivity and lower transmitter power consumption.

External Rx/Tx Switch

Figure 33 shows a configuration using an external Rx/Tx switch. This configuration allows an independent optimization of the matching and filter network in the transmit and receive path, and is, therefore, more flexible and less difficult to design than the configuration using the internal Rx/Tx switch. The PA is biased through inductor L1, while C1 blocks dc current. Both elements, L1 and C1, also form the matching network, which transforms the source impedance into the optimum PA load impedance, Z_{OPT_PA}.
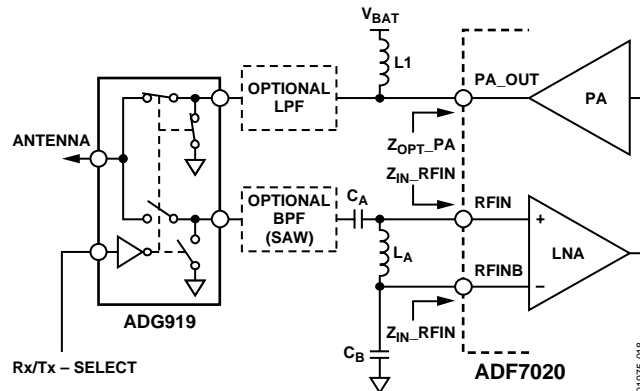
Figure 33. ADF7020-1 with External Rx/Tx Switch

Z_{OPT}_PA depends on various factors such as the required output power, the frequency range, the supply voltage range, and the temperature range. Selecting an appropriate Z_{OPT}_PA helps to minimize the Tx current consumption in the application. Application Note AN-767 contains a number of Z_{OPT}_PA values for representative conditions. Under certain conditions, however, it is recommended to obtain a suitable Z_{OPT}_PA value by means of a load-pull measurement.

Due to the differential LNA input, the LNA matching network must be designed to provide both a single-ended to differential conversion and a complex conjugate impedance match. The network with the lowest component count that can satisfy these requirements is the configuration shown in Figure 33, which consists of two capacitors and one inductor. A first-order implementation of the matching network can be obtained by understanding the arrangement as two L type matching networks

in a back-to-back configuration. Due to the asymmetry of the network with respect to ground, a compromise between the input reflection coefficient and the maximum differential signal swing at the LNA input must be established. The use of appropriate CAD software is strongly recommended for this optimization.

Depending on the antenna configuration, the user might need a harmonic filter at the PA output to satisfy the spurious emission requirement of the applicable government regulations. The harmonic filter can be implemented in various ways, such as a discrete LC pi or T-stage filter. The immunity of the ADF7020-1 to strong out-of-band interference can be improved by adding a band-pass filter in the Rx path or alternatively by selecting one of the high linearity modes outlined in Table 5.

Internal Rx/Tx Switch

Figure 34 shows the ADF7020-1 in a configuration where the internal Rx/Tx switch is used with a combined LNA/PA matching network. This is the configuration used in the ADF7020-1DBX Evaluation boards. For most applications, the slight performance degradation of 1 dB to 2 dB caused by the internal Rx/Tx switch is acceptable, allowing the user to take advantage of the cost saving potential of this solution. The design of the combined matching network must compensate for the reactance presented by the networks in the Tx and the Rx paths, taking the state of the Rx/Tx switch into consideration.
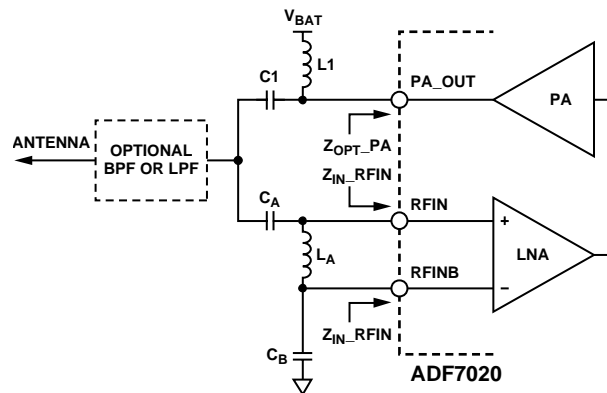
Figure 34. ADF7020-1 with Internal Rx/Tx Switch

The procedure typically requires several iterations until an acceptable compromise has been reached. The successful implementation of a combined LNA/PA matching network for the ADF7020-1 is critically dependent on the availability of an accurate electrical model for the PC board. In this context, the use of a suitable CAD package is strongly recommended. To avoid this effort however, a reference design for the ADF7020-1 is provided. Gerber files are available on the analog.com website.

As with the external Rx/Tx switch, an additional LPF or BPF might be required to suppress harmonics in the transmit spectrum or to improve the resilience of the receiver against out-of-band interferers.

TRANSMIT PROTOCOL AND CODING CONSIDERATIONS

PREAMBLE	SYNC WORD	ID FIELD	DATA FIELD	CRC
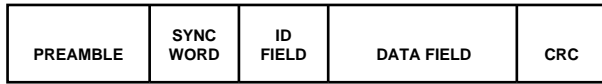
Figure 35. Typical Format of a Transmit Protocol

A dc-free preamble pattern is recommended for FSK/ASK/ OOK demodulation. The recommended preamble pattern is a dc-free pattern such as a 10101010 … pattern. Preamble patterns with longer run-length constraints such as 11001100… can also be used. However, this results in a longer synchronization time of the received bit stream in the receiver.

Manchester coding can be used for the entire transmit protocol. However, the remaining fields that follow the preamble header do not have to use dc-free coding. For these fields, the ADF7020-1 can accommodate coding schemes with a run-length of up to 6 bits without any performance degradation.

If longer run-length coding must be supported, the ADF7020-1 has several other features that can be activated. These involve a range of programmable options that allow the envelope detector output to be frozen after preamble acquisition.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

Table 10 lists the minimum number of writes needed to set up the ADF7020-1 in either Tx or Rx mode after CE is brought high. Additional registers can also be written to tailor the part to a particular application, such as setting up sync byte detection or enabling AFC. When going from Tx to Rx or vice versa, the user needs to write only to the N Register to alter the LO by 200 kHz and to toggle the Tx/Rx bit.

Table 10. Minimum Register Writes Required for Tx/Rx Setup

Mode	Registers				
Tx	Reg 0	Reg 1	Reg 2		
Rx (OOK)	Reg 0	Reg 1	Reg 2	Reg 4	Reg 6
Rx (G/FSK)	Reg 0	Reg 1	Reg 2	Reg 4	Reg 6
Tx <-> Rx	Reg 0				

Figure 38 and Figure 39 show the recommended programming sequence and associated timing for power-up from standby mode.

INTERFACING TO MICROCONTROLLER/DSP

Low level device drivers are available for interfacing to the ADF7020-1, the ADI ADuC84x microcontroller parts, or the Blackfin ADSP-BF53x DSPs using the hardware connections shown in Figure 36 and Figure 37.
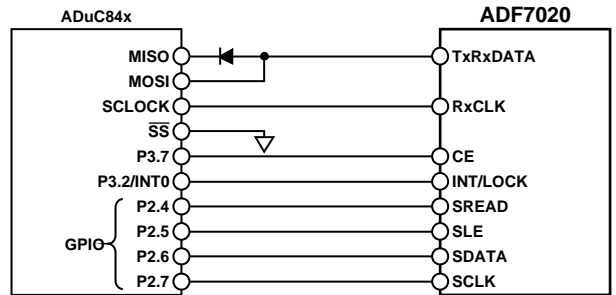
Figure 36.ADuC84x to ADF7020-1 Connection Diagram
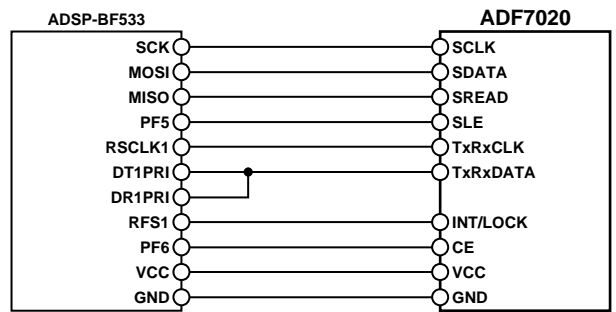
Figure 37.ADSP-BF533 to ADF7020-1 Connection Diagram
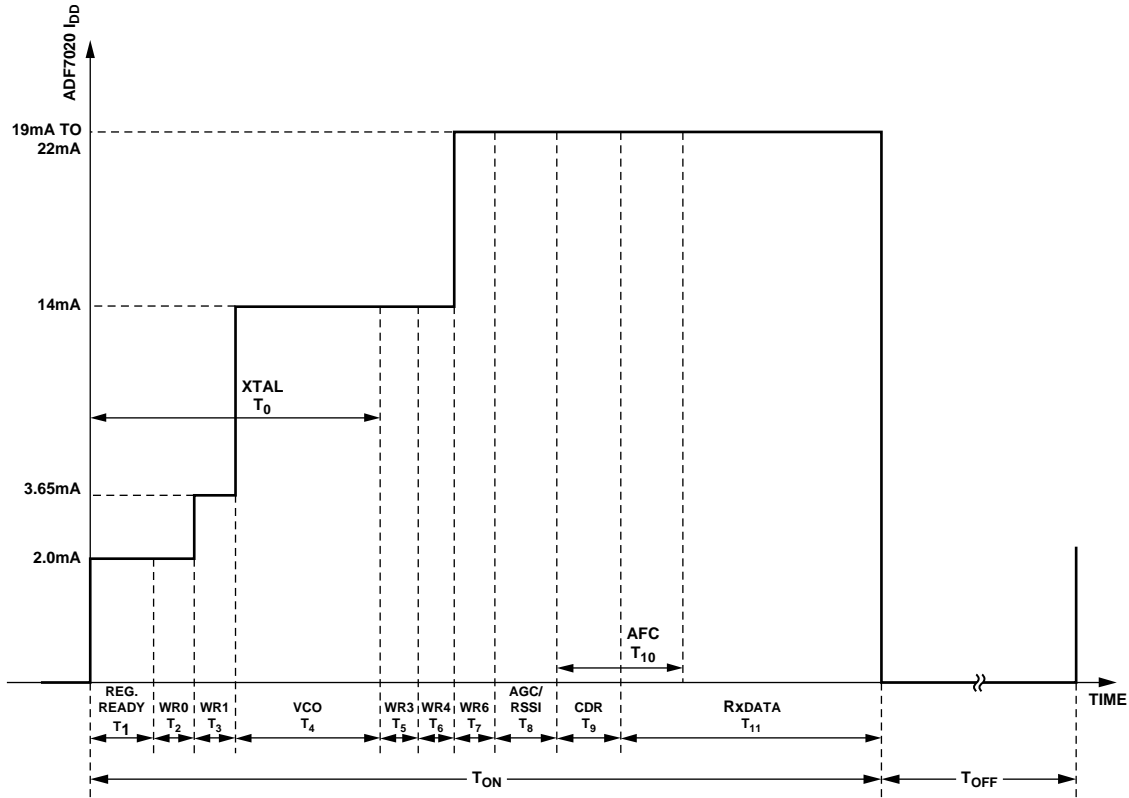
Figure 38. Rx Programming Sequence and Timing Diagram

Table 11. Power-Up Sequence Description

Parameter	Value	Description/Notes	Signal to Monitor
T0	2 ms	Crystal starts power-up after CE is brought high. This typically depends on the crystal type and the load capacitance specified.	CLKOUT
T1	10 µs	Time for regulator to power up. The serial interface can be written to after this time.	MUXOUT
T2, T3, T5, T6, T7	$32 \times 1/\text{SPI\_CLK}$	Time to write to a single register. Maximum SPI_CLK is 25 MHz.	
T4	1 ms	The VCO can power-up in parallel with the crystal. This depends on the CVCO capacitance value used. A value of 22 nF is recommended as a trade-off between phase noise performance and power-up time.	CVCO pin
T8	150 µs	This depends on the number of gain changes the AGC loop needs to cycle through and AGC settings programmed. This is described in more detail in the AGC Information and Timing section.	Analog RSSI on TEST_A pin (Available by writing 0x3800 000C)
T9	$5 \times \text{Bit\_Period}$	This is the time for the clock and data recovery circuit to settle. This typically requires 5-bit transitions to acquire sync and is usually covered by the preamble.	
T10	$16 \times \text{Bit\_Period}$	This is the time for the automatic frequency control circuit to settle. This typically requires 16-bit transitions to acquire lock and is usually covered by an appropriate length preamble.	
T11	Packet Length	Number of bits in payload by the bit period.	
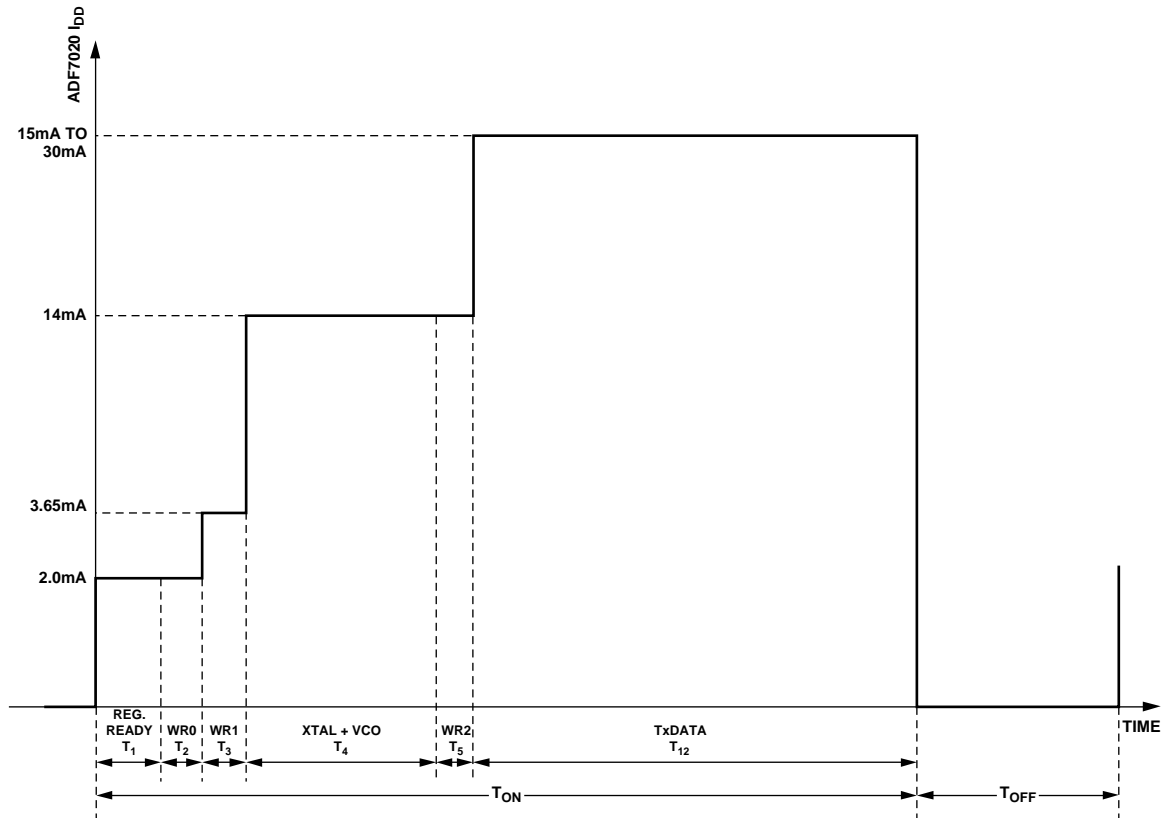
Figure 39. Tx Programming Sequence and Timing Diagram

SERIAL INTERFACE

The serial interface allows the user to program the eleven 32-bit registers using a 3-wire interface (SCLK, SDATA, and SLE). It consists of a level shifter, 32-bit shift register and eleven latches. Signals should be CMOS-compatible. The serial interface is powered by the regulator, and, therefore, is inactive when CE is low.

Data is clocked into the register, MSB first, on the rising edge of each clock (SCLK). Data is transferred to one of eleven latches on the rising edge of SLE. The destination latch is determined by the value of the four control bits (C4 to C1). These are the bottom four LSBs, DB3 to DB0, as shown in the timing diagram in Figure 2. Data can also be read back on the SREAD pin.

READBACK FORMAT

The readback operation is initiated by writing a valid control word to the readback register and setting the readback-enable bit (R7_DB8 = 1). The readback can begin after the control word has been latched with the SLE signal. SLE must be kept high while the data is being read out. Each active edge at the SCLK pin clocks the readback word out successively at the SREAD pin, as shown in Figure 3, starting with the MSB first. The data appearing at the first clock cycle following the latch operation must be ignored.

AFC Readback

The AFC readback is valid only during the reception of FSK signals with either the linear or correlator demodulator active. The AFC readback value is formatted as a signed 16-bit integer comprised of Bits RV1 to RV16, and is scaled according to the following formula:

$$FREQ\_RB \text{ [Hz]} = (AFC\_READBACK \times DEMOD\_CLK)/2^{15}$$

In the absence of frequency errors, the FREQ_RB value is equal to the IF frequency of 200 kHz. Note that, for the AFC readback to yield a valid result, the down-converted input signal must not fall outside the bandwidth of the analogue IF filter. At low-input signal levels, the variation in the readback value can be improved by averaging.

RSSI Readback

The RSSI readback operation yields valid results in Rx mode with ASK or FSK signals. The format of the readback word is shown in Figure 40. It is comprised of the RSSI level information (Bits RV1 to RV7), the current filter gain (FG1, FG2), and the current LNA gain (LG1, LG2) setting. The filter and LNA gain are coded in accordance with the definitions in Register 9. With the reception of ASK modulated signals, averaging of the measured RSSI values improves accuracy. The input power can be calculated from the RSSI readback value as outlined in the RSSI/AGC.

Battery Voltage ADCIN/Temperature Sensor Readback

The battery voltage is measured at Pin VDD4. The readback information is contained in Bits RV1 to RV7. This also applies for the readback of the voltage at the ADCIN pin and the temperature sensor. From the readback information, the battery or ADCIN voltage can be determined using

$$V_{BATTERY} = (Battery\_Voltage\_Readback)/21.1$$
$$V_{ADCIN} = (ADCIN\_Voltage\_Readback)/42.1$$

Silicon Revision Readback

The silicon revision readback word is valid without setting any other registers, especially directly after power-up. The silicon revision word is coded with four quartets in BCD format. The product code (PC) is coded with three quartets extending from Bits RV5 to RV16. The revision code (RV) is coded with 1 quartet extending from Bits RV1 to RV4. The product code for the ADF7020-1 should read back as PC = 0x200. The current revision code should read as RC = 0x6.

Filter Calibration Readback

The filter calibration readback word is contained in Bits RV1 to RV8, and is for diagnostic purposes only. Using the automatic filter calibration function, accessible through Register 6, is recommended. Before filter calibration is initiated decimal 32 should be read back.

READBACK MODE	READBACK VALUE															
	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
AFC READBACK	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
RSSI READBACK	X	X	X	X	X	LG2	LG1	FG2	FG1	RV7	RV6	RV5	RV4	RV3	RV2	RV1
BATTERY VOLTAGE/ADCIN/ TEMP. SENSOR READBACK	X	X	X	X	X	X	X	X	X	RV7	RV6	RV5	RV4	RV3	RV2	RV1
SILICON REVISION	RV16	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1
FILTER CAL READBACK	0	0	0	0	0	0	0	0	RV8	RV7	RV6	RV5	RV4	RV3	RV2	RV1

Figure 40. Readback Value Table

REGISTER 0—N REGISTER
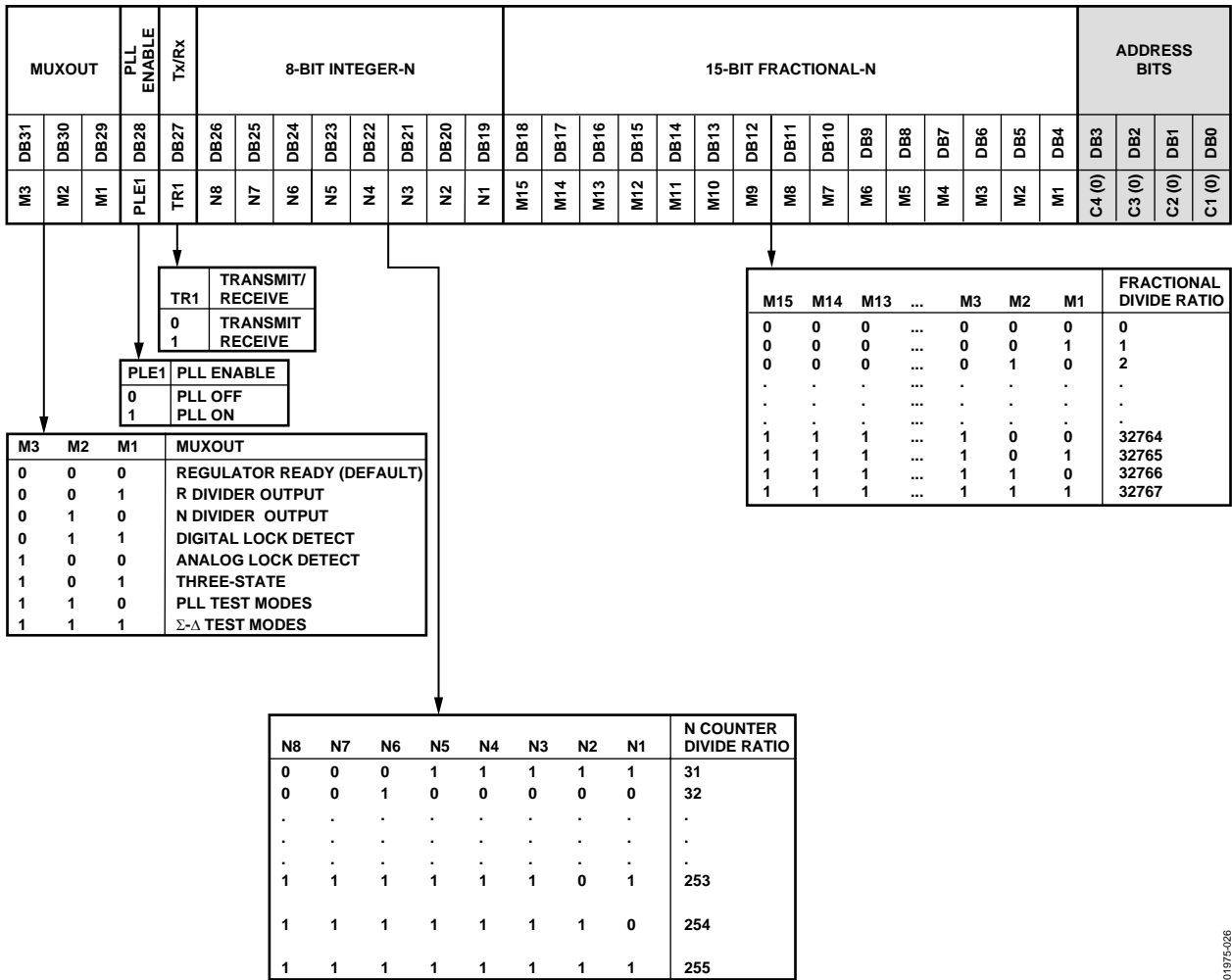
Figure 41.

Notes

1. The Tx/Rx bit (R0_DB27) configures the part in Tx or Rx mode and also controls the state of the internal Tx/Rx switch.

2. $F_{OUT} = \dfrac{XTAL}{R} \times (Integer\text{-}N + \dfrac{Fractional\text{-}N}{2^{15}})$.

REGISTER 1—OSCILLATOR/FILTER REGISTER
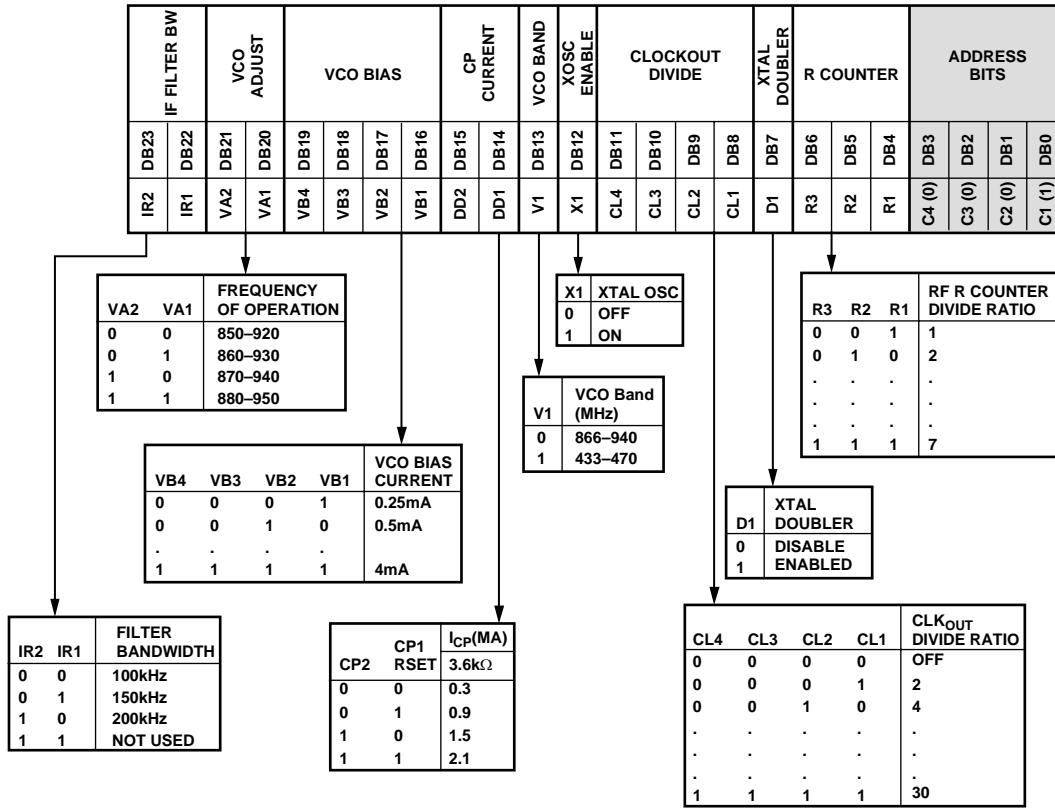
Figure 42.

Notes

1. Set the VCO adjust bits (R1_DB (20:21) to 0 for normal operation.

2. VCO bias setting should be 0x6. All VCO gain numbers are specified for this setting.

3. The Divide-by-2 block is enabled by setting R1_DB13. As this divide block is outside the PLL loop, you need to program an N-value, which corresponds to twice the dividee-by-2 output frequency.

REGISTER 2—TRANSMIT MODULATION REGISTER (ASK/OOK MODE)
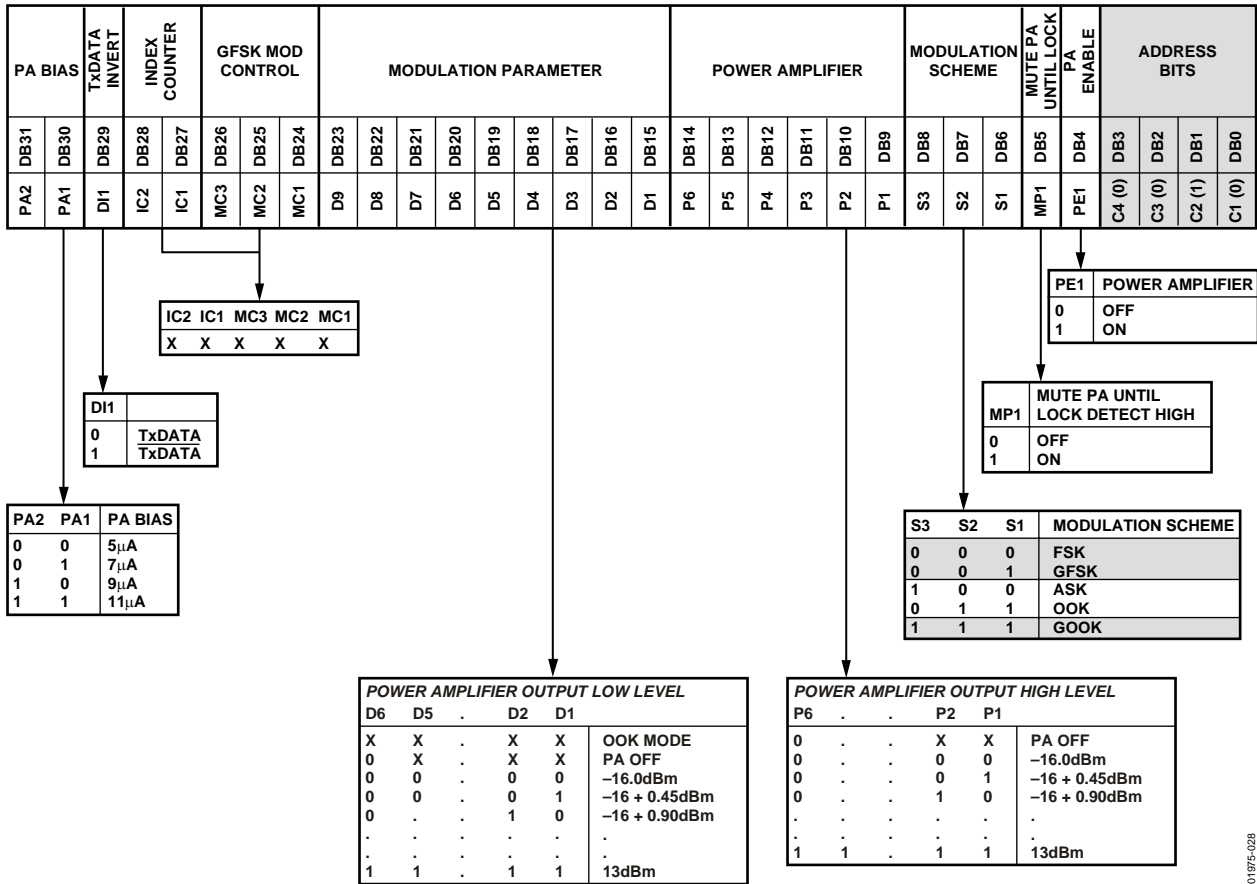
Figure 43.

Notes

1. See the Transmitter section for a description of how the PA bias affects power amplifier level. Default level is 9 µA. If you need maximum power then program this value to 11 µA.

2. See Figure 13.

3. D7, D8, and D9 are don't care bits.

REGISTER 2—TRANSMIT MODULATION REGISTER (FSK MODE)

PA BIAS		TxDATA INVERT	INDEX COUNTER		GFSK MOD CONTROL			MODULATION PARAMETER									POWER AMPLIFIER						MODULATION SCHEME			MUTE PA UNTIL LOCK	PA ENABLE	ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PA2	PA1	DI1	IC2	IC1	MC3	MC2	MC1	D9	D8	D7	D6	D5	D4	D3	D2	D1	P6	P5	P4	P3	P2	P1	S3	S2	S1	MP1	PE1	C4 (0)	C3 (0)	C2 (1)	C1 (0)

IC2	IC1	MC3	MC2	MC1
X	X	X	X	X

DI1	
0	TxDATA
1	TxDATĀ

PA2	PA1	PA BIAS
0	0	5µA
0	1	7µA
1	0	9µA
1	1	11µA

FOR FSK MODE,

D9	....	D3	D2	D1	F DEVIATION
0	....	0	0	0	PLL MODE
0	....	0	0	1	1 × F_{STEP}
0	....	0	1	0	2 × F_{STEP}
0	....	0	1	1	3 × F_{STEP}
.	....	.	.	.	.
1	....	1	1	1	511 × F_{STEP}

PE1	POWER AMPLIFIER
0	OFF
1	ON

MP1	MUTE PA UNTIL LOCK DETECT HIGH
0	OFF
1	ON

S3	S2	S1	MODULATION SCHEME
0	0	0	FSK
0	0	1	GFSK
0	1	0	ASK
0	1	1	OOK
1	1	1	GOOK

POWER AMPLIFIER OUTPUT LEVEL

P6	.	.	P2	P1	
0	.	.	X	X	PA OFF
0	.	.	0	0	−16.0dBm
0	.	.	0	1	−16 + 0.45dBm
0	.	.	1	0	−16 + 0.90dBm
.	.	.	.	.	.
1	1	.	1	1	13dBm

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Figure 44.

Notes

1. $F_{STEP} = PFD/2^{14}$.

2.   PA bias default = 9 µA.

REGISTER 2—TRANSMIT MODULATION REGISTER (GFSK/GOOK MODE)

PA BIAS		TxDATA INVERT	INDEX COUNTER		GFSK MOD CONTROL			MODULATION PARAMETER									POWER AMPLIFIER						MODULATION SCHEME			MUTE PA UNTIL LOCK	PA ENABLE	ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PA2	PA1	DI1	IC2	IC1	MC3	MC2	MC1	D9	D8	D7	D6	D5	D4	D3	D2	D1	P6	P5	P4	P3	P2	P1	S3	S2	S1	MP1	PE1	C4 (0)	C3 (0)	C2 (1)	C1 (0)

D7	...	D3	D2	D1	DIVIDER_FACTOR
0	...	0	0	0	INVALID
0	...	0	0	1	1
0	...	0	1	0	2
0	...	0	1	1	3
.	...	.	.	.	.
1	...	1	1	1	127

PE1	POWER AMPLIFIER
0	OFF
1	ON

DI1	
0	TxDATA
1	$\overline{\text{TxDATA}}$

MP1	MUTE PA UNTIL LOCK DETECT HIGH
0	OFF
1	ON

PA2	PA1	PA BIAS
0	0	5μA
0	1	7μA
1	0	9μA
1	1	11μA

D9	D8	GAUSSIAN – OOK MODE
0	0	NORMAL MODE
0	1	OUTPUT BUFFER ON
1	0	BLEED CURRENT ON
1	1	BLEED/BUFFER ON

S3	S2	S1	MODULATION SCHEME
0	0	0	FSK
0	0	1	GFSK
1	0	0	ASK
0	1	1	OOK
1	1	1	GOOK

IC2	IC1	INDEX_COUNTER
0	0	16
0	1	32
1	0	64
1	1	128

POWER AMPLIFIER OUTPUT LEVEL

P6	.	.	P2	P1	
0	.	.	X	X	PA OFF
0	.	.	0	0	−16.0dBm
0	.	.	0	1	−16 + 0.45dBm
0	.	.	1	0	−16 + 0.90dBm
.	.	.	.	.	.
1	1	.	1	1	13dBm

MC3	MC2	MC1	GFSK_MOD_CONTROL
0	0	0	0
0	0	1	1
.	.	.	.
1	1	1	7

01975-030

Figure 45.

Notes

1. $GFSK\_DEVIATION = (2^{GFSK\_MOD\_CONTROL} \times PFD)/2^{12}$.

2. $Data\text{-}Rate = PFD/(INDEX\_COUNTER \times DIVIDER\_FACTOR)$.

3. PA Bias default = 9 μA.

REGISTER 3—RECEIVER CLOCK REGISTER

SEQUENCER CLOCK DIVIDE								CDR CLOCK DIVIDE								DEMOD CLOCK DIVIDE	BB OFFSET CLOCK DIVIDE	ADDRESS BITS			
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SK8	SK7	SK6	SK5	SK4	SK3	SK2	SK1	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	OK2	OK1	BK2	BK1	C4(0)	C3(0)	C2(1)	C1(1)

SK8	SK7	...	SK3	SK2	SK1	SEQ_CLK_DIVIDE
0	0	...	0	0	1	1
0	0	...	0	1	0	2
.	.	...	.	.	.	.
1	1	...	1	1	0	254
1	1	...	1	1	1	255

BK2	BK1	BBOS_CLK_DIVIDE
0	0	4
0	1	8
1	x	16

OK2	OK1	DEMOD_CLK_DIVIDE
0	0	4
0	1	1
1	0	2
1	1	3

FS8	FS7	...	FS3	FS2	FS1	CDR_CLK_DIVIDE
0	0	...	0	0	1	1
0	0	...	0	1	0	2
.	.	...	.	.	.	.
1	1	...	1	1	0	254
1	1	...	1	1	1	255

Figure 46.

Notes

1. Baseband offset clock frequency (BBOS_CLK) must be greater than 1 MHz and less than 2 MHz, where:

$$BBOS\_CLK = \frac{XTAL}{BBOS\_CLK\_DIVIDE}$$

2. The demodulator clock (DEMOD_CLK) must be < 12 MHz for FSK and < 6 MHz for ASK, where:

$$DEMOD\_CLK = \frac{XTAL}{DEMOD\_CLK\_DIVIDE}$$

3. Data/clock recovery frequency (CDR_CLK) should be within 2% of (32 × data rate), where:

$$CDR\_CLK = \frac{DEMOD\_CLK}{CDR\_CLK\_DIVIDE}$$

Note that this might affect your choice of XTAL, depending on the desired data rate.

4. The sequencer clock (SEQ_CLK) supplies the clock to the digital receive block. It should be close to 100 kHz for FSK and close to 40 kHz for ASK:

$$SEQ\_CLK = \frac{XTAL}{SEQ\_CLK\_DIVIDE}$$

REGISTER 4—DEMODULATOR SET-UP REGISTER

DB31	DB30	DB29	DB28	DB27	DB26	DEMOD LOCK/ SYNC WORD MATCH		DEMODULATOR LOCK SETTING								POSTDEMODULATOR BW											DEMOD SELECT		ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
						LM2	LM1	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DW10	DW9	DW8	DW7	DW6	DW5	DW4	DW3	DW2	DW1	DS2	DS1	C4(0)	C3(1)	C2(0)	C1(0)

DS2	DS1	DEMODULATOR TYPE
0	0	LINEAR DEMODULATOR
0	1	CORRELATOR/DEMODULATOR
1	0	ASK/OOK
1	1	INVALID

DEMOD MODE	LM2	LM1	DL8	DEMOD LOCK/SYNC WORD MATCH	INT/LOCK PIN
0	0	0	0	SERIAL PORT CONTROL – FREE RUNNING	–
1	0	0	1	SERIAL PORT CONTROL – LOCK THRESHOLD	–
2	0	1	0	SYNC WORD DETECT – FREE RUNNING	OUTPUT
3	0	1	1	SYNC WORD DETECT – LOCK THRESHOLD	OUTPUT
4	1	0	X	INTERRUPT/LOCK PIN LOCKS THRESHOLD	INPUT
5	1	1	DL8	DEMOD LOCKED AFTER DL8–DL1 BITS	–

MODE5 ONLY

DL8	DL7	...	DL3	DL2	DL1	LOCK_THRESHOLD_TIMEOUT
0	0	...	0	0	0	0
0	0	...	0	0	1	1
0	0	...	0	1	0	2
.	.	...	.	.	.	.
1	1	...	1	1	0	254
1	1	...	1	1	1	255

Figure 47.

01975-032

Notes

1. Demodulator Modes 1, 3, 4, and 5 are modes that can be activated to allow the ADF7020-1 to demodulate data-encoding schemes that have run-length constraints greater than 7.

2. $Post\_Demod\_BW = 2^{11} \pi F_{CUTOFF}/DEMOD\_CLK$, where the cutoff frequency (F_{CUTOFF}) of the postdemodulator filter should typically be 0.75 times the data-rate.

3. For Mode 5, the *timeout delay to lock threshold* = $(LOCK\_THRESHOLD\_SETTING)/SEQ\_CLK$, where *SEQ_CLK* is defined in the Register 3—Receiver Clock Register section.

REGISTER 5—SYNC BYTE REGISTER

SYNC BYTE SEQUENCE																								MATCHING TOLERANCE		SYNC BYTE LENGTH		CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
																								MT2	MT1	PL2	PL1	C4(0)	C3(1)	C2(0)	C1(1)

PL2	PL1	SYNC BYTE LENGTH
0	0	12 BITS
0	1	16 BITS
1	0	20 BITS
1	1	24 BITS

MT2	MT1	MATCHING TOLERANCE
0	0	0 ERRORS
0	1	1 ERROR
1	0	2 ERRORS
1	1	3 ERRORS
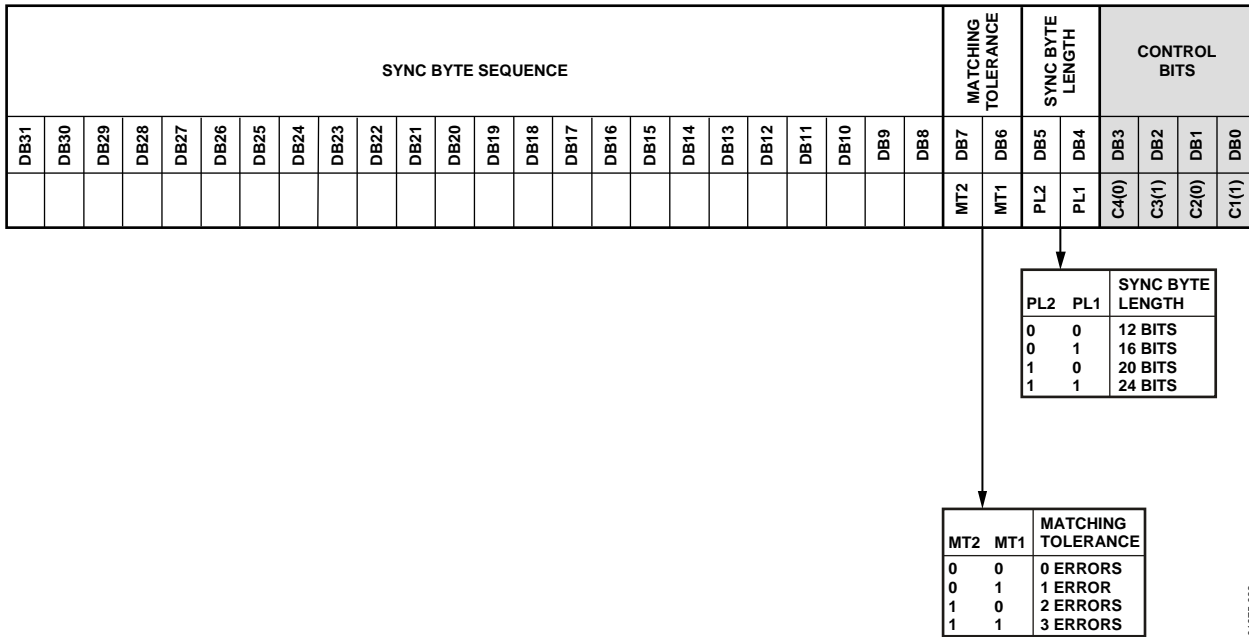
Figure 48.

Notes

1. Sync byte detect is enabled by programming Bits R4_DB (25:23) to [010] or [011].

2. This register allows a 24-bit sync byte sequence to be stored internally. If the sync byte detect mode is selected, then the INT/LOCK pin goes high when the sync byte has been detected in Rx mode. Once the sync word detect signal has gone high, it goes low again after nine data bits.

3. The transmitter must Tx the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync byte detection hardware.

4. Choose a sync byte pattern that has good autocorrelation properties, for example, more 1s than 0s.

REGISTER 6—CORRELATOR/DEMODULATOR REGISTER
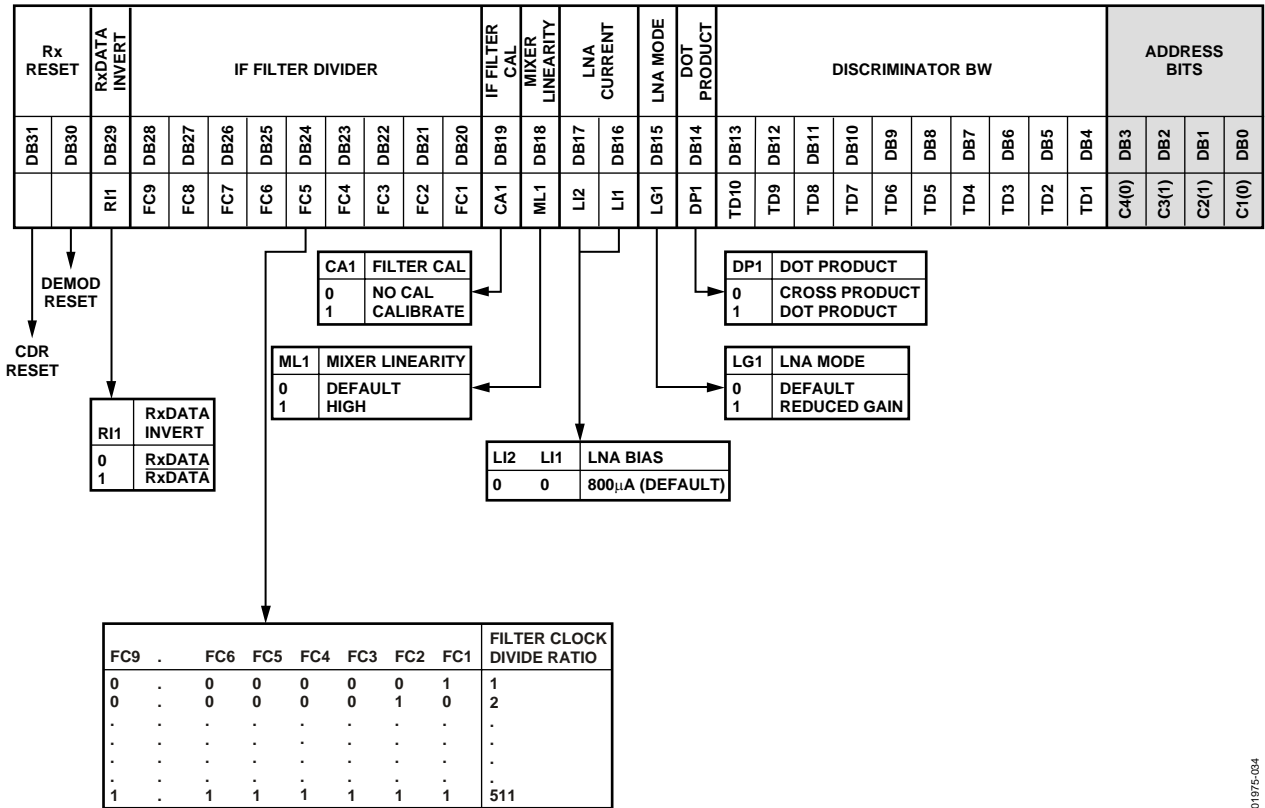
Figure 49.

Notes

1. See the FSK Correlator/Demodulator section for an example of how to determine register settings.

2. Nonadherence to correlator programming guidelines results in poorer sensitivity.

3. The filter clock is used to calibrate the IF filter. The filter clock divide ratio should be adjusted so that the frequency is 50 kHz. The formula is XTAL/FILTER_CLOCK_DIVIDE.

4. The filter should be calibrated only when the crystal oscillator is settled. The filter calibration is initiated every time Bit R6_DB19 is set high.

5. $Discriminator\_BW = (DEMOD\_CLK \times K)/(800 \times 10^3)$. See the FSK Correlator/Demodulator section.
   $Maximum\ value = 600$.

6. When LNA Mode = 1 (reduced gain mode), this prevents the Rx from selecting the highest LNA gain setting. This might be used when linearity is a concern. See Table 5 for details of the different Rx modes.

REGISTER 7—READBACK SET-UP REGISTER
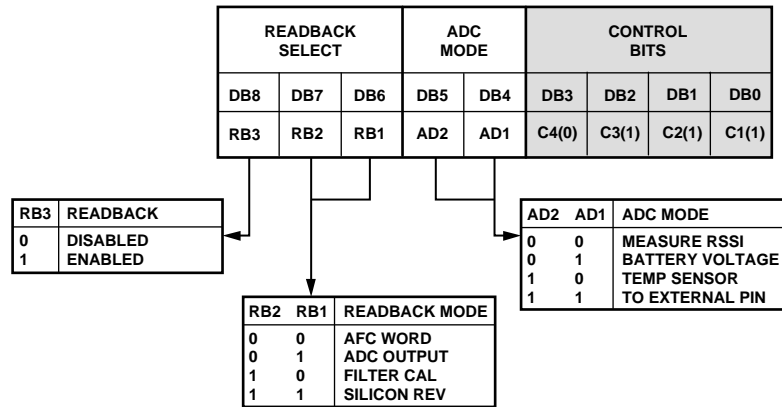
Figure 50.

Notes

1. Readback of the measured RSSI value is valid only in Rx mode. Tn enable readback of the battery voltage, the temperature sensor, or the voltage at the external pin in Rx mode, you need to disable AGC function in Register 9. To read back these parameters in Tx mode you need to first power up the ADC using Register 8, as this is off by default in Tx mode to save power. This is the recommended method of using the battery readback function as most configurations typically require AGC.

2. Readback of the AFC word is valid in Rx mode only if either the linear demodulator or the correlator/demodulator is active.

3. See the Readback Format section for more information.

REGISTER 8—POWER-DOWN TEST REGISTER
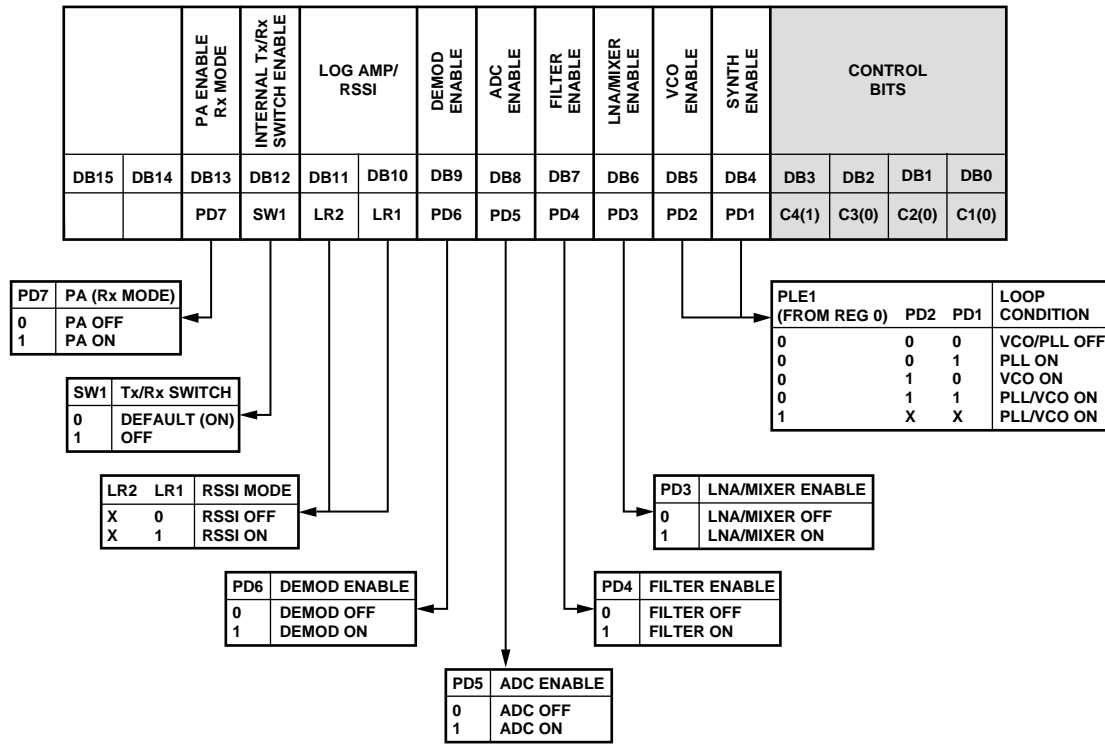
Figure 51.

Notes

1. For a combined LNA/PA matching network, Bit R8_DB12 should always be set to 0. This is the power-up default condition.

2. It is not necessary to write to this register under normal operating conditions.

REGISTER 9—AGC REGISTER

				DIGITAL TEST IQ	FILTER CURRENT	FILTER GAIN		LNA GAIN		GAIN CONTROL	AGC SEARCH	AGC HIGH THRESHOLD							AGC LOW THRESHOLD							ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
							FI1	FG2	FG1	LG2	LG1	GC1	GS1	GH7	GH6	GH5	GH4	GH3	GH2	GH1	GL7	GL6	GL5	GL4	GL3	GL2	GL1	C4(1)	C3(0)	C2(0)	C1(1)

FI1	FILTER CURRENT
0	LOW
1	HIGH

FG2	FG1	FILTER GAIN
0	0	8
0	1	24
1	0	72
1	1	INVALID

LG2	LG1	LNA GAIN
0	0	<1
0	1	3
1	0	10
1	1	30

GS1	AGC SEARCH
0	AUTO AGC
1	HOLD SETTING

GC1	GAIN CONTROL
0	AUTO
1	USER

GL7	GL6	GL5	GL4	GL3	GL2	GL1	AGC LOW THRESHOLD
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	1	1	1	0	1	61
1	1	1	1	1	1	0	62
1	1	1	1	1	1	1	63

GH7	GH6	GH5	GH4	GH3	GH2	GH1	RSSI LEVEL CODE
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	0	0	1	1	1	0	78
1	0	0	1	1	1	1	79
1	0	1	0	0	0	0	80

01975-037

Figure 52.

Notes

1. Default AGC_LOW_THRESHOLD = 30, default AGC_HIGH_THRESHOLD = 70. See the RSSI/AGC for details.

2. AGC high and low settings must be more than 30 apart to ensure correct operation.

3. LNA gain of 30 is available only if LNA mode, R6_DB15, is set to zero.

REGISTER 10—AGC 2 REGISTER

			SELECT I/Q	I/Q PHASE ADJUST				RESERVED	SELECT IQ	UP/DOWN	I/Q GAIN ADJUST					AGC DELAY				LEAK FACTOR				PEAK RESPONSE				ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
			SIQ2	PH4	PH3	PH2	PH1	R1	SIQ1	UD1	GC5	GC4	GC3	GC2	GC1	DH4	DH3	DH2	DH1	GL7	GL6	GL5	GL4	PR4	PR3	PR2	PR1	C4 (1)	C3 (0)	C2 (1)	C1 (0)

SIQ2	SELECT IQ
0	PHASE TO I CHANNEL
1	PHASE TO Q CHANNEL

SIQ2	SELECT IQ
0	GAIN TO I CHANNEL
1	GAIN TO Q CHANNEL

DEFAULT = 0xA

DEFAULT = 0xA

DEFAULT = 0x2

01975-038

Figure 53.

Notes

1. This register is not used under normal operating conditions.

2. For ASK/OOK modulation, the recommended settings for operation over the full input range is peak response = 6, leak factor = 10 (default) and AGC delay =10 (default). Bits DB31 to DB16 should be cleared.
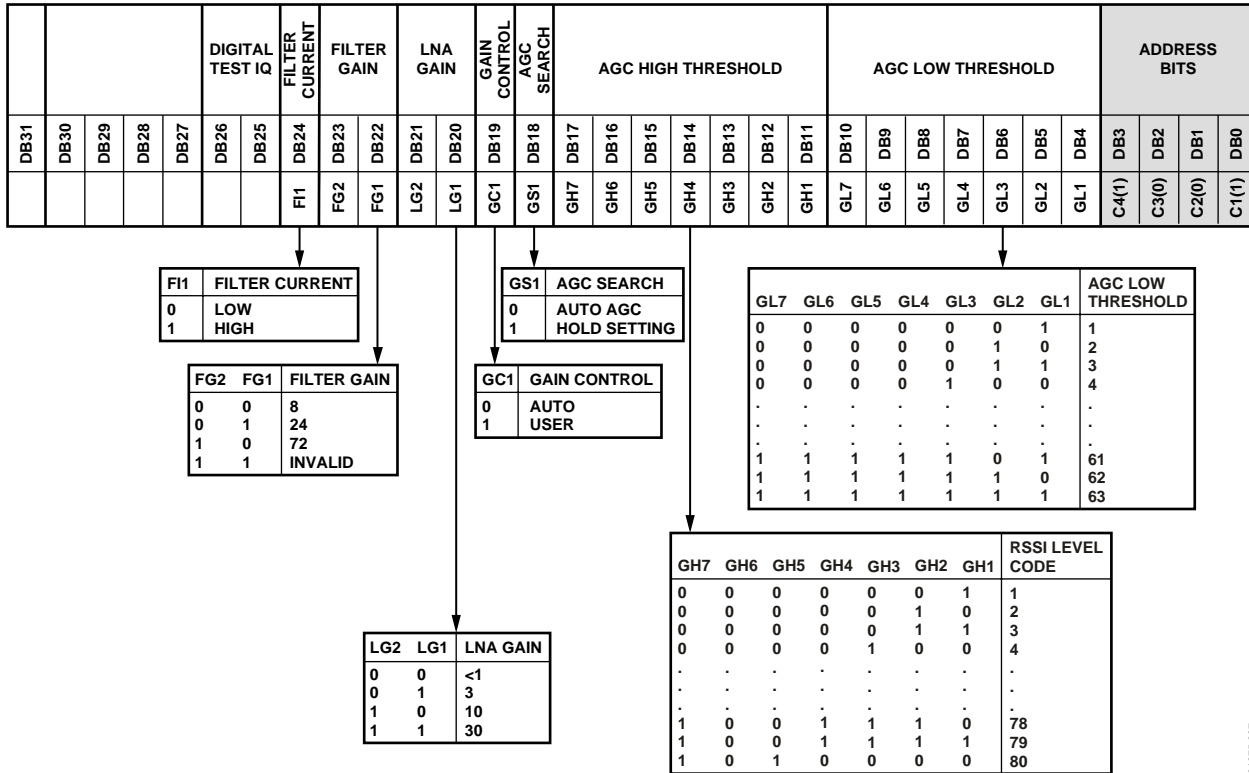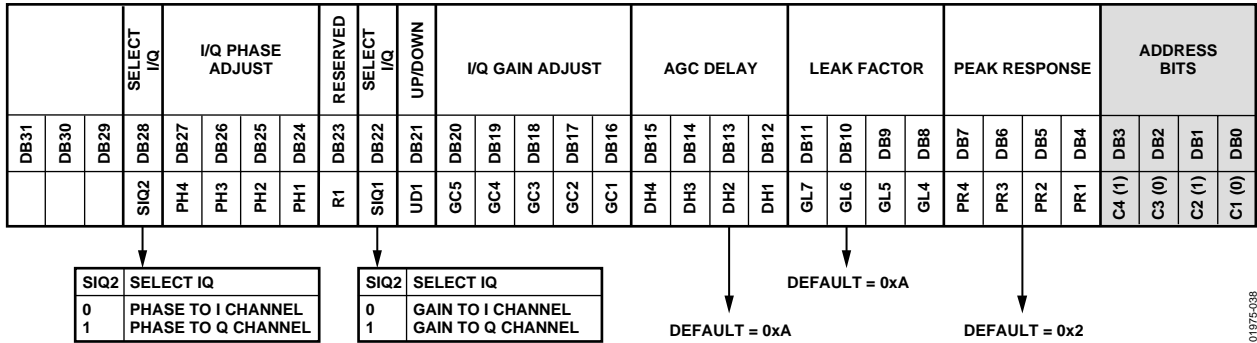
REGISTER 11—AFC REGISTER

											AFC ENABLE	AFC SCALING COEFFICIENT																CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
											AE1	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

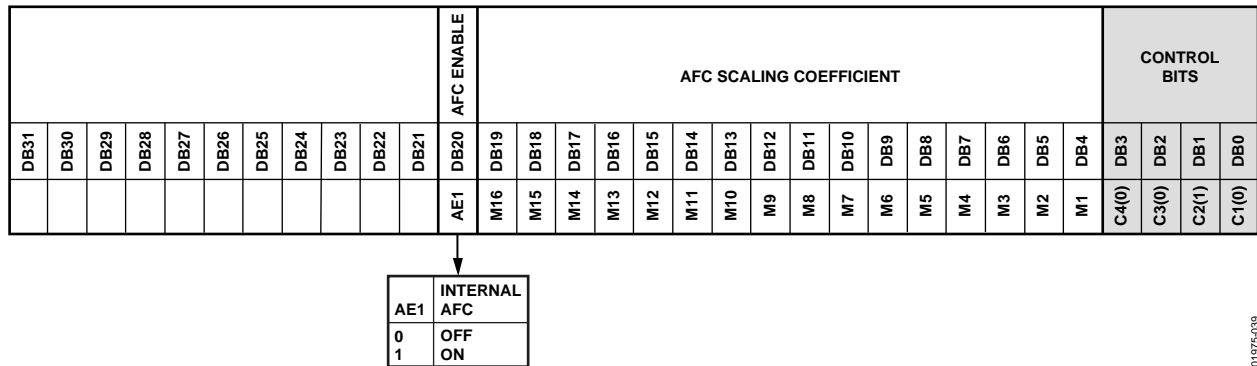| AE1	INTERNAL AFC
0	OFF
1	ON

01975-039

Figure 54.

Notes

1. See the Internal AFC section to program AFC scaling coefficient bits.

2. The AFC scaling coefficient bits can be programmed using the following formula:
$AFC\_Scaling\_Coefficient = Round((500 \times 2^{24})/XTAL)$
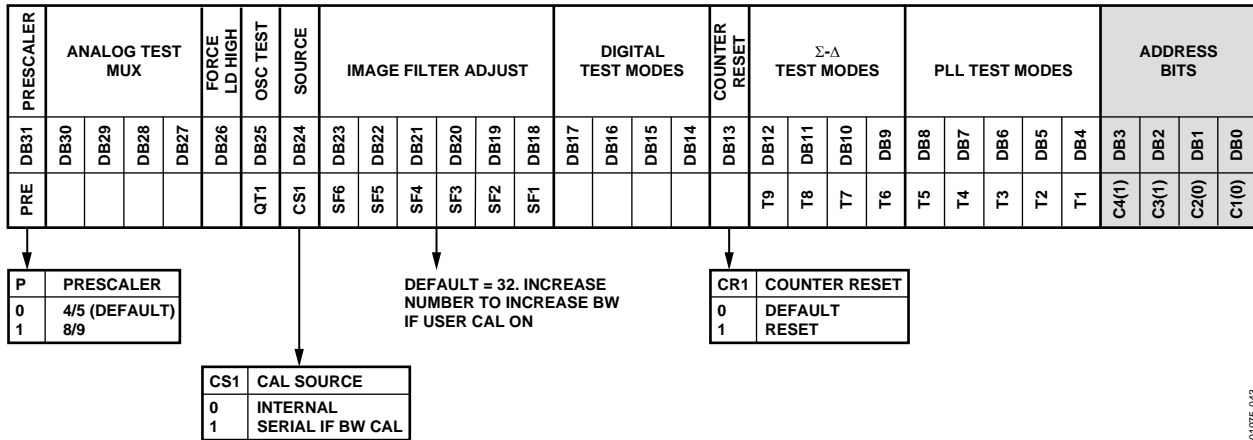
REGISTER 12—TEST REGISTER

PRESCALER	ANALOG TEST MUX				FORCE LD HIGH	OSC TEST	SOURCE	IMAGE FILTER ADJUST						DIGITAL TEST MODES				COUNTER RESET	Σ-Δ TEST MODES				PLL TEST MODES					ADDRESS BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PRE						QT1	CS1	SF6	SF5	SF4	SF3	SF2	SF1						T9	T8	T7	T6	T5	T4	T3	T2	T1	C4(1)	C3(1)	C2(0)	C1(0)

P	PRESCALER
0	4/5 (DEFAULT)
1	8/9

DEFAULT = 32. INCREASE NUMBER TO INCREASE BW IF USER CAL ON

CR1	COUNTER RESET
0	DEFAULT
1	RESET

CS1	CAL SOURCE
0	INTERNAL
1	SERIAL IF BW CAL

01975-043

Figure 55.

Using the Test DAC on the ADF7020-1 to Implement Analog FM DEMOD and Measuring SNR

The test DAC allows the output of the postdemodulator filter for both the linear and correlator/demodulators (Figure 31 and Figure 32) to be viewed externally. It takes the 16-bit filter output and converts it to a high frequency, single-bit output using a second-order error feedback Σ-Δ converter. The output can be viewed on the XCLK_OUT pin. This signal, when IF filtered appropriately, can then be used to

- Monitor the signals at the FSK/ASK postdemodulator filter output. This allows the demodulator output SNR to be measured. Eye diagrams can also be constructed of the received bit stream to measure the received signal quality.

- Provide analog FM demodulation.

While the correlators and filters are clocked by DEMOD_CLK, CDR_CLK clocks the test DAC. Note that, although the test DAC functions in a regular user mode, the best performance is achieved when the CDR_CLK is increased up to or above the frequency of DEMOD_CLK. The CDR block does not function when this condition exists.

Programming the test register, Register 12, enables the test DAC. Both the linear and correlator/demodulator outputs can be multiplexed into the DAC.

Register 13 allows a fixed offset term to be removed from the signal (to remove the IF component in the ddt case). It also has a signal gain term to allow the usage of the maximum dynamic range of the DAC.

Setting Up the Test DAC

- Digital test modes = 7: enables the test DAC, with no offset removal.

- Digital test modes = 10: enables the test DAC, with offset removal.

The output of the active demodulator drives the DAC, that is, if the FSK correlator/demodulator is selected, the correlator filter output drives the DAC.

REGISTER 13—OFFSET REMOVAL AND SIGNAL GAIN REGISTER

TEST DAC GAIN						TEST DAC OFFSET REMOVAL										PULSE EXTENSION				KI				KP				CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
																PE4	PE3	PE2	PE1									C4(1)	C3(1)	C2(0)	C1(1)

```
PE4  PE3  PE2  PE1   PULSE EXTENSION
0    0    0    0     NORMAL PULSE WIDTH
0    0    0    1     2 × PULSE WIDTH
0    0    1    0     3 × PULSE WIDTH
.    .    .    .     .
.    .    .    .     .
.    .    .    .     .
1    1    1    1     16 × PULSE WIDTH
```
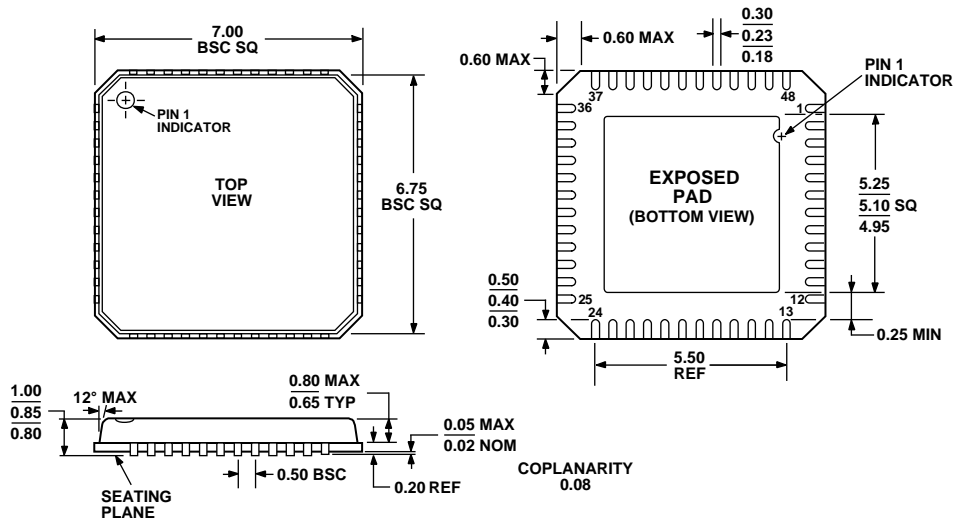
Figure 56.

Notes

1. Because the linear demodulator's output is proportional to frequency, it usually consists of an offset combined with a relatively low signal. The offset can be removed, up to a maximum of 1.0 and gained to use the full dynamic range of the DAC:

   $DAC\_input = (2^\wedge \ Test\_DAC\_Gain) \times (Signal - Test\_DAC\_Offset\_Removal/4096)$

OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 57. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF7020-1BCPZ[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
ADF7020-1BCPZ-RL[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
ADF7020-1BCPZ-RL7[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
EVAL-ADF70XXMB		Control Mother Board	
EVAL-ADF70XXMB2		Evaluation Platform	
EVAL-ADF7020-1DB4		400 to 435 MHz Daughter Board	

[1] Z = Pb-free part.

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