FAIRCHILD SEMICONDUCTOR®

January 2006

FDMB3800N

Dual N-Channel PowerTrench® MOSFET

4.8A, 30V, 40mΩ

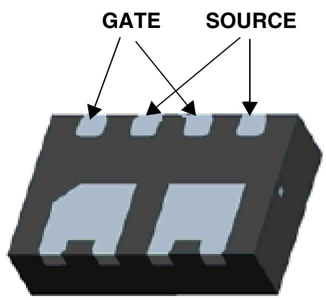
General Description

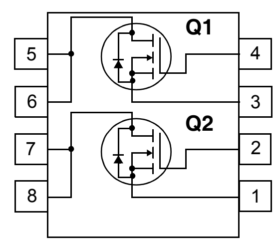
These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- $R_{DS(ON)}$ = 40 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 51 mΩ @ V_{GS} = 4.5 V
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability.
- RoHS Compliant





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current -Continuous	(Note 1a)	4.8	A
	-Pulsed		9	
P_D	Power dissipation for Single Operation	(Note 1a)	1.6	W
	Power dissipation for Single Operation	(Note 1b)	0.75	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	165	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
3800	FDMB3800N	7inch	8mm	3000 units

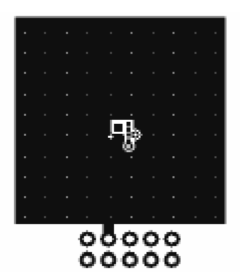
Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA	30	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250µA, Referenced to 25°C	-	24	-	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 24V, V_{GS} = 0V, T_J = 55°C	-	-	10	
I_{GSS}	Gate-Body Leakage,	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250µA, Referenced to 25°C	-	-4	-	mV/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 4.8A	-	32	40	mΩ
		V_{GS} = 4.5V, I_D = 4.3A	-	41	51	
		V_{GS} = 10V, I_D = 4.8A T_J = 125°C	-	43	61	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10V, V_{DS} = 5V	10	-	-	A
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 4.8A	-	14	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz	-	350	465	pF
C_{oss}	Output Capacitance		-	90	120	pF
C_{rss}	Reverse Transfer Capacitance		-	40	60	pF
R_G	Gate Resistance	f=1.0MHz	-	3	-	Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 1A V_{GS} = 10V, R_{GEN} = 6Ω	-	8	16	ns
t_r	Turn-On Rise Time		-	5	10	ns
$t_{d(off)}$	Turn-Off Delay Time		-	21	34	ns
t_f	Turn-Off Fall Time		-	2	10	ns
Q_g	Total Gate Charge	V_{DS} = 15V, I_D = 7.5A, V_{GS} = 5V	-	4	5.6	nC
Q_{gs}	Gate-Source Charge		-	1.0	-	nC
Q_{gd}	Gate-Drain Charge		-	1.5	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		-	-	1.25	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S =1.25 A (Note 2)	-	0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F= 4.8A, dI_F/dt=100A/µs	-	-	22	ns
Q_{rr}	Diode Reverse Recovery Charge		-	-	9	nC

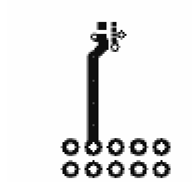
Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

2: Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%



a) 80°C/W when mounted on a 1in^2 pad of 2 oz copper



b) 165°C/W when mounted on a minimum pad of 2 oz copper
Scale 1: 1 on letter size paper

Typical Characteristics

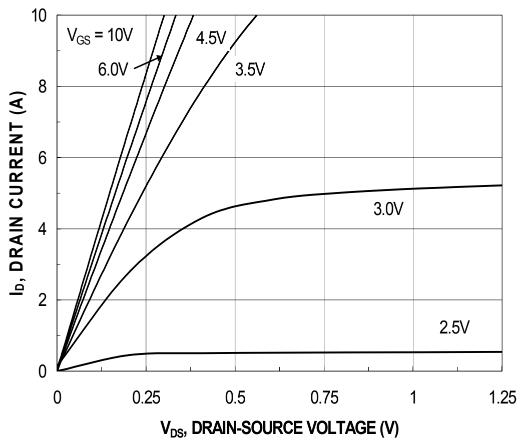


Figure 1. On Region Characteristics

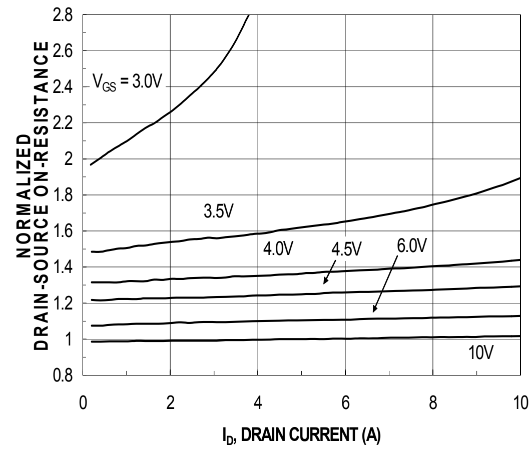


Figure 2. On Resistance vs Drain Current and Gate Voltage

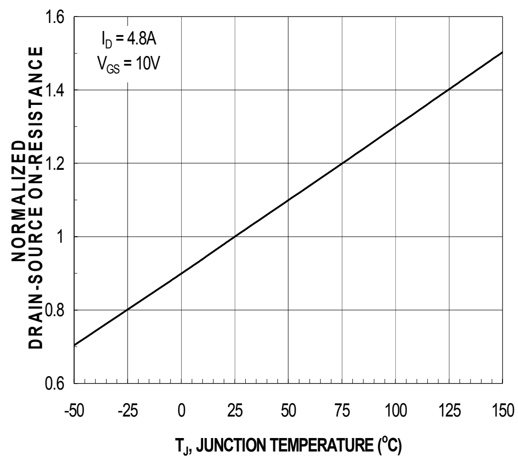


Figure 3. Normalized On Resistance vs Temperature

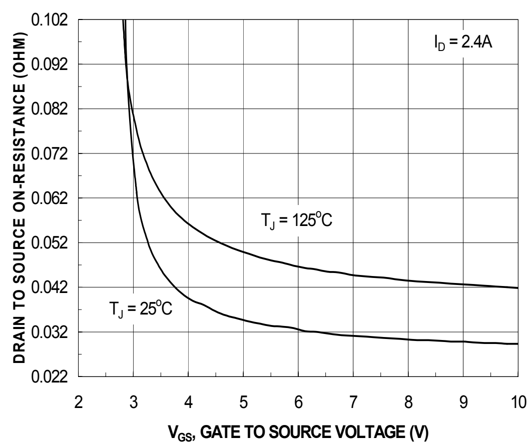


Figure 4. On Resistance vs Gate to Source Voltage

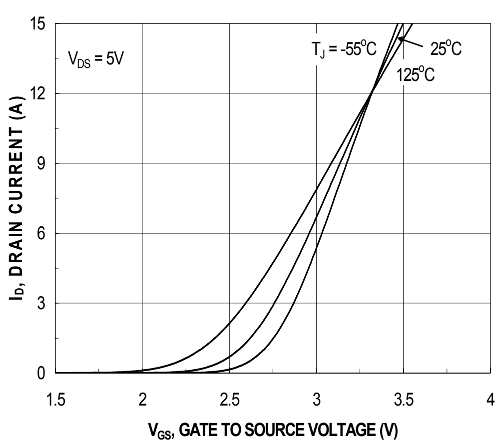


Figure 5. Transfer Characteristics

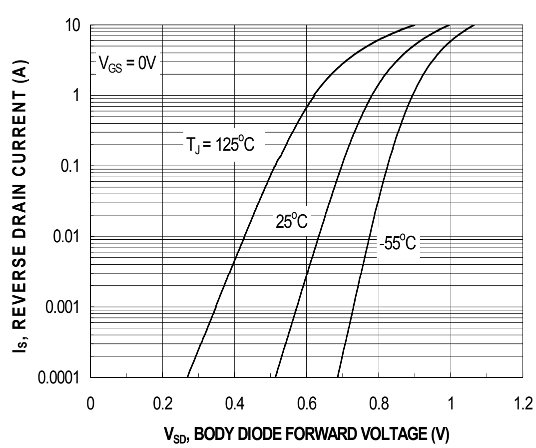


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

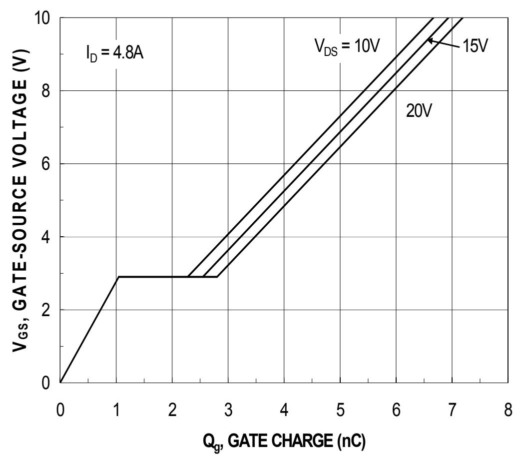


Figure 7. Gate Charge Characteristics

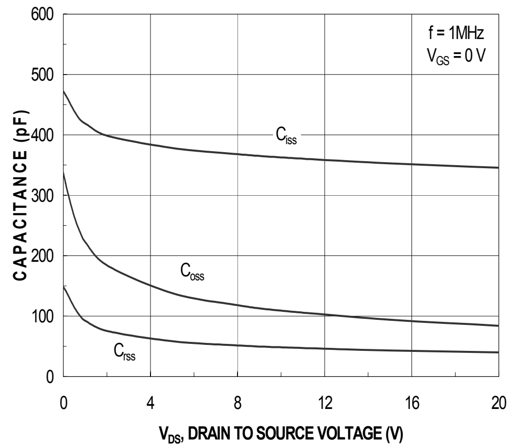


Figure 8. Capacitance vs Drain to Source Voltage

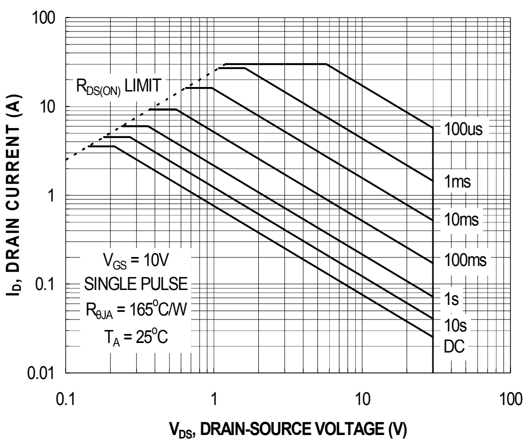


Figure 9. Forward Bias Safe Operating Area

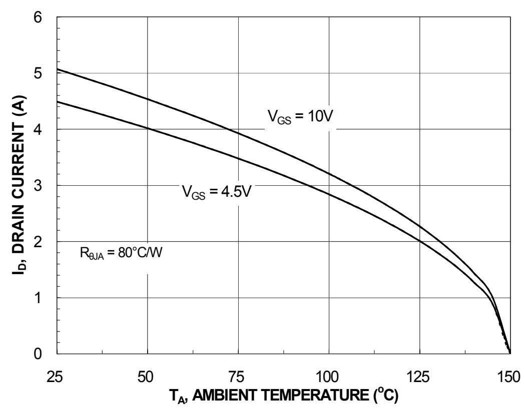


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

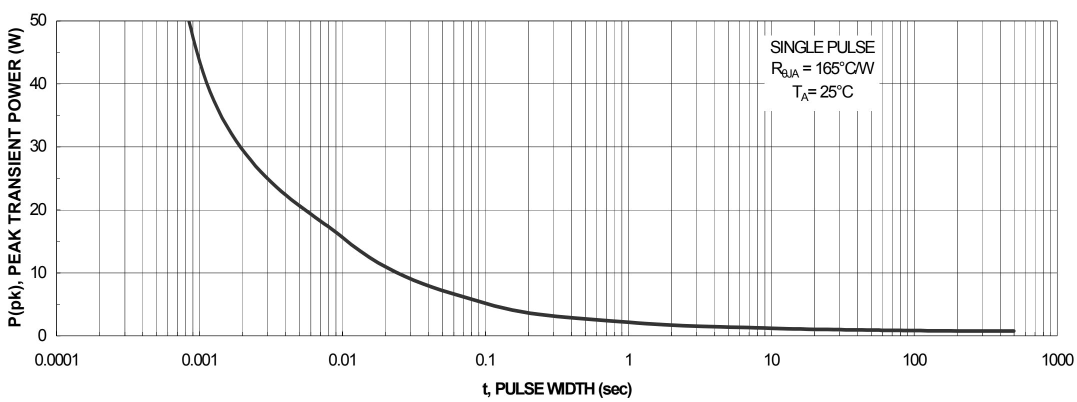


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics

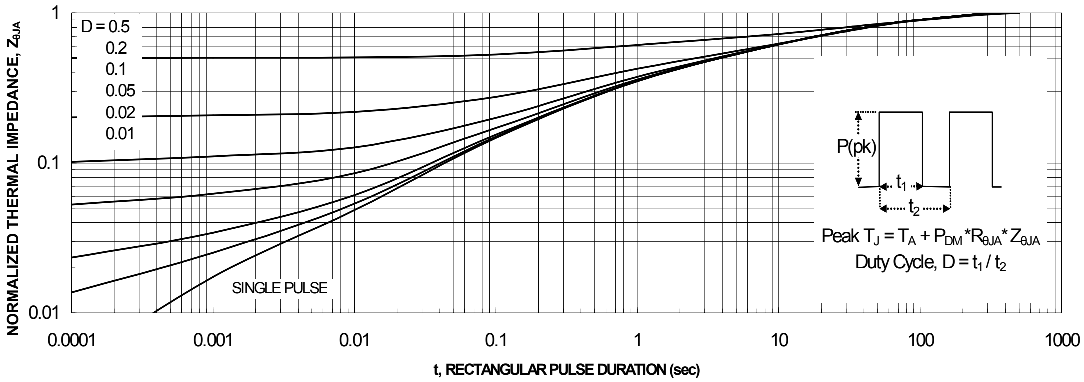
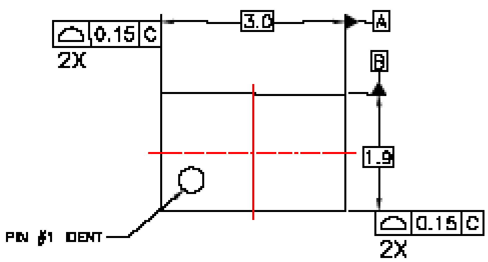


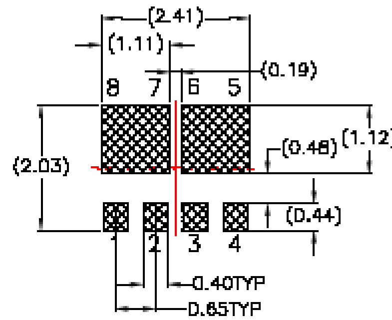
Figure 12. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

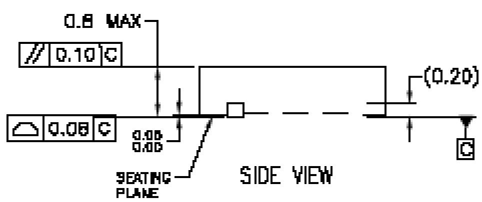
Dimensional Outline and Pad Layout



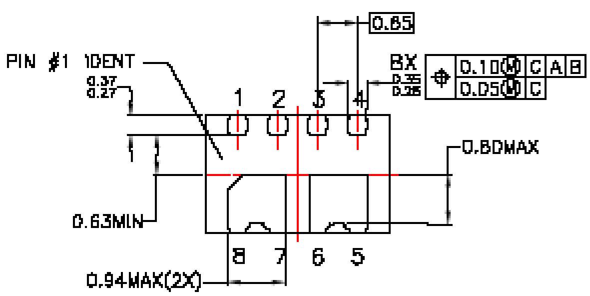
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

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