Data Sheet | August 7, 2006 | FN9177.1

High-Performance Notebook PWM Controller with Bias Regulator and Audio-Frequency Clamp

The ISL6269 IC is a Single-Phase Synchronous-Buck PWM controller featuring Intersil's Robust Ripple Regulator (R^3) technology that delivers truly superior dynamic response to input voltage and output load transients. Integrated MOSFET drivers, 5V LDO, and bootstrap diode result in fewer components and smaller implementation area.

Intersil's R^3 technology combines the best features of fixed-frequency PWM and hysteretic PWM while eliminating many of their shortcomings. R^3 technology employs an innovative modulator that synthesizes an AC ripple voltage signal V_R, analogous to the output inductor ripple current. The AC signal V_R enters a hysteretic comparator where the lower threshold is the error amplifier output V_{COMP}, and the upper threshold is a programmable voltage reference V_W, resulting in generation of the PWM signal. The voltage reference V_W sets the steady-state PWM frequency. Both rising and falling edges of the PWM are modulated, providing faster response to input voltage transients and output load transients than conventional fixed-frequency PWM controllers. Unlike a conventional hysteretic converter, the ISL6269 has an error amplifier that provides ±1% voltage regulation at the FB pin.

The ISL6269 has a 1.5ms digital soft-start and can be started into a pre-biased output voltage. A resistor divider is used to program the output voltage setpoint. The ISL6269 can be configured to operate in forced-continuous-conduction-mode (FCCM) or in diode-emulation-mode (DEM), which improves light-load efficiency. In FCCM the controller always operates as a synchronous rectifier, switching the low-side MOSFET regardless of the output load, however with DEM enabled, the low-side MOSFET is disabled preventing negative current flow from the output inductor during low load operation. An audio filter prevents the PWM switching frequency from entering the audible spectrum due to extremely light load while in DEM.

A PGOOD pin indicates when the converter is capable of supplying regulated voltage. The ISL6269 features a unique fault-identification capability that can drastically reduce trouble-shooting time and effort. The pull-down resistance of the PGOOD pin is 30Ω for an overcurrent fault, 60Ω for an overvoltage fault, or 90Ω for either an undervoltage fault or during soft-start. The overcurrent protection is accomplished by measuring the voltage drop across the $r_{DS(ON)}$ of the low-side MOSFET. A single resistor programs the overcurrent and short-circuit points. Overvoltage and undervoltage protection is monitored at the FB voltage feedback pin.

Features

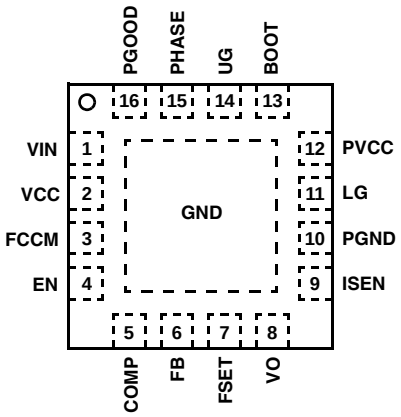
- High performance synthetic ripple regulation
- Extremely fast transient response
- External type-two loop compensation
- ±1% regulation accuracy: -10°C to +100°C
- Starts into a pre-biased output
- Wide input voltage range: +7.0V to +25.0V
- Wide output voltage range: +0.6V to +3.3V
- Wide output load range: 0A to 25A
- Programmable PWM frequency: 200kHz to 600kHz
- Power good monitor
- Fault identification by PGOOD pull-down resistance
- Integrated MOSFET drivers with shoot-through protection
- Internal digital soft-start
- Internal 5V LDO for self-biasing from up to 25V
- Configure forced continuous conduction or diode emulation for increased light load efficiency
- PWM minimum frequency above audible spectrum
- Integrated boot-strap diode
- Low-side MOSFET $r_{DS(ON)}$ overcurrent protection
- Undervoltage protection
- Soft crowbar overvoltage protection
- Over-temperature protection
- Pb-free plus anneal available (RoHS compliant)

Applications

- PCI express graphical processing unit
- Auxiliary power rail
- VRM
- Network adapter

Pinout

16 LD QFN (4mm x 4mm)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6269CRZ (See Note)	6269CRZ	-10 to +100	16 Ld 4x4 QFN (Pb-Free)	L16.4x4
ISL6269CRZ-T (See Note)	6269CRZ	16 Ld 4x4 QFN Tape and Reel (Pb-Free)		L16.4x4

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Voltage Ratings

ISEN, VIN to GND. . . . . -0.3V to +28V
VCC, PGOOD to GND . . . . . -0.3V to +7.0V
PVCC to PGND. . . . . -0.3V to +7.0V
GND to PGND. . . . . -0.3V to +0.3V
EN, FCCM. . . . . -0.3V to GND, VCC +3.3V
PHASE to GND (DC) . . . . . -0.3V to +28V
(<100ns Pulse Width, 10µJ . . . . . -5.0V
BOOT to GND, or PGND . . . . . -0.3V to +33V
BOOT to PHASE . . . . . -0.3V to +7V
UG (DC) . . . . . -0.3V to PHASE, BOOT +0.3V
(<200ns Pulse Width, 20µJ) . . . . . -4.0V
LG (DC). . . . . -0.3V to PGND, PVCC +0.3V
(<100ns Pulse Width, 4µJ) . . . . . -2.0V
ESD Classification . . . . . Level 1 (HBM = 2kV)

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	43	11.5

Junction Temperature Range . . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (soldering, 10s). . . . . +300°C

Recommended Operating Conditions

Ambient Temperature Range . . . . . -10°C to 100°C
Supply Voltage (VIN to GND) . . . . . 7V to 25V

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a highly effective thermal conductivity test board on free air. See Tech Brief TB379 for details
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for V_{IN} = 15V, T_A = (-10°C) to (+100°C), unless otherwise stated. All typical specifications T_A = (+25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN						
VIN Voltage Range	V_{IN}		7.0		25.0	V
VIN Input Bias Current	I_{VIN}	EN and FCCM = 5V, FB = 0.65V, VIN = 7V to 25V		2.2	3.0	mA
VIN Shutdown Current	I_{SHDN}	EN = GND, VIN = 25V		0.1	1.0	µA
VCC LDO						
VCC Output Voltage Range	V_{CC}	VIN = 7V to 25V, I_{LDO} = 0mA to 80mA	4.75	5.00	5.25	V
VCC POR THRESHOLD						
Rising VCC POR Threshold Voltage	V_{CCTHR}		4.35	4.45	4.55	V
Falling VCC POR Threshold Voltage	V_{CCTHF}		4.10	4.20	4.30	V
REGULATION						
Error Amplifier Reference Voltage	V_{REF}			0.6		V
Voltage Regulation Accuracy	V_{REG}		-1		+1	%
PWM						
Frequency Range	F_{OSC}	FCCM = 5V	200		600	kHz
	F_{AUDIO}	FCCM = GND	21	28		kHz
Frequency-Set Accuracy		F_{OSC} = 300kHz	-12		+12	%
VO Range	V_{VO}		0.60		3.30	V
VO Input Leakage Current	I_{VO}	VO = 0.60V VO = 3.30V		1.3 7.0		µA µA
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB}	FB = 0.60V		± 20		nA
COMP Source Current	$I_{COMPSRC}$	FB = 0.40V, COMP = 3.20V		2.5		mA
COMP Sink Current	$I_{COMPSNK}$	FB = 0.80V, COMP = 0.30V		0.3		mA
COMP High Clamp Voltage	V_{COMPHC}	FB = 0.40V, Sink 50µA	3.10	3.40	3.65	V
COMP Low Clamp Voltage	V_{COMPLC}	FB = 0.80V, Source 50µA	0.09	0.15	0.21	V

Electrical Specifications These specifications apply for V_{IN} = 15V, T_A = (-10°C) to (+100°C), unless otherwise stated. All typical specifications T_A = (+25°C) **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PGOOD pull-down Impedance	PGR_{SS}	PGOOD = 5mA Sink	80	95	133	Ω
	PGR_{UV}					
	PGR_{OV}	PGOOD = 5mA Sink	53	63	89	Ω
	PGR_{OC}	PGOOD = 5mA Sink	26	32	46	Ω
PGOOD Leakage Current	I_{PGOOD}	PGOOD = 5V		<0.1	1.0	µA
PGOOD Maximum Sink Current				5.0		mA
PGOOD Soft-Start Delay	T_{SS}	EN High to PGOOD High	2.20	2.75	3.30	ms
GATE DRIVER						
UG Pull-Up Resistance	R_{UGPU}	200mA Source Current (Note 2)		1.0	1.5	Ω
UG Source Current	I_{UGSRC}	V_{UG} to PHASE = 2.5V		2.0		A
UG Sink Resistance	R_{UGPD}	250mA Sink Current (Note 2)		1.0	1.5	Ω
UG Sink Current	I_{UGSNK}	V_{UG} to PHASE = 2.5V		2.0		A
LG Pull-Up Resistance	R_{LGPU}	250mA Source Current (Note 2)		1.0	1.5	Ω
LG Source Current	I_{LGSRC}	V_{LG} to PGND = 2.5V		2.0		A
LG Sink Resistance	R_{LGPD}	250mA Sink Current (Note 2)		0.5	0.9	Ω
LG Sink Current	I_{LGSNK}	V_{LG} to PGND = 2.5V		4.0		A
Delay From UG Falling to LG Rising	t_{UGFLGR}	UG falling to LG rising		21		ns
Delay From LG Falling to UG Rising	t_{LGFUGR}	LG falling to UG rising		14		ns
BOOTSTRAP DIODE						
Forward Voltage	V_F	PVCC = 5V, I_F = 2mA		0.58		V
Reverse Leakage	I_R	V_R = 25V		0.2		µA
CONTROL INPUTS						
EN High Threshold Voltage	V_{ENTHR}		2.0			V
EN Low Threshold Voltage	V_{ENTHF}				0.5	V
FCCM High Threshold Voltage	$V_{FCCMTHR}$		2.0			V
FCCM Low Threshold Voltage	$V_{FCCMTHF}$				1.0	V
EN Leakage Current	I_{ENL}	EN = 0V		<0.1	1.0	µA
	I_{ENH}	EN = 5.0V		20		µA
FCCM Leakage Current	I_{FCCML}	FCCM = 0V		<0.1	1.0	µA
	I_{FCCMH}	FCCM = 5.0V		2.0		µA
PROTECTION						
ISEN OCP Threshold Current	I_{OC}		-33	-26	-19	µA
ISEN Short-Circuit Threshold Current	I_{SC}			-50		µA
UVP Threshold Voltage	V_{UV}		81	84	87	%
OVP Rising Threshold Voltage	V_{OVR}		113	116	119	%
OVP Falling Threshold Voltage	V_{OVF}			103		%
OTP Rising Threshold Temperature	T_{OTR}	(Note 2)		150		°C
OTP Temperature Hysteresis	T_{OTHYS}	(Note 2)		25		°C

NOTE:

3. Guaranteed by design.

Functional Pin Descriptions

GND Pin

Bottom terminal pad of QFN package
Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin, not the PGND pin.

VIN Pin-1 (Input)

The VIN pin measures the converter input voltage with respect to the GND pin. VIN is a required input to the R^3 PWM modulator. The VIN pin is also the input source for the integrated +5V LDO regulator.

VCC Pin-2 (Output)

The VCC pin is the output of the integrated +5V LDO regulator, which provides the bias voltage for the IC. The VCC pin delivers regulated +5V whenever the EN pin is pulled above V_{ENTHR}. For best performance the LDO requires at least a 1µF MLCC decouple capacitor to the GND pin.

FCCM Pin-3 (Logic)

The FCCM pin configures the controller to operate in forced-continuous-conduction-mode (FCCM) or diode-emulation-mode (DEM.) DEM is disabled when the FCCM pin is pulled above the rising threshold voltage $V_{FCCMTHR}$, and DEM is enabled when the FCCM pin is pulled below the falling threshold voltage $V_{FCCMTHF}$.

EN Pin-4 (Logic)

The EN pin is the on/off switch of the IC. When the EN pin is pulled above the rising threshold voltage V_{ENTHR}, V_{CC} will ramp up and begin regulation. The soft-start sequence begins once V_{CC} ramps above the power-on reset (POR) rising threshold voltage V_{CCTHR}. When the EN pin is pulled below the falling threshold voltage V_{ENTHF}, PWM immediately stops and V_{CC} decays below the POR falling threshold voltage V_{CCTHF}, at which time the IC turns off.

COMP Pin-5 (Signal)

The COMP pin is the output of the control-loop error amplifier. Loop compensation components connect from the COMP pin to the FB pin.

FB Pin-6 (Signal)

The FB pin is the inverting input of the control loop error amplifier. The converter will regulate to 600mV at the FB pin with respect to the GND pin. Scale the desired output voltage to 600mV with a voltage divider network made from resistors R_{TOP} and R_{BOTTOM}. Loop compensation components connect from the FB pin to the COMP pin.

FSET Pin-7 (Signal)

The FSET pin programs the PWM switching frequency of the converter. Connect a resistor R_{FSET} and a 10nF capacitor C_{FSET} from the FSET pin to the GND pin.

VO Pin-8 (Input)

The VO pin makes a direct measurement of the converter output voltage used exclusively by the R^3 PWM modulator. The VO pin should be connected to the top of feedback resistor R_{TOP} at the converter output. Refer to Figure 1, Typical Application Schematic.

ISEN Pin-9 (Input)

The ISEN pin is the input to the overcurrent protection (OCP) and short-circuit protection (SCP) circuits. Connect a resistor R_{SEN} between the ISEN pin and the PHASE pin. Select the value of R_{SEN} that will force the ISEN pin to source the I_{SEN} threshold current I_{OC} when the peak inductor current reaches the desired OCP setpoint. The SCP threshold current I_{SC} is fixed at twice the OCP threshold current I_{OC}

PGND Pin-10

The PGND pin should be connected to the source of the low-side MOSFET, preferably with an isolated path that is in parallel with the trace connecting the LG pin to the gate of the MOSFET. The PGND pin is an isolated path used exclusively to conduct the turn-off transient current that flows out the PGND pin, through the gate-source capacitance of the low-side MOSFET, into the LG pin, and back to the PGND pin through the pull-down resistance of the LG driver. The adaptive shoot-through protection circuit, measures the low-side MOSFET gate voltage with respect to the PGND pin, not the GND pin.

LG Pin-11 (Output)

The LG pin is the output of the low-side MOSFET gate driver. Connect to the gate of the low-side MOSFET.

PVCC Pin-12 (Input)

The PVCC pin is the input voltage for the low-side MOSFET gate driver LG. Connect a +5V power source to the PVCC pin with respect to the GND pin, a 1µF MLCC bypass capacitor needs to be connected from the PVCC pin to the PGND pin, not the GND pin. The VCC output may be used for the PVCC input voltage source. Connect the VCC pin to the PVCC pin through a low-pass filter consisting of a resistor and the PVCC bypass capacitor. Refer to Figure 1, Typical Application Schematic.

BOOT Pin-13 (Input)

The BOOT pin is the input voltage for the high-side MOSFET gate driver UG. An MLCC capacitor C_{BOOT} is connected between the BOOT pin and the PHASE pin, the return current path for the UG MOSFET driver. Capacitor C_{BOOT} is charged from the voltage source at the PVCC pin via the internal diode D_{BOOT} each time the PHASE pin drops below PVCC minus diode D_{BOOT} forward voltage drop V_F.

UG Pin-14 (Output)

The UG pin is the output of the high-side MOSFET gate driver. Connect to the gate of the high-side MOSFET.

PHASE Pin-15 (Input)

The PHASE pin is the return current path for the UG MOSFET driver. The PHASE pin also measures the polarity of the low-side MOSFET drain voltage for the diode emulation function. Connect the PHASE pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor. Refer to Figure 1, Typical Application Schematic.

PGOOD Pin-16 (Output)

The PGOOD pin is an open-drain output that is high impedance when the converter is in regulation, or when the EN pin is pulled below the falling threshold voltage V_{ENTHF}. The PGOOD pin has three distinct pull-down impedances that correspond to an OVP fault, OCP/SCP, or UVP and soft-start. Connect the PGOOD pin to a pull-up resistor.

Typical Application

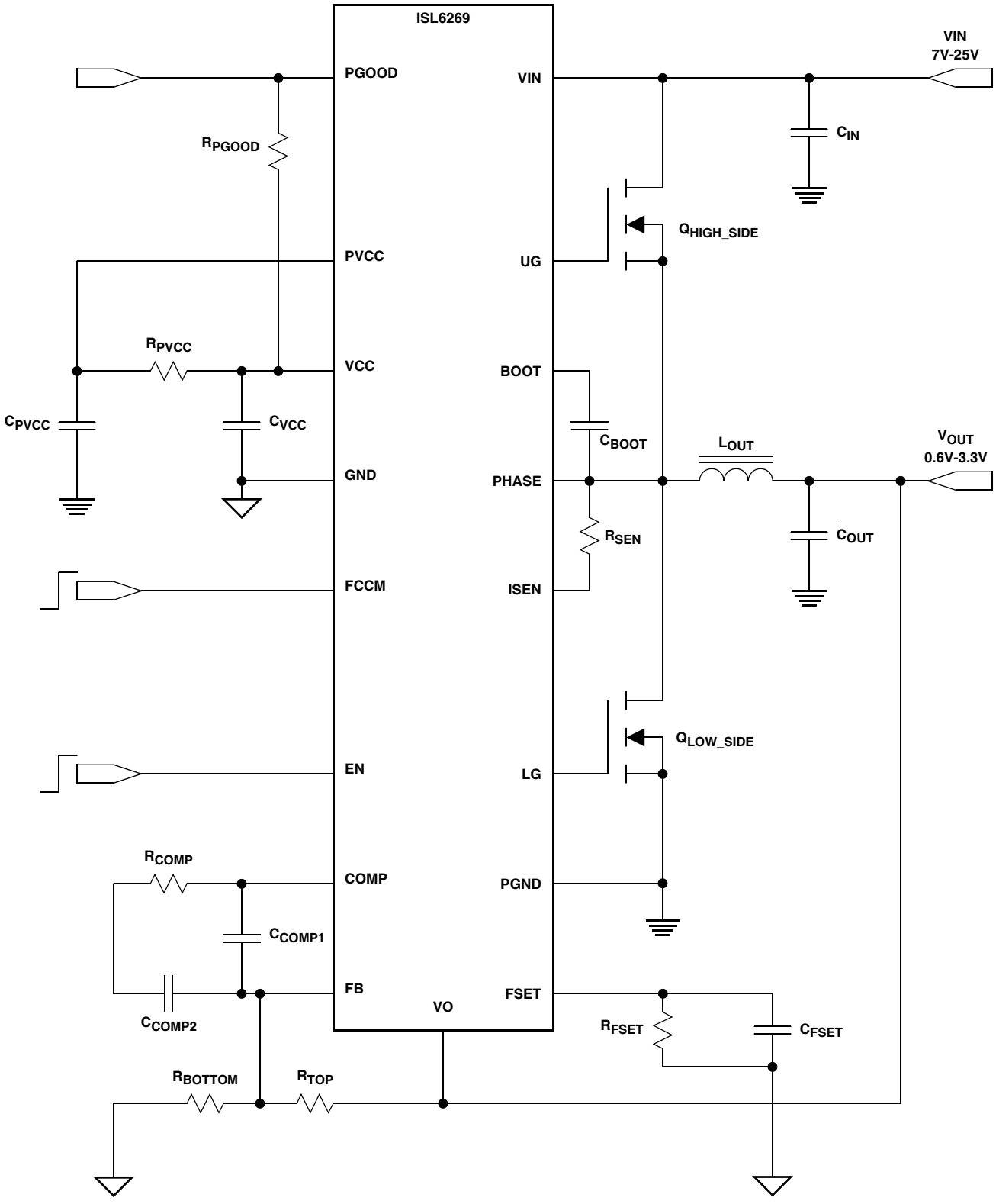


FIGURE 1. TYPICAL APPLICATION SCHEMATIC

Block Diagram

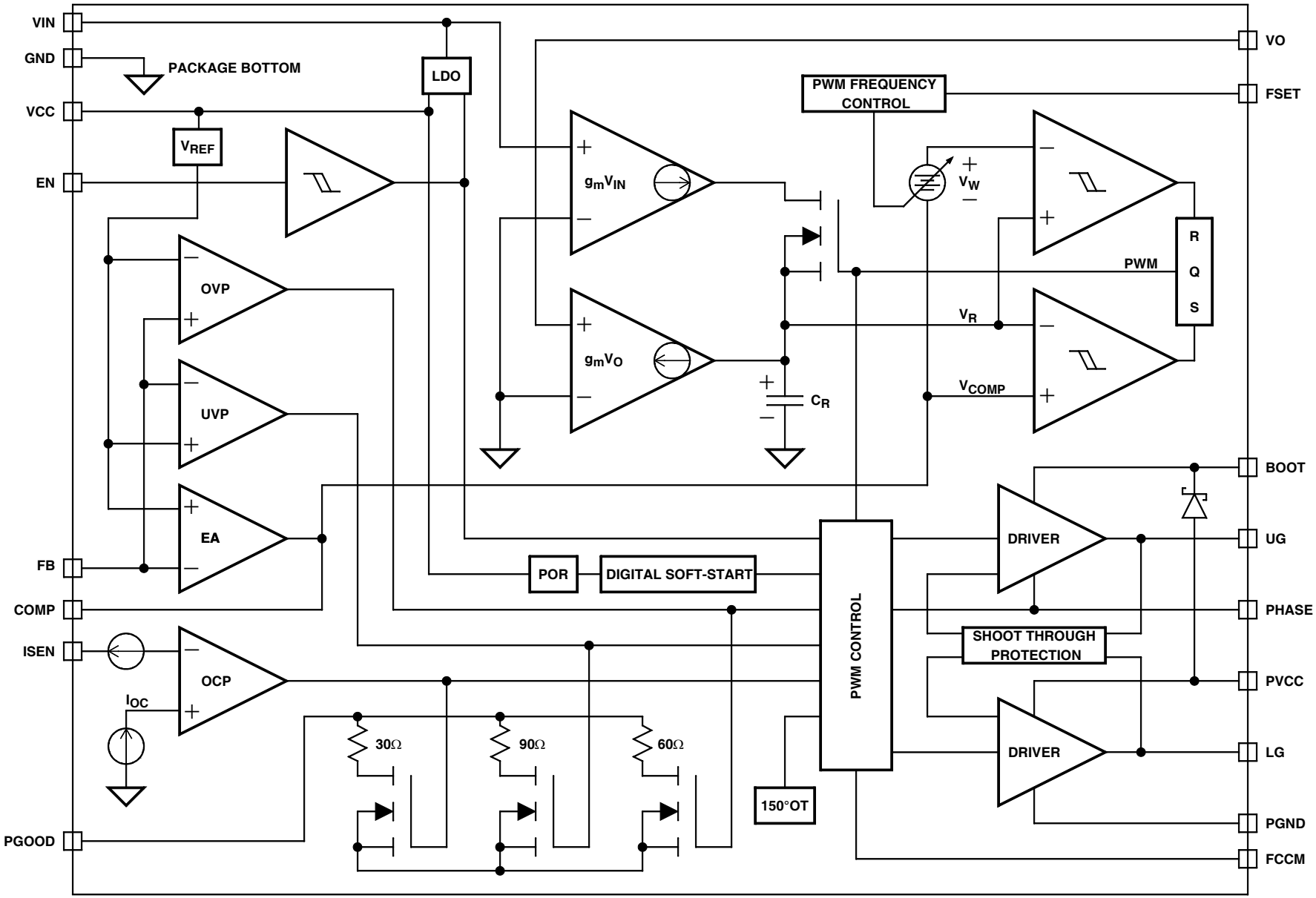


FIGURE 2. SCHEMATIC BLOCK DIAGRAM

Theory of Operation

Modulator

The ISL6269 is a hybrid of fixed frequency PWM control, and variable frequency hysteretic control. The term “Ripple” in the name “Robust-Ripple-Regulator” refers to the converter output inductor ripple current, not the converter output ripple voltage. The output voltage is regulated to 600mV at the FB pin with respect to the GND pin. The FB pin is the inverting input of the error amplifier. The frequency response of the feedback control loop is tuned with a type-two compensation network connected across the FB pin and COMP pin.

The R^3 modulator synthesizes an AC signal V_R, which is an ideal representation of the output inductor ripple current. The duty-cycle of V_R is derived from the voltage measured at the VIN pin and VO pin with respect to the GND pin. Transconductance amplifiers convert the VIN and VO voltages into currents that charge and discharge the ripple capacitor C_R. The positive slope of V_R can be written as:

$$V_{RPOS} = (gm) \cdot (V_{IN} - V_O) \quad \text{(EQ. 1)}$$

The negative slope of V_R can be written as:

$$V_{RNEG} = gm \cdot V_O \quad \text{(EQ. 2)}$$

A voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP}, creating a window-voltage envelope into which voltage V_R is compared. The V_R, V_{COMP}, and V_W signals feed into a hysteretic window comparator in which V_{COMP} is the lower threshold voltage and V_W is the higher threshold voltage. PWM pulses are generated as V_R traverses the V_W and V_{COMP} thresholds. The charging and discharging rates of capacitor C_R determine the PWM switching frequency for a given amplitude of V_W with respect to V_{COMP}. The R^3 regulator simultaneously affects switching frequency and duty cycle because it modulates both edges of the PWM pulses.

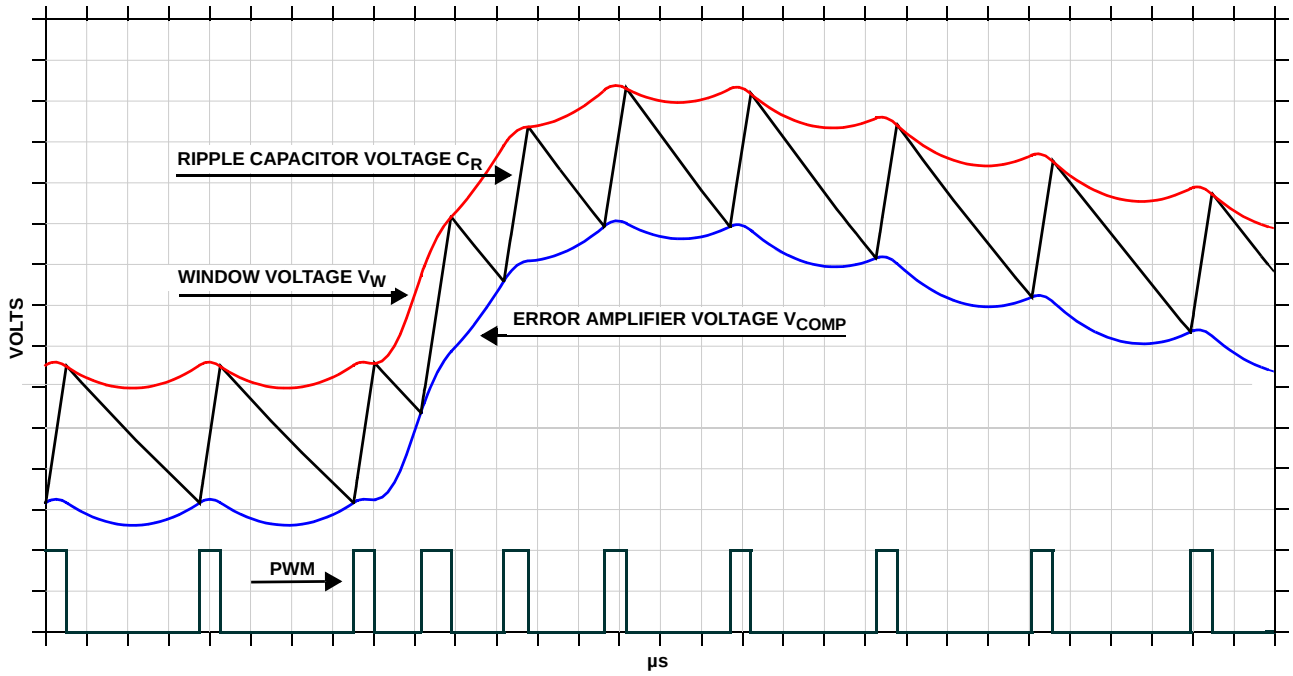


FIGURE 3. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

LDO

Voltage applied to the VIN pin with respect to the GND pin is regulated to +5VDC by an internal low-dropout voltage regulator (LDO). The output of the LDO is called V_{CC}, which is the bias voltage used by the IC internal circuitry. The LDO output is routed to the VCC pin and requires a ceramic capacitor connected to the GND pin to stabilize the LDO and to decouple load transients.

When the EN pin rises above the V_{ENR} threshold, V_{CC} will turn on and rise to its regulation voltage. The LDO regulates V_{CC} by pulling up towards the voltage at the VIN pin; the LDO has no pull-down capability.

POR and Soft-Start

The power-on reset (POR) circuit monitors V_{CC} for the V_{CCR} (rising) and V_{CCF} (falling) voltage thresholds. The purpose of soft-start is to limit the inrush current through the output capacitors when the converter first turns on.The PWM soft-start sequence initializes once V_{CC} rises above the V_{CCR} threshold, beginning from below the V_{CCF} threshold. The ISL6269 uses a digital soft-start circuit to ramp the output voltage of the converter to the programmed regulation setpoint in approximately 1.5ms. The converter regulates to 600mV at the FB pin with respect to the GND pin. During soft-start a digitally derived voltage reference forces the converter to regulate from 0V to 600mV at the FB pin.

When the EN pin is pulled below the V_{ENF} threshold, the LDO stops regulating and PWM immediately stops, regardless of the falling V_{CC} voltage. The soft-start sequence can be reinitialized and fault latches reset, once V_{CC} falls below the V_{CCF} threshold.

MOSFET Gate-Drive Outputs

The ISL6269 incorporates a MOSFET driver that controls both high-side and low-side N-Channel MOSFETS. The drivers are optimized for low duty-cycle applications prevalent with large step down voltages. At low duty-cycle, the low-side MOSFET conducts for a much longer time in a switching period than the high-side MOSFET, necessitating lower $r_{DS(ON)}$ at the expense of larger parasitic capacitance. The low-side gate driver is therefore sized much larger to meet this application requirement. The larger sink current capability enables the low-side gate driver to hold the gate-source voltage of the MOSFET below its V_{GSTH} as current conducts through the drain-to-gate parasitic capacitance. Both drivers incorporate adaptive shoot-through protection to prevent high-side and low-side MOSFETS from conducting simultaneously and shorting the input supply. During turn-off of the low-side MOSFET, the LG to PGND voltage is monitored until it reaches a 1V threshold, at which time the UG driver is allowed to switch. During turn-off of the high-side MOSFET, the UG to PHASE voltage is monitored until it reaches a 1V threshold, at which time the LG driver is allowed to switch.

The input power for the LG driver circuit is sourced directly from the PVCC pin. The input power for the UG driver circuit is sourced from a “boot” capacitor connected from the BOOT pin to the PHASE pin. The same supply that is connected to the PVCC pin is used to charge the boot capacitor via the internal Schottky diode of the IC.

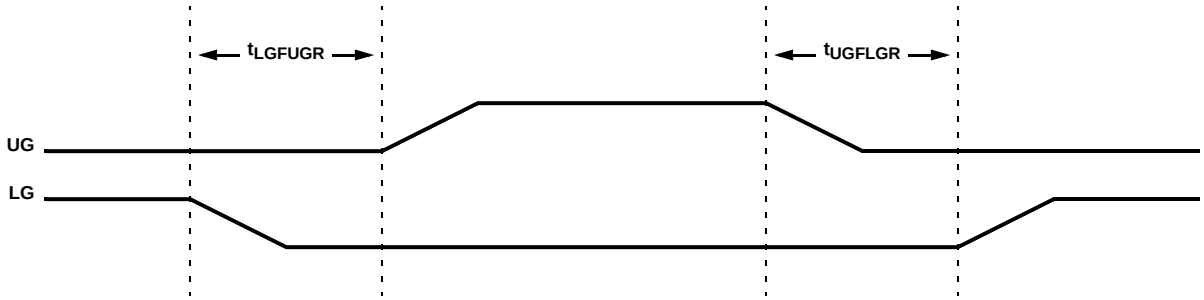


FIGURE 4. GATE DRIVE TIMING DIAGRAM

Diode Emulation

Positive inductor current can flow *from* the source of the high-side MOSFET or *from* the drain of the low-side MOSFET. Negative inductor current flows *into* the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the GND pin. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the GND pin. Negative inductor current occurs when the output load current is less than ½ the inductor ripple current.

The ISL6269 can be configured to operate in forced-continuous-conduction-mode (FCCM) or in diode-emulation-mode (DEM), which can improve light-load efficiency. In FCCM, the controller always operates as a synchronous rectifier, switching the low-side MOSFET regardless of the polarity of the output inductor current. In DEM, the low-side MOSFET is disabled during negative current flow from the output inductor. DEM is permitted when the FCCM pin is pulled low, and disabled when pulled high.

When DEM is permitted, the converter will automatically select FCCM or DEM according to load conditions. If positive PHASE pin voltage is measured for eight consecutive PWM pulses, then the converter will enter diode-emulation mode on the next PWM cycle. If a negative PHASE pin voltage is measured, the converter will exit DEM on the following PWM pulse. An audio filter is incorporated into the PWM generation circuitry that prevents the switching frequency from entering the audible spectrum at low load conditions.

Overcurrent and Short-Circuit Protection

When an OCP or SCP fault is detected, the ISL6269 overcurrent and short-circuit protection circuit will pull the PGOOD pin low and latch off the converter. The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN pin is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold. Selecting the appropriate value of resistor R_{SEN} programs the OCP threshold. The resistor R_{SEN} is connected from the ISEN pin to the PHASE pin. The PHASE pin is connected to the drain terminal of the low-side MOSFET.

The OCP circuit measures positive-flowing, peak-current through the output inductor, not the DC current flowing from the converter to the load. The low-side MOSFET drain current is assumed to be equal to the positive output inductor current when the high-side MOSFET is turn off. Current briefly conducts through the low-side MOSFET body diode until the LG driver goes high. The peak inductor current develops a voltage across the $r_{DS(ON)}$ of the low-side MOSFET just as if it were a discrete current-sense resistor. An OCP fault will occur when the ISEN pin has measured more than the OCP threshold current $I_{OC,}$ on consecutive PWM pulses, for a period exceeding 20µs. It does not matter how many PWM pulses are measured during the 20µs period. If a measurement falls below I_{OC} before 20µs has elapsed, then the timer is reset to zero. An SCP fault will occur when the ISEN pin has measured more than the short-circuit threshold current $I_{SC,}$ in less than 10µs, on consecutive PWM pulses. The relationship between I_D and I_{SEN} can be written as:

$$-I_{SEN} \cdot R_{SEN} = -I_D \cdot r_{DS(ON)} \quad \text{(EQ. 3)}$$

The value of RSEN can then be written as:

$$R_{SEN} = \frac{\left[I_{FL} + \frac{I_{PP}}{2}\right] \cdot OC_{SP} \cdot r_{DS(ON)}}{I_{OC}} \quad \text{(EQ. 4)}$$

Where:

- R_{SEN} (Ω) is the resistor used to program the over-current setpoint
- I_{SEN} is the current sense current that is sourced from the ISEN pin
- I_{OC} is the I_{SEN} threshold current value sourced from the ISEN pin that will activate the OCP circuit
- I_{FL} is the maximum continuous DC load current
- I_{PP} is the inductor peak-to-peak ripple current
- OC_{SP} is the desired overcurrent setpoint expressed as a multiplier relative to I_{FL}

Overvoltage

When an OVP fault is detected, the ISL6269 overvoltage protection circuit will pull the PGOOD pin low and latch off the converter. The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN pin is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

When the voltage at the FB pin relative to the GND pin, has exceeded the rising overvoltage threshold V_{OVR}, the converter will latch off however, the LG driver output will stay high, forcing the low-side MOSFET to pull-down the output voltage of the converter. The low-side MOSFET will continue to pull-down the output voltage until the voltage at the FB pin relative to the GND pin, has decayed below the falling overvoltage threshold $V_{OVF,}$ at which time the LG driver output is driven low, forcing the low-side MOSFET off. The LG driver output will continue to switch on at V_{OVR} and switch off at V_{OVF} until the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

Undervoltage

When an UVP fault is detected, the ISL6269 undervoltage protection circuit will pull the PGOOD pin low and latch off the converter. The UVP fault occurs when the voltage at the FB pin relative to the GND pin, has fallen below the undervoltage threshold V_{UV}. The fault will remain latched until the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold.

Over-Temperature

When an OTP fault is detected, the ISL6269 over-temperature protection circuit suspends PWM, but will not affect the PGOOD pin, or latch off the converter. The over-temperature protection circuit measures the temperature of the silicon and activates when the rising threshold temperature T_{OTR} has been exceeded. The PWM remains suspended until the silicon temperature falls below the temperature hysteresis T_{OTHYS} at which time normal operation is resumed. All other protection circuits will function normally during OTP however, since PWM is inhibited, it is likely that the converter will immediately experience an undervoltage fault, latch off, and pull PGOOD low. If the EN pin is pulled below V_{ENF} or if the voltage at the VIN is reduced to the extent that V_{CC} has fallen below the POR V_{CCF} threshold, normal operation will resume however, the temperature hysteresis T_{OTHYS} is reset.

PGOOD

The PGOOD pin connects to three open drain MOSFETS each of which has a different $r_{DS(ON)}$. Consult the Electrical Specifications Table for the pull-down resistance of PGOOD for the corresponding fault. The PGOOD pin is high impedance whenever V_{CC} is below the rising POR threshold V_{OVR}, the falling POR threshold V_{OVF}, after delay T_{SS} elapses, without an OVP, OCP, SCP, or UVP fault. This fault-identification capability is a useful tool for trouble-shooting.

TABLE 1. PGOOD PULL-DOWN RESISTANCE

CONDITION	PGOOD RESISTANCE
IC Off	Open
Soft Start	95Ω
Undervoltage Fault	95Ω
Overvoltage Fault	60Ω
Overcurrent Fault	30Ω

Component Selection

Programming the Output Voltage

When the converter is in regulation there will be 600mV from the FB pin to the GND pin. Connect a two-resistor voltage divider across the VO pin and the GND pin with the output node connected to the FB pin. Scale the voltage-divider network such that the FB pin is 600mV with respect to the GND pin when the converter is regulating at the desired output voltage.

Programming the output voltage can be written as:

$$V_{REF} = V_{OUT} \cdot \frac{R_{BOTTOM}}{R_{TOP} + R_{BOTTOM}} \quad \text{(EQ. 5)}$$

Where:

- V_{OUT} is the desired output voltage of the converter.
- V_{REF} is the voltage that the converter regulates to at the FB pin.
- R_{TOP} is the voltage-programming resistor that connects from the FB pin to the VO pin. It is usually chosen to set the gain of the control-loop error amplifier. It follows that R_{BOTTOM} will be calculated based upon the already selected value of R_{TOP}.
- R_{BOTTOM} is the voltage-programming resistor that connects from the FB pin to the GND pin.

Calculating the value of R_{BOTTOM} can now be written as:

$$R_{BOTTOM} = \frac{V_{REF} \cdot R_{TOP}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 6)}$$

Programming the PWM Switching Frequency

The PWM switching frequency F_{OSC} is programmed by the resistor R_{FSET} that is connected from the FSET pin to the GND pin. Programming the approximate PWM switching frequency can be written as:

$$F_{OSC} = \frac{1}{60 \cdot R_{FSET} \cdot [1 \times 10^{-12}]} \quad \text{(EQ. 7)}$$

Estimating the value of R_{FSET} can now be written as:

$$R_{FSET} = \frac{1}{60 \cdot F_{OSC} \cdot [1 \times 10^{-12}]} \quad \text{(EQ. 8)}$$

Where:

- F_{OSC} is the PWM switching frequency.
- R_{FSET} is the F_{OSC} programming resistor.
- 60 x [1 x 10^{-12}] is a constant.

Selection of the LC Output Filter

The duty cycle of a buck converter is ideally a function of the input voltage and the output voltage. This relationship can be written as:

$$D(V_{IN}) = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 9)}$$

Where:

- D is the PWM duty cycle.
- V_{IN} is the input voltage to be converted.
- V_{OUT} is the regulated output voltage of the converter.

The output inductor peak-to-peak ripple current can be written as:

$$I_{PP} = \frac{V_{OUT} \cdot [1 - D(V_{IN})]}{F_{OSC} \cdot L_O} \quad \text{(EQ. 10)}$$

Where:

- I_{PP} is the peak-to-peak output inductor ripple current.
- F_{OSC} is the PWM switching frequency.
- L_O is the nominal value of the output inductor.

A typical step-down DC/DC converter will have an I_{PP} of 20% to 40% of the nominal DC output load current. The value of I_{PP} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistance the inductor winding, DCR. The DC copper loss of the inductor can be estimated by:

$$P_{COPPER} = [I_{LOAD}]^2 \cdot DCR \quad \text{(EQ. 11)}$$

The inductor copper loss can be significant in the total system power loss. Attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{PP} can flow. Current I_{PP} develops a corresponding ripple voltage V_{PP} across C_O, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages can be written as:

$$\Delta V_{ESR} = I_{PP} \cdot ESR \quad \text{(EQ. 12)}$$

and

$$\Delta V_C = \frac{I_{PP}}{8 \cdot C_O \cdot F_{OSC}} \quad \text{(EQ. 13)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to adjust the ESR to achieve the required V_{PP}. The inductance of the capacitor can cause a brief voltage dip when the load transient has an extremely high slew rate. Low inductance capacitors constructed with reverse package geometry are available.

A capacitor dissipates heat as a function of RMS current. Be sure that I_{PP} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current. Take into account that the specified value of a capacitor can drop as much as 50% as the DC voltage across it increases.

Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. For most cases, the RMS current rating requirement for the input capacitors of a buck regulator is approximately 1/2 the DC output load current. The maximum RMS current required by the regulator can be approximated through the following equation:

$$I_{RMS} = I_{LOAD} \cdot \sqrt{[D] - [D]^2} \quad \text{(EQ. 14)}$$

Where:

- D is the converter duty cycle.
- I_{RMS} is the input capacitance RMS ripple current.
- I_{LOAD} is the converter output DC load current.

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain terminal of the high-side MOSFET and the source terminal of the low-side MOSFET, in order to reduce the voltage ringing created by the switching current across parasitic circuit elements.

MOSFET Selection and Considerations

Typically, MOSFETS cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETS used in the power conversion stage of the converter should have a maximum V_{DS} rating that exceeds the upper voltage tolerance of the input power source, and the voltage spike that occurs when the MOSFET switches off. Placing a low ESR ceramic capacitor as close as practical across the drain of the high-side MOSFET and the source of the low-side MOSFET will reduce the amplitude of the turn-off voltage spike.

The MOSFET input capacitance C_{ISS}, and on-state drain to source resistance $r_{DS(ON)}$, are to an extent, inversely related; reduction of $r_{DS(ON)}$ typically results in an increase of C_{ISS}. These two parameters affect the efficiency of the converter in different ways. The $r_{DS(ON)}$ affects the power loss when the MOSFET is completely turned on and conducting current. The C_{ISS} affects the power loss when the MOSFET is actively switching. Switching time increases as C_{ISS} increases. When the MOSFET switches it will briefly conduct current while the drain to source voltage is still present. The power dissipation during this time is substantial so it must be kept as short as practical. Often the high-side MOSFET and the low-side MOSFET are different devices due to the trade-offs that have to be made between C_{ISS} and $r_{DS(ON)}$.

The low-side MOSFET power loss is dominated by $r_{DS(ON)}$ because it conducts current for the majority of the PWM switching cycle; the $r_{DS(ON)}$ should be small. The switching loss is small for the low-side MOSFET even though C_{ISS} is large due to the low $r_{DS(ON)}$ of the device, because the drain to source voltage is clamped by the body diode. The high-side MOSFET power loss is dominated by C_{ISS} because it conducts current for the minority of the PWM switching cycle; the C_{ISS} should be small. The switching loss of the high-side MOSFET is large compared to the low-side MOSFET because the drain to source voltage is not clamped. For the lower MOSFET, its power loss can be

assumed to be the conduction loss only and can be written as:

$$P_{CONLS}D(V_{IN}) \approx [I_{LOAD}]^2 \cdot r_{DS(ON)LS} \cdot [1 - D(V_{IN})] \quad \text{(EQ. 15)}$$

For the high-side MOSFET, its conduction loss can be written as:

$$P_{CONHS}D(V_{IN}) = [I_{LOAD}]^2 \cdot r_{DS(ON)HS} \cdot D(V_{IN}) \quad \text{(EQ. 16)}$$

For the high-side MOSFET, its switching loss can be written as:

$$P_{SWHS}(V_{IN}) = \frac{V_{IN} \cdot I_{VAL} \cdot T_{ON} \cdot F_{OSC}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot T_{OFF} \cdot F_{OSC}}{2} \quad \text{(EQ. 17)}$$

The peak and valley current of the inductor can be obtained based on the inductor peak-to-peak current and the load current. The turn-on and turn-off time can be estimated with the given gate driver parameters in the Electrical Specification Table.

Selecting The Bootstrap Capacitor

The selection of the bootstrap capacitor can be written as:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 18)}$$

Where:

- Q_g is the total gate charge required to switch the high-side MOSFET
- ΔV_{BOOT}, is the maximum allowed voltage decay across the boot capacitor each time the MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate charge Q_G, of 25nC at V_{GS} = 5V, and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; select at least the first standard component value of greater capacitance than calculated, that being 0.15µF. Use an X7R or X5R ceramic capacitor.

Layout Considerations

Power and Signal Layer Placement on the PCB

As a general rule, power layers should be adjacent to one another towards one side of the board, with signal layers adjacent to one another towards the opposite side of the board. For example, prospective layer arrangement on a 4 layer board is shown below:

1. Top Layer: ISL6269 signal lines
2. Signal Ground
3. Power Layers: Power Ground
4. Bottom Layer: Power MOSFET, Inductors and other Power traces

It is a good engineering practice to separate the power conductors from the signal conductors. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces. The loop formed by the bottom MOSFET, output inductor, and output capacitor, should be very small.

A guard-ring placed around high impedance inputs FB and FSET is recommended.

Component Placement

Power MOSFETs should be placed close to the IC so that VIN, LG, UG, PHASE, BOOT, and ISEN traces can be short.

Place components in such a way that the area near the FSET, FB, COMP, and VO pins avoid traces with high dv/dt and di/dt, such as gate signals and phase node signals.

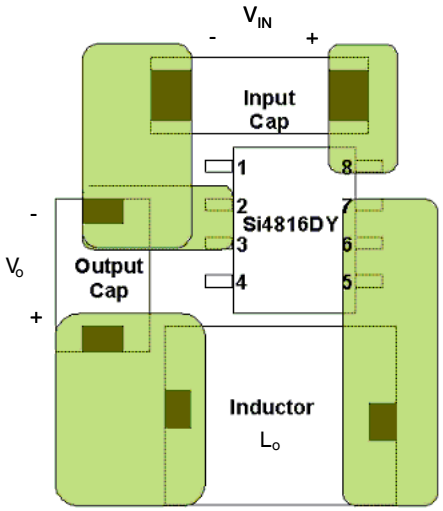


FIGURE 5. TYPICAL POWER COMPONENT PLACEMENT

Signal Ground and Power Ground Connection

The bottom of the ISL6269 QFN package is the analog and logic ground terminal (GND) of the IC. Connect the GND pad of the ISL6269 to the signal ground layer of the pcb using at least five vias, for a robust thermal and electrical conduction path. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitors that is not in the return path of the inductor ripple current flowing through the output capacitors.

Pin 1 (VIN)

The VIN pin should be connected to the drain of the high-side MOSFET, using a low resistance and low inductance path.

Pin 2 VCC

For best performance the LDO requires at least a 1µF MLCC decouple capacitor connected from the VCC pin to the GND pin.

Pin 3 (FCCM) and Pin 4 (EN)

These are logic inputs that are referenced to the GND pin. Treat as a typical logic signal.

Pin 5 (COMP)

The loop compensation components connect from the COMP pin to the FB pin. Place the components close to the FB pin to make the traces as short as possible.

Pin 6 (FB)

There is usually a resistor divider connecting the output voltage of the converter to the FB pin. The correct layout should bring the output voltage from the regulation point to the FB pin with kelvin traces. The input impedance of the FB pin is high, so place the resistor divider close to the pin, keeping the high impedance trace short.

Pin 7 (FSET)

This pin requires a quiet environment. The resistor R_{FSET} and capacitor C_{FSET} should be placed directly adjacent to this pin. Keep fast moving nodes away from this pin.

Pin 8 (VO)

The VO pin should be connected to the Kelvin traces at the FB voltage divider.

Pin 9 (ISEN)

The ISEN trace should be routed away from the traces and components connected to the FB pin, COMP pin, and FSET pin.

Pin 10 (PGND)

This is the pull-down return path for the LG low-side MOSFET gate drive. This should be an isolated low-resistance, low-inductance trace that connects to the source of the low-side MOSFET.

Pin 11 (LG)

Connect to the gate terminal of the low-side MOSFET. The signal going through this trace is both high dv/dt and high di/dt, with high peak charging and discharging current. Route this trace in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in parallel with these traces on any layer.

Pin 12 (PVCC)

A ceramic decoupling capacitor connects from the PVCC pin to the PGND pin, not the GND pin. Closely place the capacitor on the same side of the board as the ISL6269 IC.

Pin 13 (BOOT)

The di/dt and dv/dt of this pin are as high as that of the LG pin, UG pin, and the PHASE pin; therefore, the traces should be as short as possible.

Pin 14 (UG)

Connect to the gate terminal of the high-side MOSFET. The signal going through this trace is both high dv/dt and high di/dt, with high peak charging and discharging current. Route this trace in parallel with the trace from the PHASE pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in parallel with these traces on any layer.

Pin 15 (PHASE)

Connect to the low-side MOSFET drain terminal. The phase node has a very high dv/dt with a voltage swing from the input voltage to ground. This trace should be short, and positioned away from other weak signal traces.

Pin 16 (PGOOD)

A very robust pin. Treat as a typical logic signal.

Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. If ringing is excessive, it could easily affect current sample information. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

Identify the Power and Signal Ground

The input and output capacitors of the converter, the source terminal of the low-side MOSFET, and the PGND pin should be closely connected to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at the negative terminal of the output capacitors.

Decoupling Capacitor for Switching MOSFET

Ceramic capacitors should be closely connected to the drain side of the high-side MOSFET, and the source of the low-side MOSFET. This capacitor reduces the amplitude of the turn-off voltage spike.

Control Loop

The control loop model of the ISL6269 is partitioned into function blocks consisting of:

- The Duty cycle to Vo transfer function $G_{vd}(s)$ which is determined by the value of the output power components, input voltage, and output voltage.
- The Vcomp to Duty cycle transfer function $F_m(s)$ which is determined by the PWM frequency, input voltage, output voltage, resistor R_{FSET}, and capacitor C_{FSET}.
- The product of the $G_{vd}(s)$ and $F_m(s)$ transfer functions is expressed as the Vcomp to Vo transfer function $G_{vovc}(s)$.
- The type-two compensation network $G_{comp}(s)$ that connects across the COMP and FB pins.
- The product of the $G_{comp}(s)$ and $G_{vovc}(s)$ transfer functions is expressed as the loop transfer function T(s).

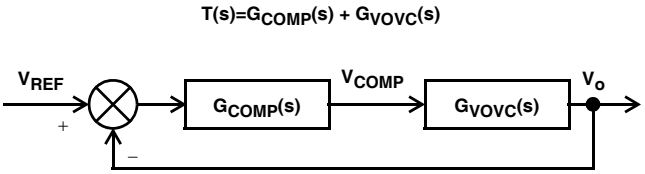


FIGURE 6. SYSTEM CONTROL BLOCK DIAGRAM

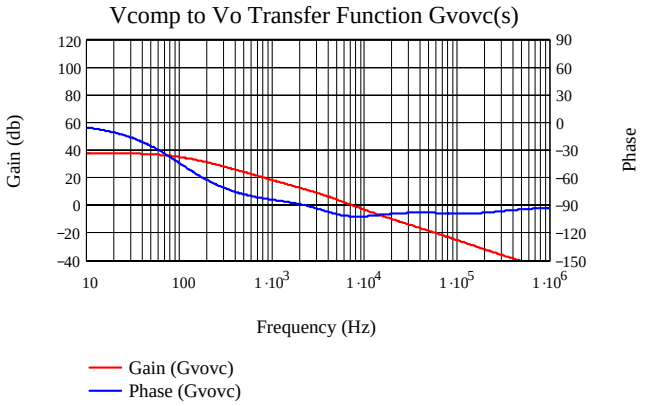


FIGURE 7. OPEN LOOP TRANSFER FUNCTION

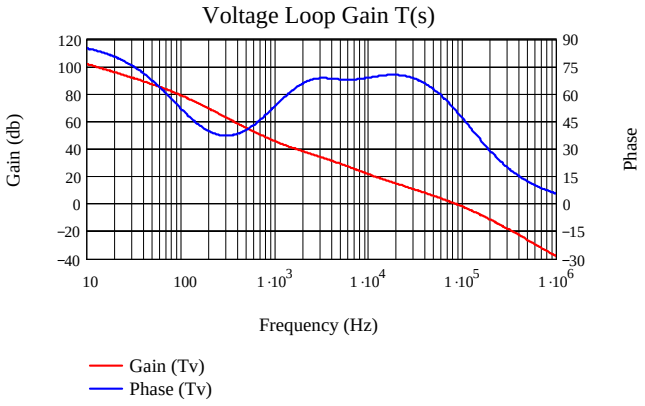


FIGURE 8. CLOSED LOOP TRANSFER FUNCTION

The compensator zero *fz1* is written as:

$$\omega_{z1} = \frac{1}{R_{comp} \cdot C_{comp2}} \quad \text{(EQ. 19)}$$

$$f_{z1} = \frac{\omega_{z1}}{2 \cdot \pi} \quad \text{(EQ. 20)}$$

The compensator pole *fp1* is written as:

$$\omega_{p1} = \left[\frac{1}{C_{comp1}} + \frac{1}{C_{comp2}}\right] \cdot \frac{1}{R_{comp}} \quad \text{(EQ. 21)}$$

$$f_{p1} = \frac{\omega_{p1}}{2 \cdot \pi} \quad \text{(EQ. 22)}$$

The compensator gain is written as:

$$\omega_i = \frac{1}{R_{comp} \cdot [C_{comp1} + C_{comp2}]} \quad \text{(EQ. 23)}$$

The compensator transfer function is written as:

$$G_{comp}(s) = \frac{\omega_i \cdot \left[1 + \frac{s}{\omega_{z1}}\right]}{s \cdot \left[1 + \frac{s}{\omega_{p1}}\right]} \quad \text{(EQ. 24)}$$

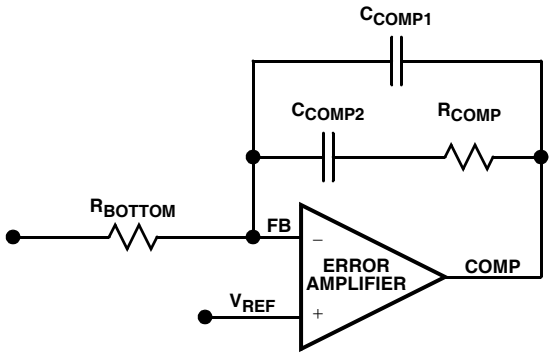
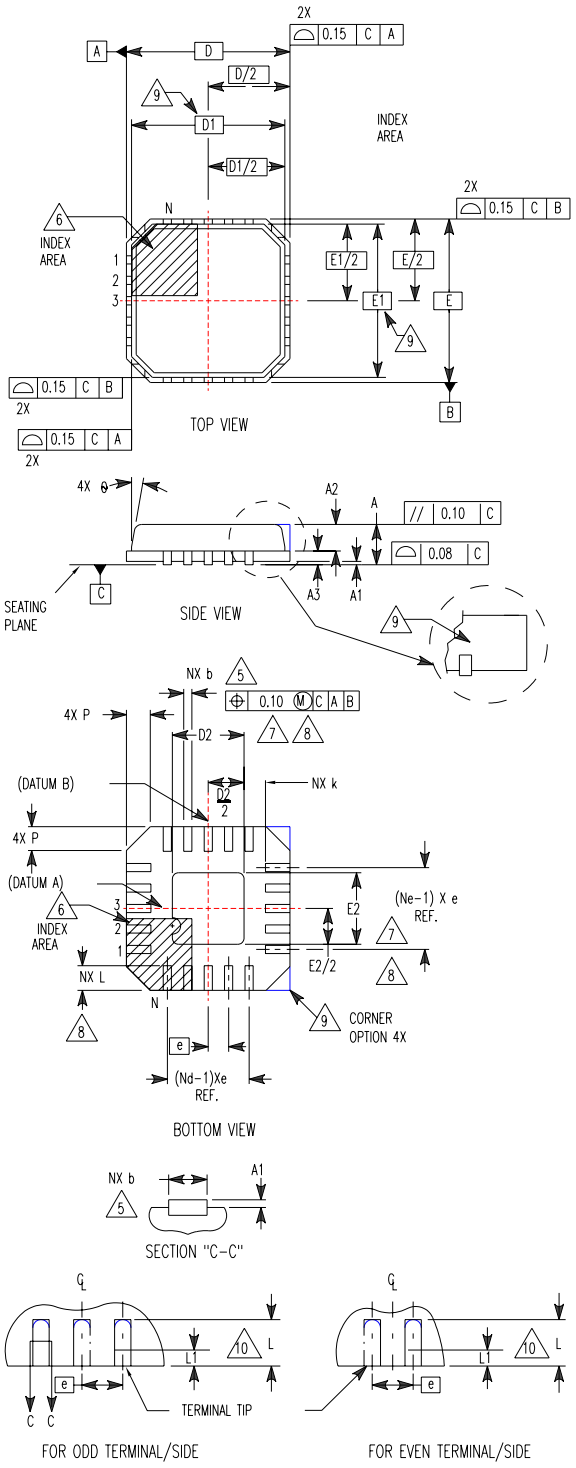


FIGURE 9. SYSTEM CONTROL BLOCK DIAGRAM

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerances conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.