/VI/IXI/VI

Quad, High-Side Power Switch

<div style="text-align: right">MAX625</div>

General Description

The MAX625 is a quad, high-side power switch that switches 1A steady-state loads with 4A peak currents. The switch resistances are typically 0.2Ω, and internal clamp diodes allow inductive load switching. The MAX625 is completely self-contained in a 24-pin, 0.300" narrow plastic DIP package and requires no external components for normal operation.

The +4.5V to +16.5V input supply range and a typical quiescent current of only 70μA make the MAX625 ideal for a wide range of line- and battery-powered switching and control applications that require high efficiency and small size.

An internal quad latch accepts four TTL/CMOS logic signals that control the four switches. The MAX625 eliminates expensive logic MOSFETs in +5V-only and other low-voltage switching circuits. It also replaces costly, bulky, less efficient P-channel MOSFETs or PNP transistors.

Applications

Portable Computer Battery-Load Management

High-Side Power, N-Channel MOSFET Switching

Low-Side Switching from Low Supply Voltages

Solid-State Relay

Quad-Latching Level Translators
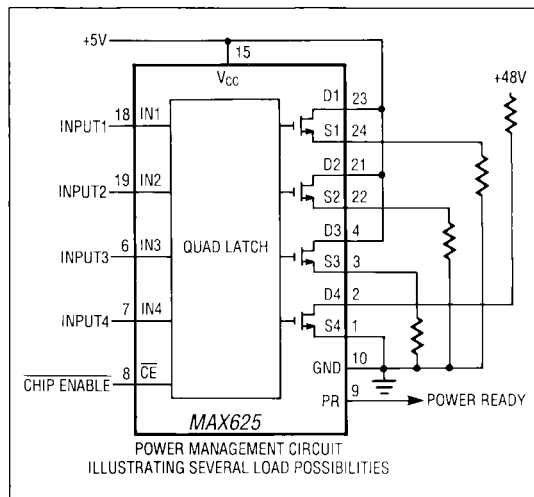
H-Bridge Motor Drivers

Stepper Motor Drivers
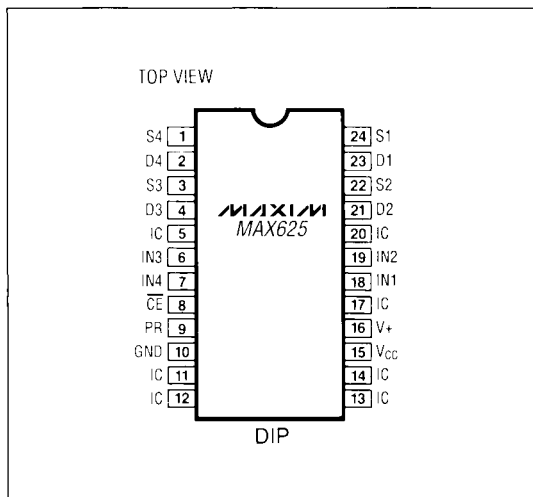
Features

♦ **0.2Ω Max Switch Resistance**

♦ **+4.5V to +16.5V Operating Supply Voltage Range**

♦ **Output Voltage Regulated to V_{CC} + 11V (Typ) Available at V+**

♦ **70μA Quiescent Current (Typ)**

♦ **Quad Latched TTL/CMOS Inputs**

♦ **Power-Ready Output**

♦ **Undervoltage Lockout**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX625CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX625ENG	-40°C to +85°C	24 Narrow Plastic DIP

Pin Configuration

DIP

Typical Operating Circuit

POWER MANAGEMENT CIRCUIT
ILLUSTRATING SEVERAL LOAD POSSIBILITIES

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ABSOLUTE MAXIMUM RATINGS

V_{CC} 17V
V+ to GND 30V
IN1–IN4, $\overline{CE}$ .... (GND – 0.3V) to (V+ + 0.3V)
Power Ready (PR) Output ... (GND – 0.3V) to (V_{CC} + 0.3V)
V+ Output Current 25mA
Drain-to-Source Breakdown Voltage 60V
Continuous Drain to Source Current
  Single MOSFET 5A
  All four MOSFETs 1.2A

Continuous Total Power Dissipation
  to +70°C 1067mW
  derate above +70°C .... 13.33mW/°C
Operating Temperature Ranges:
  MAX625CNG .... 0°C to +70°C
  MAX625ENG .... –40°C to +85°C
Storage Temperature Range .... –65°C to +160°C
Lead Temperature (soldering, 10 sec) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}			4.5		16.5	V
Internal MOSFET ON Resistance (Note 2)	$R_{DS(ON)}$	T_A = +25°C V_{CC} = 4.5V to 16.5V (High-side)			150	200	mΩ
		T_A = +25°C V_{CC} = 4.5V to 8V (Low-side)			140	200	
		T_A = T_{MIN} to T_{MAX} V_{CC} = 4.5V to 16.5V (High-side)				260	
		T_A = T_{MIN} to T_{MAX} V_{CC} = 4.5V to 8V (Low-side)				260	
Off Leakage Current	$I_{DS(OFF)}$	V_{DS} = 55V			0.05	1.0	µA
High-Side Voltage (Note 3)	V+	I_{OUT} = 0, V_{CC} = +4.5V		14.5	15.5	17.5	V
		I_{OUT} = 0, V_{CC} = 16.5V		26.5	27.5	29.5	
		I_{OUT} = 250µA, V_{CC} = 5V		15	16	18	
		I_{OUT} = 500µA, V_{CC} = 16.5V		26.5	27.5	29.5	
Power-Ready Threshold	PRT	I_{OUT} = 100µA Sink (Note 4)		12	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100µA		3.8	4.7	5	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA			0.1	0.4	V
Switching Frequency	f_O	I_{OUT} = 0, T_A = +25°C			70		kHz
Quiescent Supply Current	I_Q	T_A = +25°C, I_{OUT} = 0	V_{CC} = 16.5V		50	350	µA
			V_{CC} = 5V		70	500	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

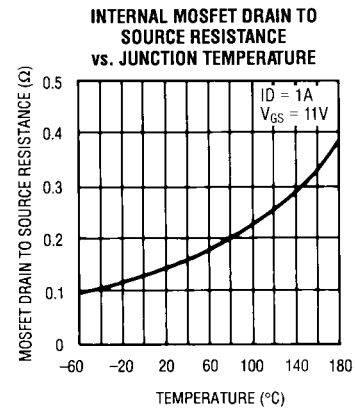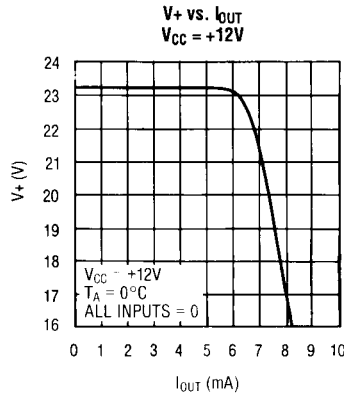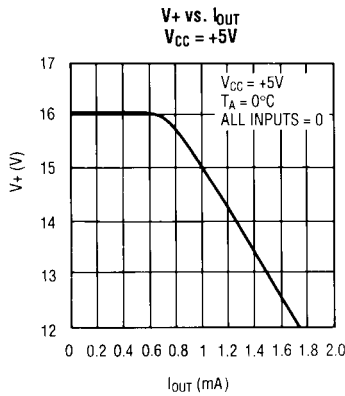| PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Inputs						
Input Threshold Low	V_{TL}				0.8	V
Input Threshold High	V_{TH}		2.4			V
Input Bias Current	I_B	0V < V_{IN} < 5V	-100		+100	nA
Chip Enable Threshold Low	CE_{LO}				0.8	V
Chip Enable Threshold High	CE_{HI}		2.4			V
Minimum CE Pulse Duration	t_{CE}		100	50		ns
Pull-Down Current	I_{CE}			10		µA
Data Hold Time	t_{DH}			-10	+10	ns
Data Set-Up Time	t_{SU}			50	100	ns
Data Delay Time	t_{OD}	V_{CE} = 0V		150		ns

Note 1: To avoid exceeding the maximum V_{GS} rating of the internal N-channel MOSFET switches, V_{CC} must not exceed +8V in low-side switching applications.

Note 2: A "low-side" switch connects between the load and ground.
A "high-side" switch connects between the voltage source and load.

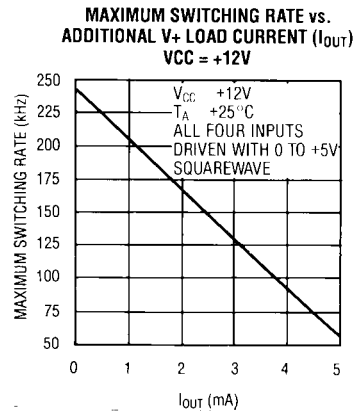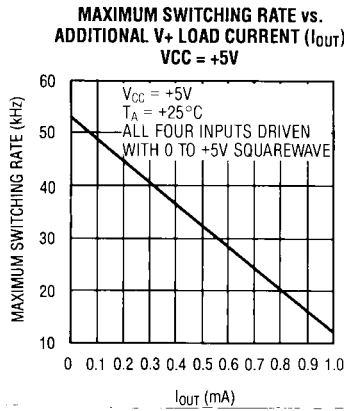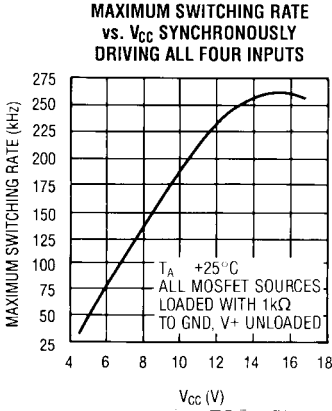**Note 3:** The High-Side Voltage (V+) is measured with respect to ground.

Note 4: Power Ready Threshold is the voltage measured with respect to ground at V+ when PR switches high (PR HIGH = V_{CC}).
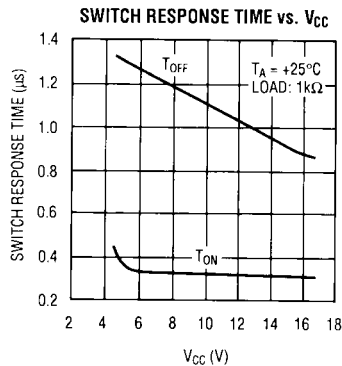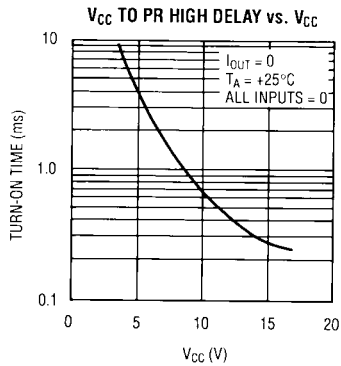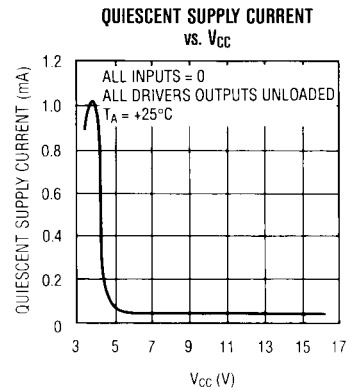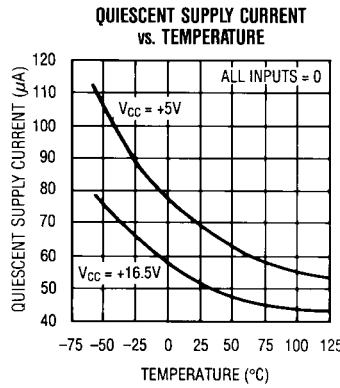
Typical Operating Characteristics

V+ vs. I_{OUT}
V_{CC} = +5V

V+ vs. I_{OUT}
V_{CC} = +12V

INTERNAL MOSFET DRAIN TO SOURCE RESISTANCE vs. JUNCTION TEMPERATURE

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MAXIMUM SWITCHING RATE vs. V_CC SYNCHRONOUSLY DRIVING ALL FOUR INPUTS

MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (I_{OUT}) VCC = +5V

MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (I_{OUT}) VCC = +12V

NOTE: THE MAXIMUM SWITCHING RATE OCCURS JUST BELOW THE POINT WHERE DRIVER OUTPUT AND V+ LOADING PULLS V+ TO PRT (PRT - V_{CC} + 8.5V).

V+ RIPPLE vs. V_CC

QUIESCENT SUPPLY CURRENT vs. TEMPERATURE

QUIESCENT SUPPLY CURRENT vs. V_CC

V_CC TO PR HIGH DELAY vs. V_CC

SWITCH RESPONSE TIME vs. V_CC
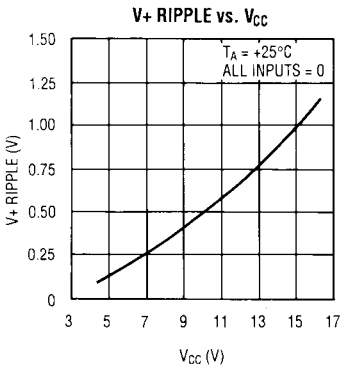
NOTE: MEASURED FROM THE DRIVER INPUT EDGE TO THE POINT WHERE THE SWITCH IS FULLY ON OR OFF

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PIN	NAME	FUNCTION
1	S4	MOSFET Source 4.
2	D4	MOSFET Drain 4.
3	S3	MOSFET Source 3.
4	D3	MOSFET Drain 3.
5	IC	Internal Connection. Make no connection to this pin.
6	IN3	TTL/CMOS Compatible Input to Switch 3. Connect to GND if unused.
7	IN4	TTL/CMOS Compatible Input to Switch 4. Connect to GND if unused.
8	CE	Chip Enable. Logic high inhibits input data. Logic low transfers data to switches. CE pulse must be at least 100ns. Connect to GND for direct data transfer.
9	PR	Power-Ready Output is a logic high equal to V_{CC} when V+ ≥ V_{CC} + 8.5V.
10	GND	Ground.
11	IC	Internal Connection. Make no connection to this pin.
12	IC	Internal Connection. Make no connection to this pin.

PIN	NAME	FUNCTION
13	IC	Internal Connection. Make no connection to this pin.
14	IC	Internal Connection. Make no connection to this pin.
15	V_{CC}	Supply Voltage. Connect to positive supply.
16	V+	High-side voltage out. Typically equal to V_{CC} + 11V.
17	IC	Internal Connection. Make no connection to this pin.
18	IN1	TTL/CMOS Compatible input to switch 1. Connect to GND if unused.
19	IN2	TTL/CMOS Compatible input to switch 2. Connect to GND if unused.
20	IC	Internal Connection. Make no connection to this pin.
21	D2	MOSFET Drain 2.
22	S2	MOSFET Source 2.
23	D1	MOSFET Drain 1.
24	S1	MOSFET Source 1.

Detailed Description

Figure 1 shows the MAX625 functional block diagram. A regulated multistage charge pump supplies four MOSFET drivers with V_{CC} + 11V for driving the internal MOSFETs (Figure 2). Logic inputs to the four drivers are stored in a quad latch. Data is latched by pulling CE high. An undervoltage lockout prevents the internal MOSFETs from turning on until V+ reaches the Power Ready Threshold (PRT) voltage (V_{CC} + 8.5V) and V_{CC} is greater than +3V.

The Dual-Charge Pump

A high-side voltage of approximately V_{CC} + 11V is generated by a multistage charge pump (Figure 2). Although the charge pump is capable of multiplying V_{CC} by up to four times, the output is regulated to V_{CC} + 11V by an internal feedback circuit. The charge pump typically operates at 70kHz, but regulates by pulse-skipping. When V+ exceeds V_{CC} + 11V, the charge pump shuts off. As V+ falls below V_{CC} + 11V, the charge pump turns on.
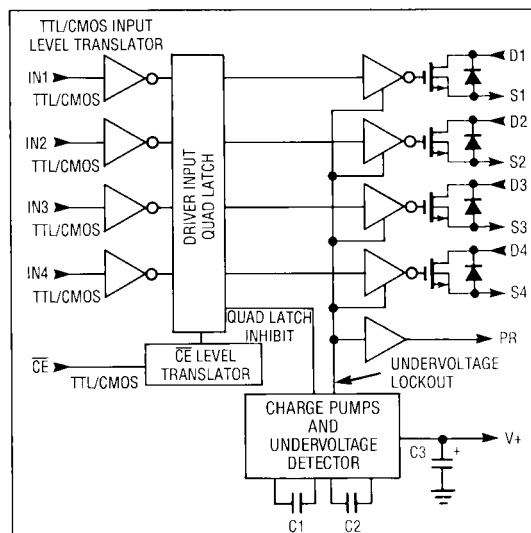

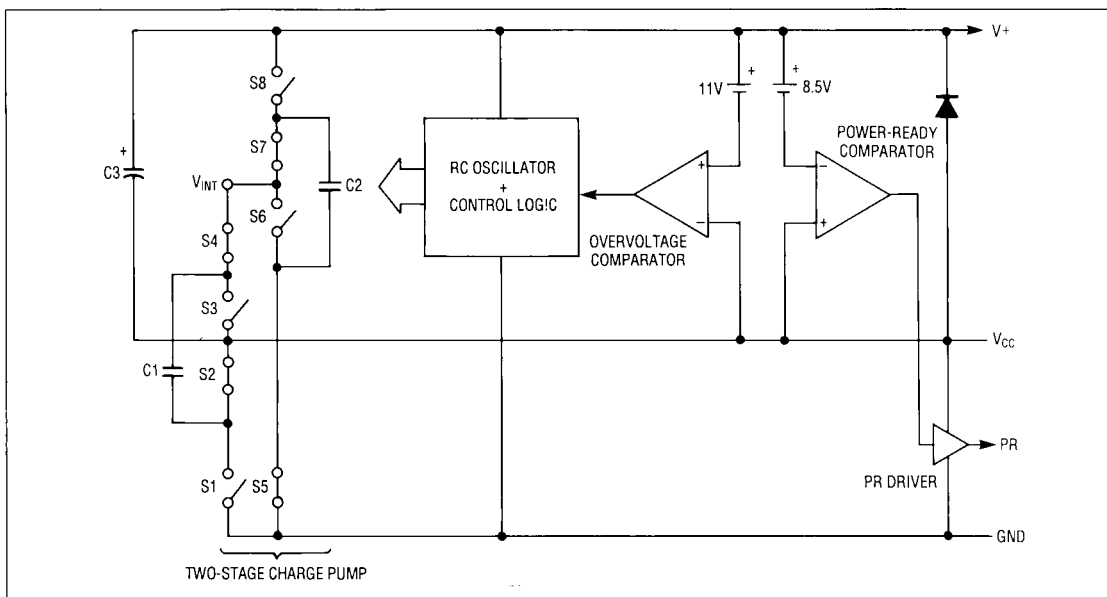Figure 1. MAX625 Functional Diagram

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Figure 2. MAX625 Charge-Pump Diagram

MOSFET Drivers

Four MOSFET drivers level shift TTL/CMOS input signals, without an inversion, to levels that switch between ground and V_{CC} + 11V. These outputs drive the internal N-channel power MOSFETs in either high-side or low-side switching applications (a bridge arrangement would contain two high-side and two low-side N-channel MOSFET switches).

Internal MOSFETs

Each internal MOSFET will handle 4A current peaks. When all four MOSFETs are on, the steady-state $I_{DS(ON)}$ is limited to 1A due to power dissipation limitations.

A body diode connects from source-to-drain on each MOSFET, making them suitable for driving inductive loads. However, the body diode prohibits applications where two different voltages are being switched to the same load. For example, if one MOSFET drain connects to a +12V supply, the other to a +5V supply, and both sources connect to the same load: when the +12V MOSFET turns on, the body diode in the +5V MOSFET forward biases, shorting the two supplies together.

Data Input Latch

Driver outputs are buffered from data inputs by a quad latch. When $\overline{CE}$ is pulled low, the latch is transparent, and data transfers directly to driver outputs. When $\overline{CE}$ goes high, the latch enters hold mode, and new input data is ignored. Input data must be valid 100ns before the rising edge of $\overline{CE}$ and held 10ns (max over temp). The minimum $\overline{CE}$ pulse width is 100ns (Figure 3). If latched operation is not required, connect $\overline{CE}$ to GND.
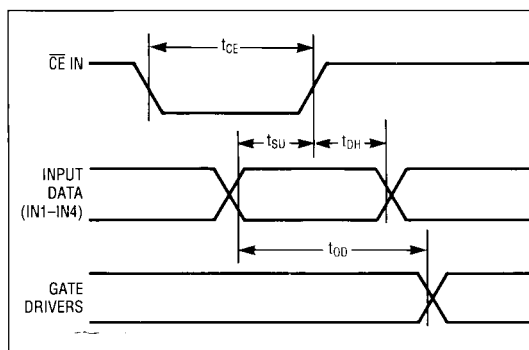

Figure 3. Digital Interface Timing Diagram

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Undervoltage Latch Inhibit

If V_{CC} falls below +3V due to power failure, or while powering down, or V+ falls below V_{CC} + 8.5V, the quad latch immediately resets, forcing the driver outputs low. The quad latch remains reset until V_{CC} rises above +3V and V+ exceeds V_{CC} + 8.5V. This prevents the latch from being corrupted with errorneous data during a momentary power failure.

Undervoltage Detector

The MAX625 contains an undervoltage detector which forces all driver outputs low when the high-side voltage (V+) is less than the Power Ready Threshold (PRT = V_{CC} + 8.5V) or when V_{CC} is less than +3V. This ensures that the internal N-channel MOSFETs have sufficient gate drive to operate without dissipating excess power. On power up, the quad latch remains reset until the charge pump boosts the high-side voltage to the PRT. As soon as V+ reaches the PRT, the undervoltage lockout disables, the quad latch is enabled, and Power Ready (PR) goes high. The undervoltage lockout feature also forces the driver outputs low if V+ is pulled below the PRT, e.g. if the driver output(s) or V+ are overloaded.

Power Ready Output

The MAX625's PR output is a direct extension of the undervoltage lockout feature. When power is applied, PR remains a logic low until V+ reaches the PRT and V_{CC} exceeds +3V. The PR output high level is V_{CC}.

Sourcing Current from V+

A small amount of current may be sourced from V+ (pin 16) to drive other circuitry. The amount of current is a function of V_{CC}, and the driver switching rate. (See "Maximum Switching Rate vs. Additional V+ Load Current", *Typical Operating Characteristics*).

The MAX625 V+ output is not internally short-circuit protected. In applications where V+ is susceptible to short circuit, external output short-circuit protection must be provided. To accomplish this, connect a resistor between V+ and the load to limit the V+ current to less than 25mA. The resistor value is determined by the following formula:

$$R_{CL} \geq \frac{V_{CC}}{25mA}$$

Application Information

Data Input Transition Time

The MAX625 is microprocessor-compatible and easy to interface. However, the driver input voltage must not remain between V_{IL} and V_{IH} for more than 500ns. In clocked databus systems, this is most easily accomplished by setting the data on the driver input lines before clocking $\overline{CE}$ low. However, most CMOS and TTL gates easily meet the 500ns transition speed requirement. Connect unused inputs to ground.

Maximum Driver Switching Rate

The maximum driver switching rate is the rate at which loading causes V+ to fall to the PRT (V_{CC} + 8.5V) and the MOSFETs turn off. It is a function of the maximum charge-pump output current available to the drivers at a given supply voltage. For example, with V_{CC} = +5V and no external load on V+, the maximum switching rate while driving all four inputs is 52kHz. (See "Maximum Switching Rate vs. V_{CC}", *Typical Operating Characteristics*).

Typical Application Circuits

For typical application circuits, see the MAX620/621 datasheet.