

50 μ A, 650 kHz Rail-to-Rail Op Amp

Features

- Gain Bandwidth Product: 650 kHz (typ.)
- Supply Current: $I_Q = 50 \mu\text{A}$ (typ.)
- Supply Voltage: 1.8V to 5.5V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to $+125^\circ\text{C}$
- Available in 5-pin SC-70 and SOT-23 packages

Applications

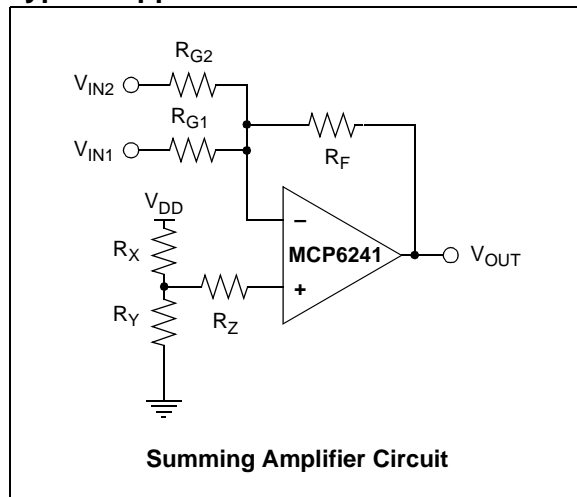
- Automotive
- Portable Equipment
- Photodiode (Transimpedance) Amplifier
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Available Tools

SPICE Macro Models (at www.microchip.com)

FilterLab[®] Software (at www.microchip.com)

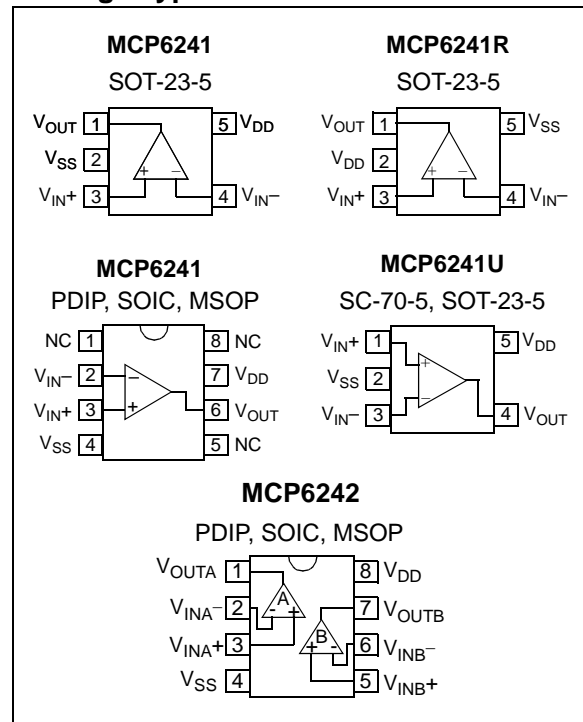
Typical Application



Description

The Microchip Technology Inc. MCP6241/2 operational amplifiers (op amps) provide wide bandwidth for the quiescent current. The MCP6241/2 has a 650 kHz Gain Bandwidth Product (GBWP) and 77° (typ.) phase margin. This family operates from a single supply voltage as low as 1.8V, while drawing 50 μA (typ.) quiescent current. In addition, the MCP6241/2 family supports rail-to-rail input and output swing, with a common mode input voltage range of $V_{DD} + 300 \text{ mV}$ to $V_{SS} - 300 \text{ mV}$. These op amps are designed in one of Microchip's advanced CMOS processes.

Package Types



MCP6241/2

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	7.0V
All Inputs and Outputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage	$ V_{DD} - V_{SS} $
Output Short Circuit Current	continuous
Current at Input Pins	± 2 mA
Current at Output and Supply Pins	± 30 mA
Storage Temperature.....	-65°C to $+150^{\circ}\text{C}$
Maximum Junction Temperature (T_J).....	$+150^{\circ}\text{C}$
ESD Protection On All Pins (HBM;MM)	≥ 4 kV; 200V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{IN+} , V_{INA+} , V_{INB+}	Non-inverting Input
V_{IN-} , V_{INA-} , V_{INB-}	Inverting Input
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
V_{OUT} , V_{OUTA} , V_{OUTB}	Output

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^{\circ}\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $R_L = 100$ k Ω to $V_{DD}/2$ and $V_{OUT} \approx V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-5.0	—	+5.0	mV	$V_{CM} = V_{SS}$
Extended Temperature	V_{OS}	-7.0	—	+7.0	mV	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, (Note)
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	± 3.0	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CM} = V_{SS}$
Power Supply Rejection	PSRR	—	83	—	dB	$V_{CM} = V_{SS}$
Input Bias Current and Impedance						
Input Bias Current:	I_B	—	± 1.0	—	pA	
At Temperature	I_B	—	20	—	pA	$T_A = +85^{\circ}\text{C}$
At Temperature	I_B	—	1100	—	pA	$T_A = +125^{\circ}\text{C}$
Input Offset Current	I_{OS}	—	± 1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13} 6$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 3$	—	ΩpF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	60	75	—	dB	$V_{CM} = -0.3\text{V}$ to 5.3V , $V_{DD} = 5\text{V}$
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	90	110	—	dB	$V_{OUT} = 0.3\text{V}$ to $V_{DD} - 0.3\text{V}$, $V_{CM} = V_{SS}$
Output						
Maximum Output Voltage Swing	V_{OL} , V_{OH}	$V_{SS} + 35$	—	$V_{DD} - 35$	mV	$R_L = 10$ k Ω , 0.5V Output Overdrive
Output Short-Circuit Current	I_{SC}	—	± 6	—	mA	$V_{DD} = 1.8\text{V}$
	I_{SC}	—	± 23	—	mA	$V_{DD} = 5.5\text{V}$
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	30	50	70	μA	$I_O = 0$, $V_{CM} = V_{DD} - 0.5\text{V}$

Note: The SC-70 package is only tested at $+25^{\circ}\text{C}$.

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +1.8$ to 5.5V , $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 10\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	650	—	kHz	
Phase Margin	PM	—	77	—	°	G = +1
Slew Rate	SR	—	0.30	—	V/ μs	
Noise						
Input Noise Voltage	E_{ni}	—	10	—	$\mu\text{Vp-p}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	45	—	nV/ $\sqrt{\text{Hz}}$	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/ $\sqrt{\text{Hz}}$	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$ and $V_{SS} = \text{GND}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	(Note)
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	

Note: The internal Junction Temperature (T_J) must not exceed the Absolute Maximum specification of $+150^\circ\text{C}$.

MCP6241/2

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

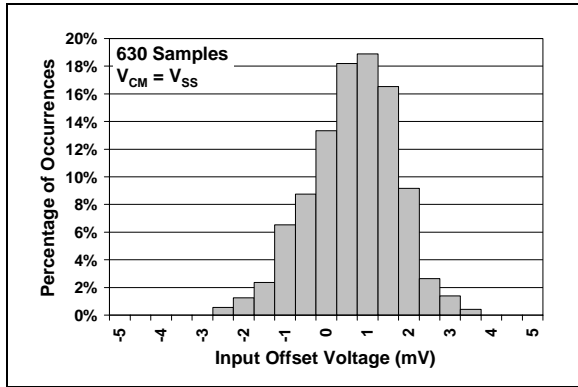


FIGURE 2-1: Input Offset Voltage.

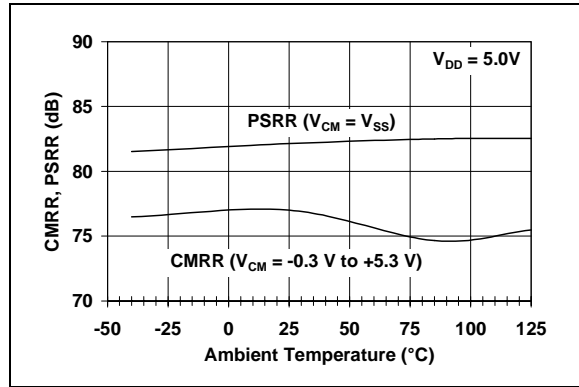


FIGURE 2-4: CMRR, PSRR vs. Ambient Temperature.

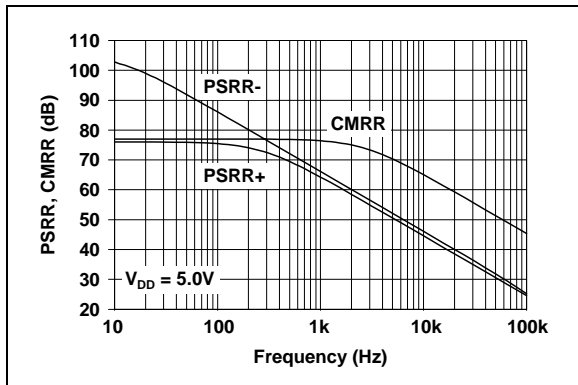


FIGURE 2-2: PSRR, CMRR vs. Frequency.

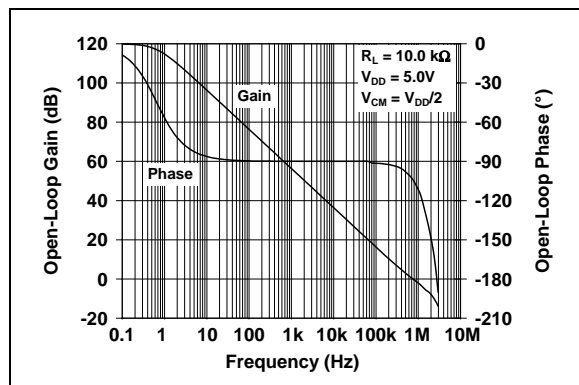


FIGURE 2-5: Open-Loop Gain, Phase vs. Frequency.

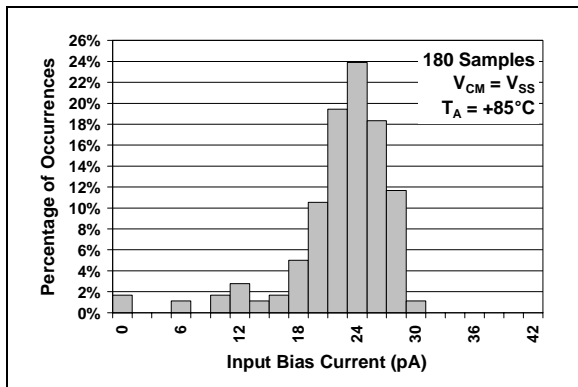


FIGURE 2-3: Input Bias Current at $+85^\circ\text{C}$.

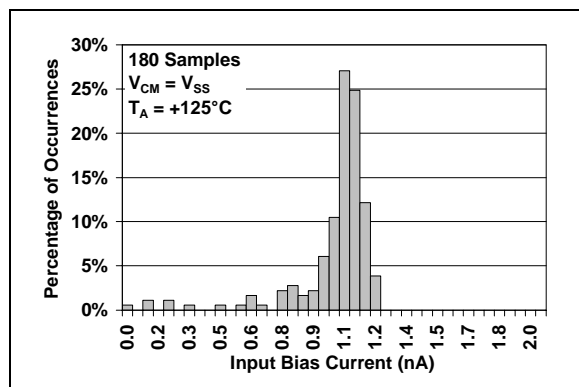


FIGURE 2-6: Input Bias Current at $+125^\circ\text{C}$.

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

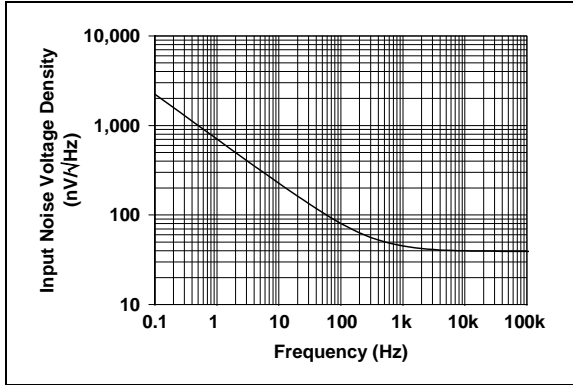


FIGURE 2-7: Input Noise Voltage Density vs. Frequency.

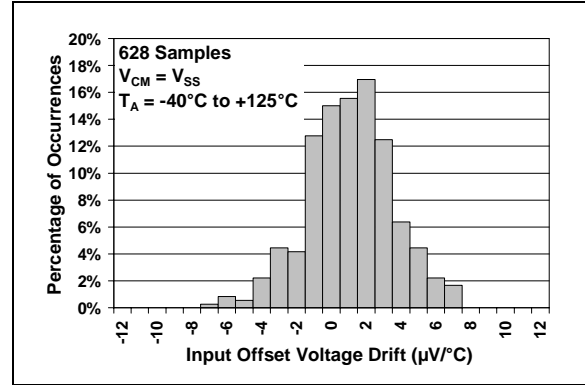


FIGURE 2-10: Input Offset Voltage Drift.

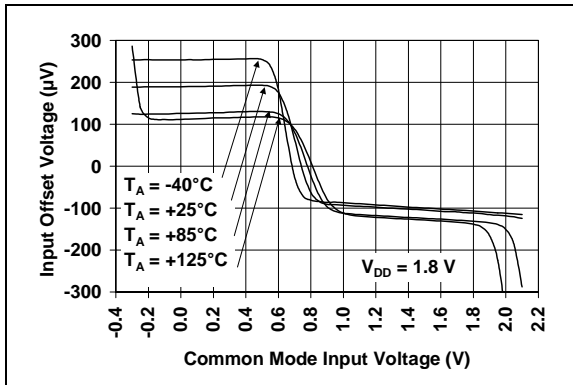


FIGURE 2-8: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 1.8\text{V}$.

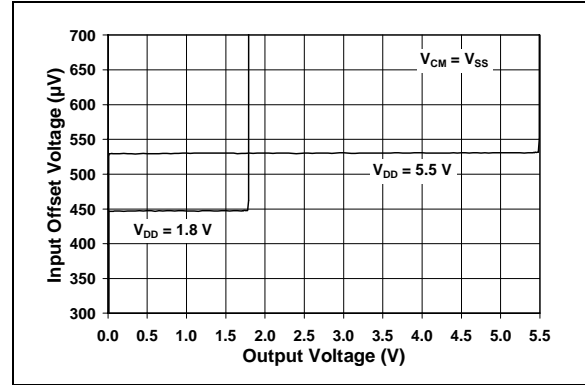


FIGURE 2-11: Input Offset Voltage vs. Output Voltage.

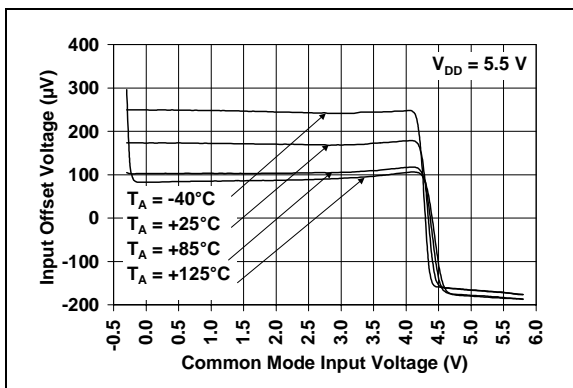


FIGURE 2-9: Input Offset Voltage vs. Common Mode Input Voltage at $V_{DD} = 5.5\text{V}$.

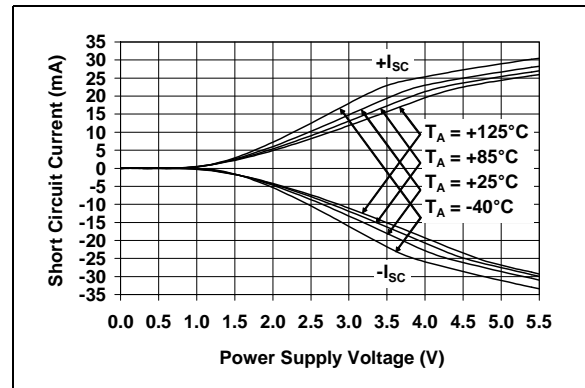


FIGURE 2-12: Output Short-Circuit Current vs. Ambient Temperature.

MCP6241/2

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{DD} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{SS} = \text{GND}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

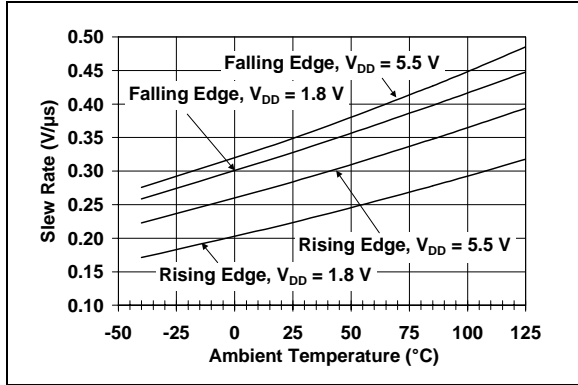


FIGURE 2-13: Slew Rate vs. Ambient Temperature.

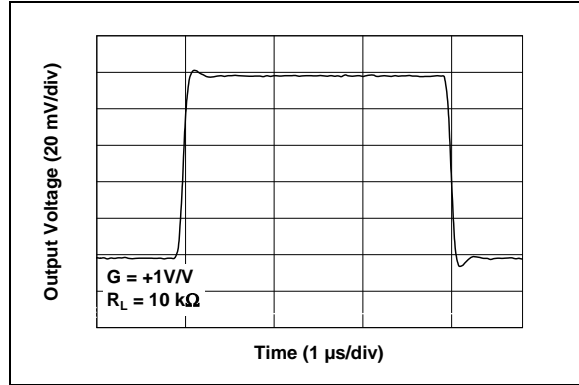


FIGURE 2-16: Small Signal Non-Inverting Pulse Response.

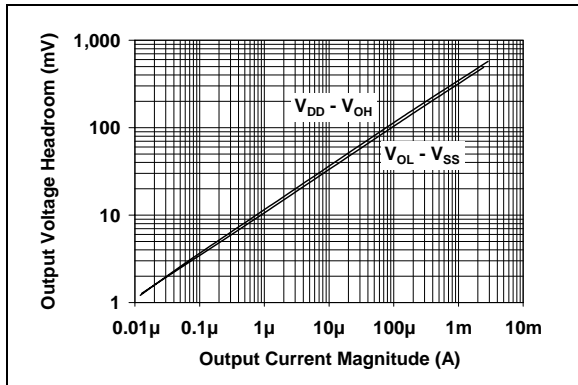


FIGURE 2-14: Output Voltage Headroom vs. Output Current Magnitude.

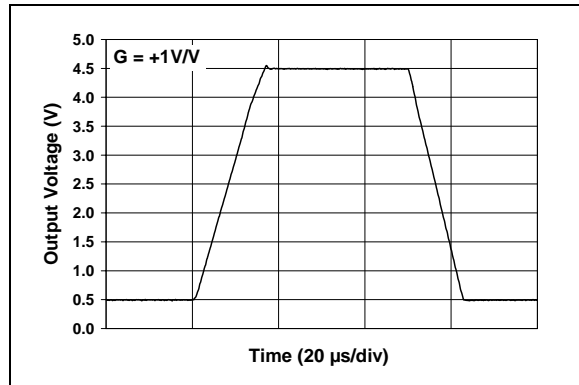


FIGURE 2-17: Large Signal Non-Inverting Pulse Response.

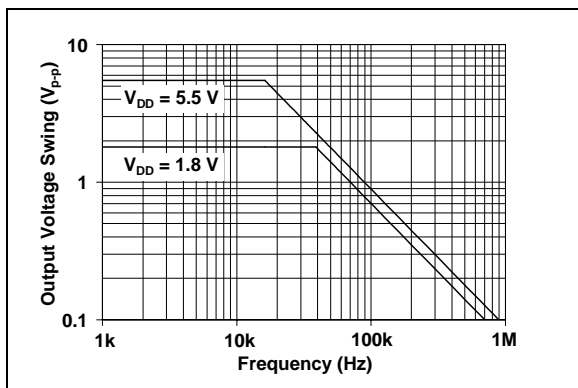


FIGURE 2-15: Output Voltage Swing vs. Frequency.

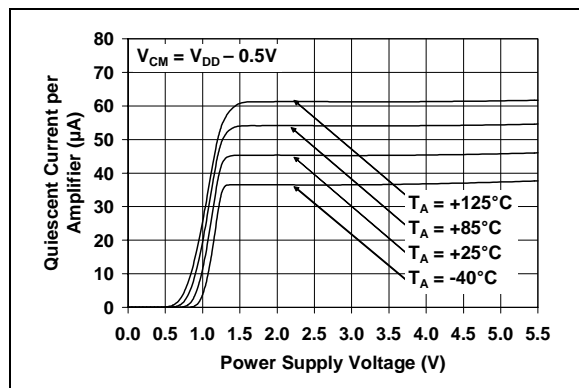


FIGURE 2-18: Quiescent Current vs. Power Supply Voltage.

3.0 APPLICATION INFORMATION

The MCP6241/2 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6241/2 ideal for battery-powered applications.

3.1 Rail-to-Rail Input

The MCP6241/2 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows the input voltage exceeding the supply voltage without any phase reversal.

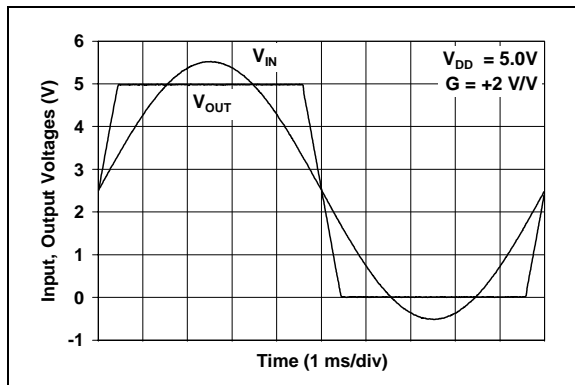


FIGURE 3-1: The MCP6241/2 Show No Phase Reversal.

The input stage of the MCP6241/2 op amps use two differential input stages in parallel. One operates at low common mode input voltage (V_{CM}) and the other at high V_{CM} . With this topology, the device operates with V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS} . The Input Offset Voltage is measured at $V_{CM} = V_{SS} - 300$ mV and $V_{DD} + 300$ mV to ensure proper operation.

Input voltages that exceed the input voltage range ($V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V at 25°C) can cause excessive current to flow into or out of the input pins. Current beyond ± 2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 3-2.

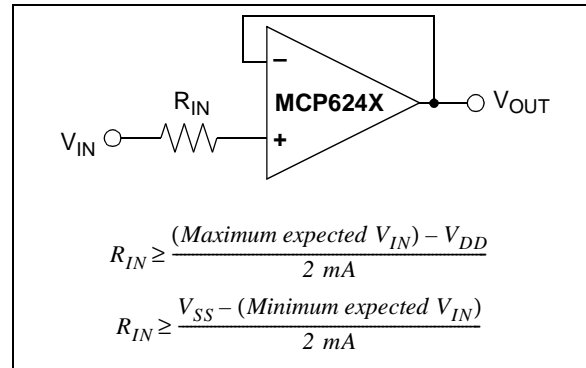


FIGURE 3-2: Input Current-Limiting Resistor (R_{IN}).

3.2 Rail-to-Rail Output

The output voltage range of the MCP6241/2 op amps is $V_{DD} - 35$ mV (min.) and $V_{SS} + 35$ mV (max.) when $R_L = 100$ k Ω is connected to $V_{DD}/2$ and $V_{DD} = 5.5$ V. Refer to Figure 2-14 for more information.

3.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer ($G = +1$) is the most sensitive to capacitive loads, but all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when $G = +1$), a small series resistor at the output (R_{ISO} in Figure 3-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. It does not, however, improve the bandwidth.

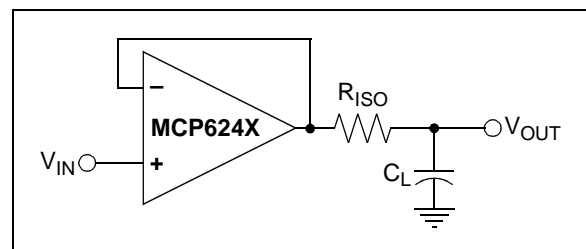


FIGURE 3-3: Output resistor, R_{ISO} stabilizes large capacitive loads.

Figure 3-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the gain are equal. For inverting gains, G_N is $1 + |\text{Gain}|$ (e.g., -1 V/V gives $G_N = +2$ V/V).

MCP6241/2

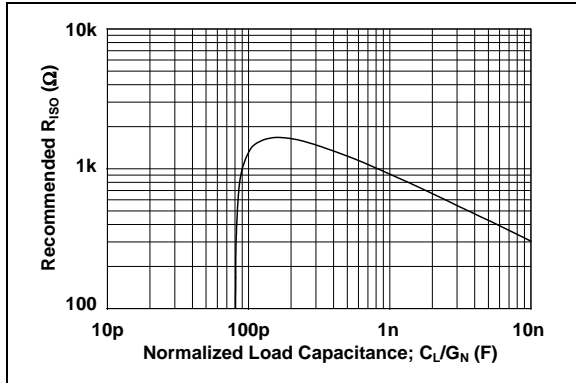


FIGURE 3-4: Recommended R_{ISO} Values for Capacitive Loads.

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Evaluation on the bench and simulations with the MCP6241/2 SPICE macro model are very helpful. Modify R_{ISO} 's value until the response is reasonable.

3.4 Supply Bypass

With this op amp, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μF to 0.1 μF) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 μF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other parts.

3.5 PCB Surface Leakage

In applications where low input bias current is critical, PCB (printed circuit board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA, if current-to-flow. This is greater than the MCP6241/2 family's bias current at 25°C (1 pA, typ).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-5.

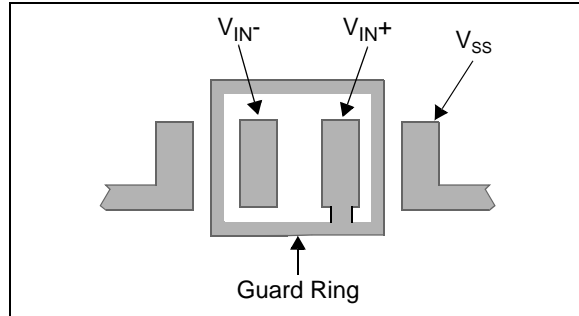


FIGURE 3-5: Example Guard Ring Layout for Inverting Gain.

1. Non-inverting Gain and Unity-Gain Buffer:
 - a. Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
 - b. Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the common mode input voltage.
2. Inverting and transimpedance gain amplifiers (convert current to voltage, such as photo detectors):
 - a. Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
 - b. Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

4.0 APPLICATION CIRCUITS

4.1 Matching the Impedance at the Inputs

To minimize the effect of offset voltage in an amplifier circuit, the impedance at both inverting and non-inverting inputs needs to be matched. This is done by choosing the circuit resistor values so that the total resistance at each input is the same. Figure 4-1 shows a summing amplifier circuit.

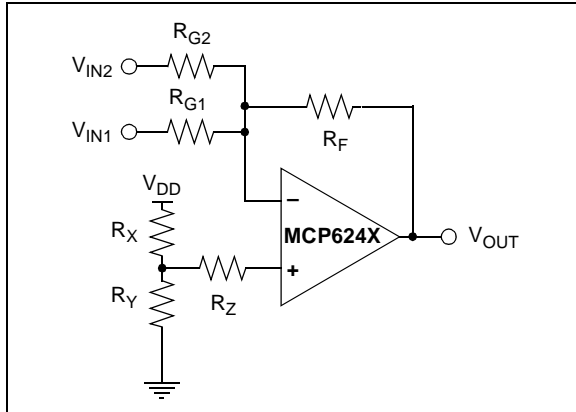


FIGURE 4-1: Summing Amplifier Circuit.

To match the inputs, set all voltage sources to ground and calculate the total resistance at the input nodes. In this summing amplifier circuit, the resistance at the inverting input is calculated by setting V_{IN1} , V_{IN2} and V_{OUT} to ground. In this case, R_{G1} , R_{G2} and R_F are in parallel. The total resistance at the inverting input is:

$$R_{VIN^-} = \frac{I}{\left(\frac{I}{R_{G1}} + \frac{I}{R_{G2}} + \frac{I}{R_F}\right)}$$

Where:

R_{VIN^-} = total resistance at the inverting input

At the non-inverting input, V_{DD} is the only voltage source. When V_{DD} is set to ground, both R_X and R_Y are in parallel. The total resistance at the non-inverting input is:

$$R_{VIN^+} = \frac{I}{\left(\frac{I}{R_X} + \frac{I}{R_Y}\right)} + R_Z$$

Where:

R_{VIN^+} = total resistance at the inverting input

To minimize offset voltage and increase circuit accuracy, the resistor values need to meet the condition:

$$R_{VIN^+} = R_{VIN^-}$$

4.2 Compensating for the Parasitic Capacitance

In analog circuit design, the PCB parasitic capacitance can compromise the circuit behavior; Figure 4-2 shows a typical scenario. If the input of an amplifier sees parasitic capacitance of several picofarad (C_{PARA} , which includes the common mode capacitance of 6 pF, typical) and large R_F and R_G , the frequency response of the circuit will include a zero. This parasitic zero introduces gain peaking and can cause circuit instability.

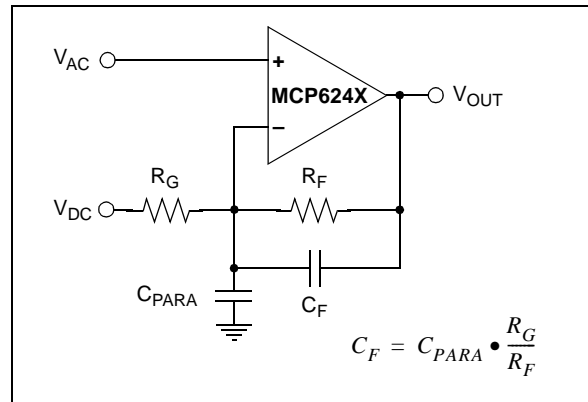


FIGURE 4-2: Effect of Parasitic Capacitance at the Input.

One solution is to use smaller resistor values to push the zero to a higher frequency. Another solution is to compensate by introducing a pole at the point at which the zero occurs. This can be done by adding C_F in parallel with the feedback resistor (R_F). C_F needs to be selected so that the ratio $C_{PARA}:C_F$ is equal to the ratio of $R_F:R_G$.

MCP6241/2

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6241/2 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6241/2 op amps is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

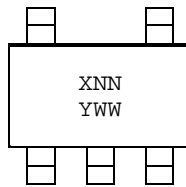
5.2 FilterLab[®] Software

The FilterLab software is an innovative tool that simplifies analog active-filter (using op amps) design. Available free of charge from our web site at www.microchip.com, the FilterLab software active-filter design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

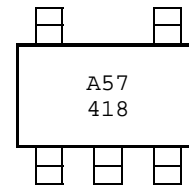
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

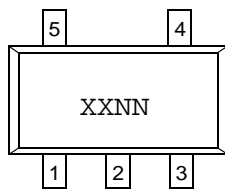
5-Lead SC-70



Example:



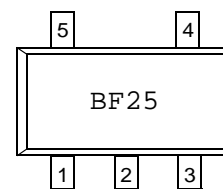
5-Lead SOT-23



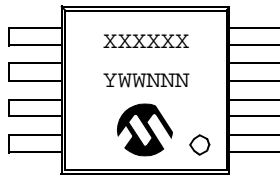
Device	Code
MCP6241	BFNN
MCP6241R	BGNN
MCP6241U	BHNN

Note: Applies to 5-Lead SOT-23.

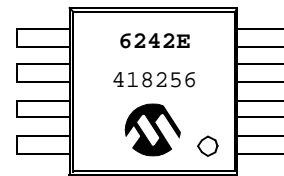
Example:



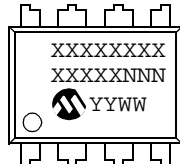
8-Lead MSOP



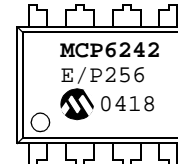
Example:



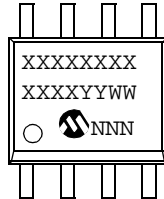
8-Lead PDIP (300 mil)



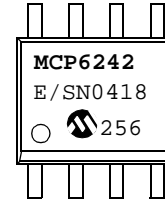
Example:



8-Lead SOIC (150 mil)



Example:



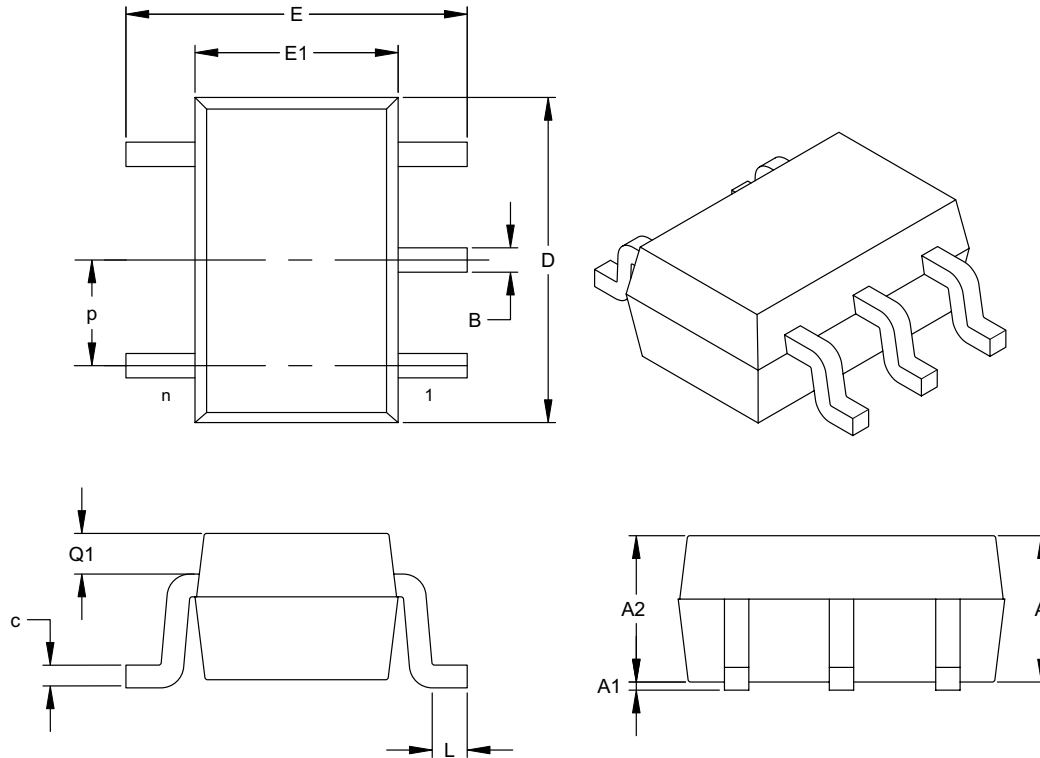
Legend: XX...X Customer specific information*
 YY Year code (last 2 digits of calendar year)
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

MCP6241/2

5-Lead Plastic Small Outline Transistor Package (LT) (SC-70)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p	.026 (BSC)			0.65 (BSC)		
Overall Height	A	.031		.043	0.80		1.10
Molded Package Thickness	A2	.031		.039	0.80		1.00
Standoff	A1	.000		.004	0.00		0.10
Overall Width	E	.071		.094	1.80		2.40
Molded Package Width	E1	.045		.053	1.15		1.35
Overall Length	D	.071		.087	1.80		2.20
Foot Length	L	.004		.012	0.10		0.30
Top of Molded Pkg to Lead Shoulder	Q1	.004		.016	0.10		0.40
Lead Thickness	c	.004		.007	0.10		0.18
Lead Width	B	.006		.012	0.15		0.30

*Controlling Parameter

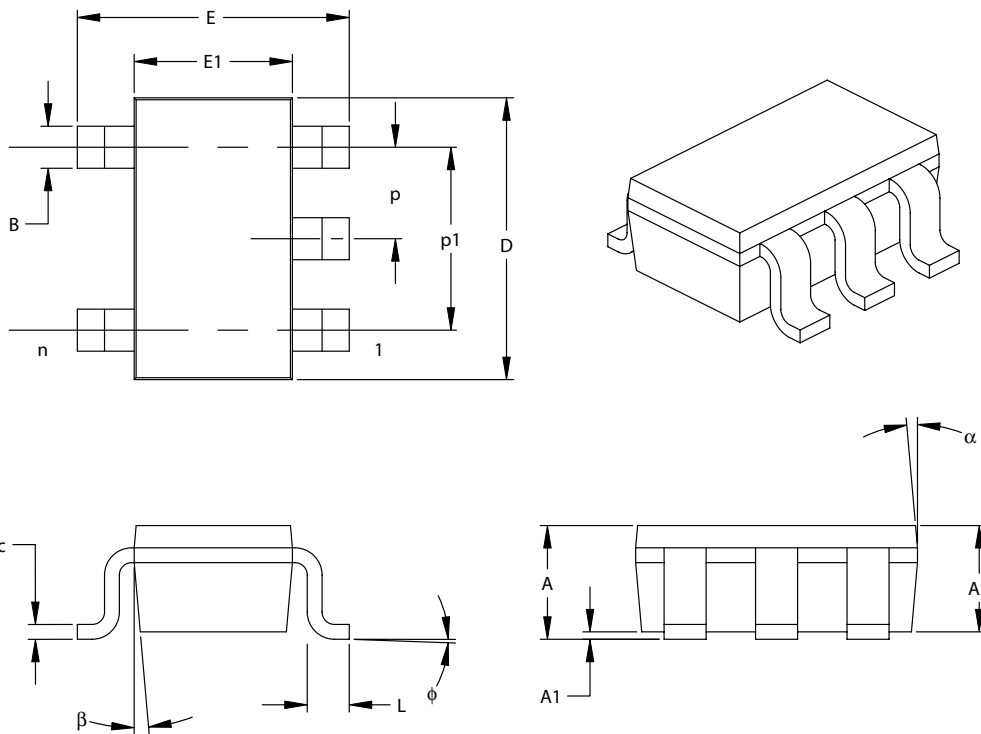
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (EIAJ) Standard: SC-70

Drawing No. C04-061

5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	5			5		
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

Notes:

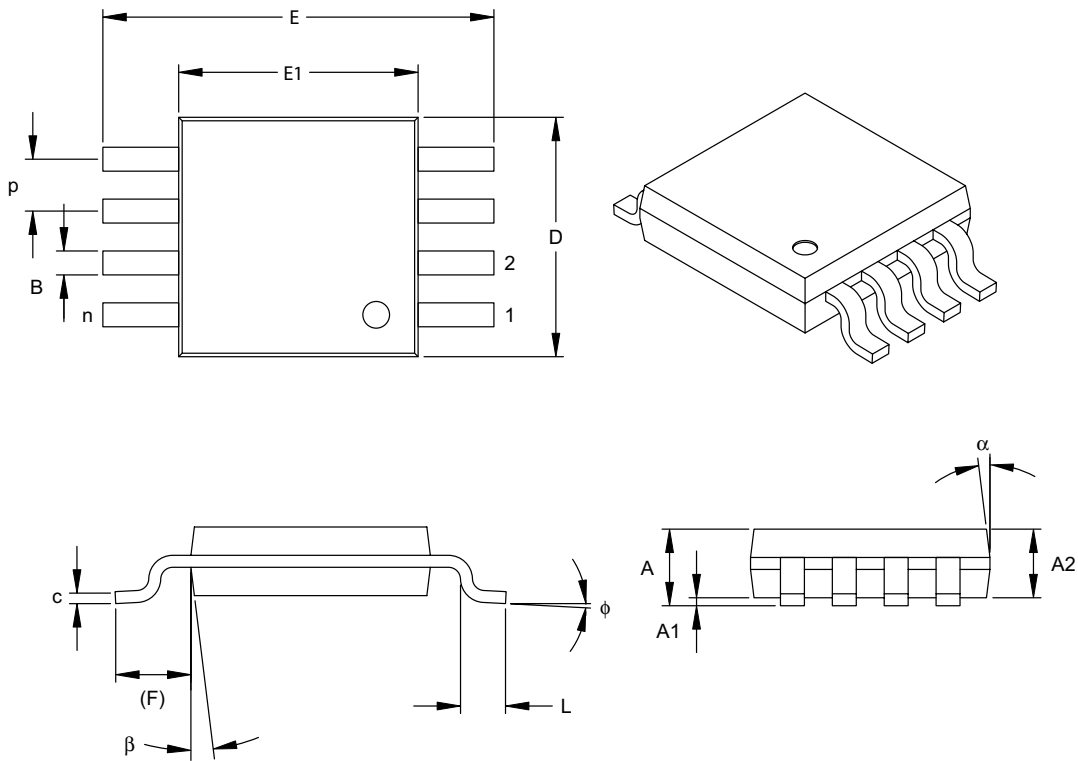
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

EIAJ Equivalent: SC-74A

Drawing No. C04-091

MCP6241/2

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
	n	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n	8			8		
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

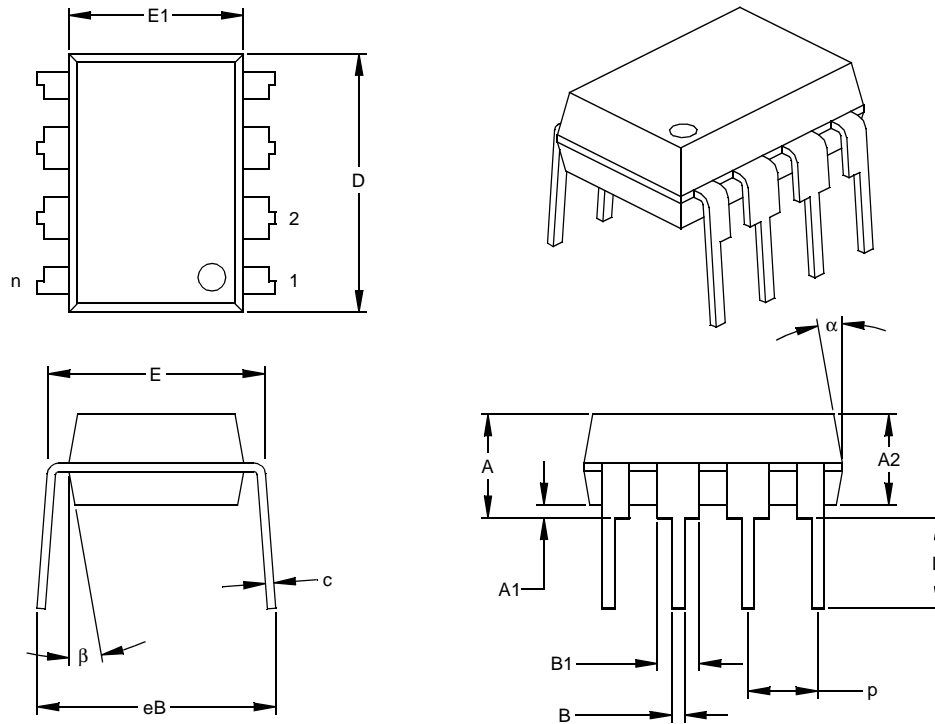
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

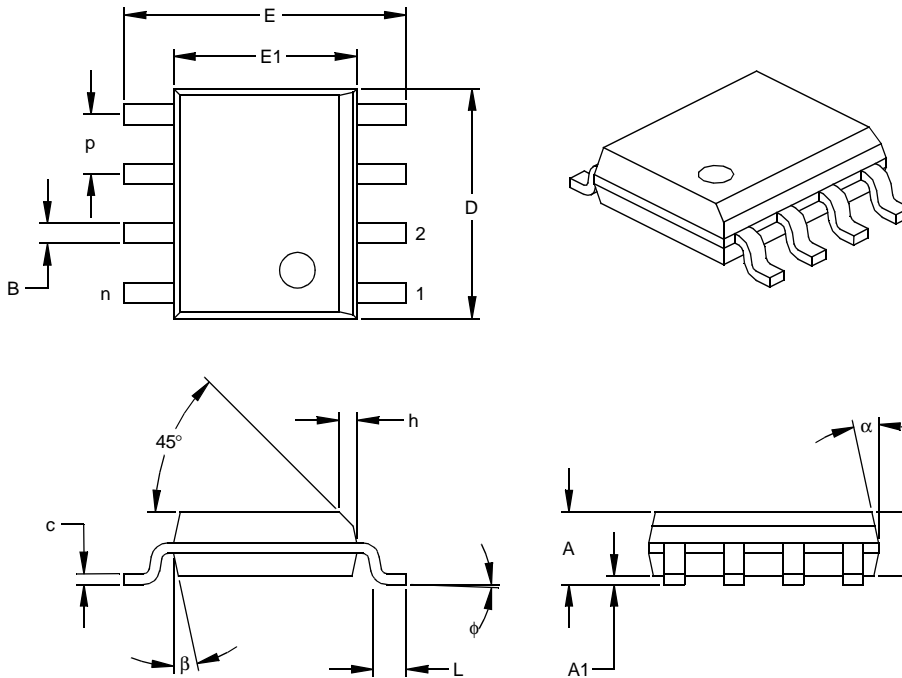
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

MCP6241/2

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-012
 Drawing No. C04-057

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>-X</u>	<u>/XX</u>	Examples:
Device	Tape and Reel and/or Alternate Pinout	Temperature Range	Package	
Device:	MCP6241: Single Op Amp (MSOP, PDIP, SOIC) MCP6241T: Single Op Amp (Tape and Reel) (SOT-23) MCP6241RT: Single Op Amp (Tape and Reel) (SOT-23) MCP6241UT: Single Op Amp (Tape and Reel) (SC-70, SOT-23)	MCP6242: Dual Op Amp (MSOP, PDIP, SOIC) MCP6242T: Dual Op Amp (Tape and Reel)		a) MCP6241-E/SN: Extended Temp., 8LD SOIC pkg. b) MCP6241-E/MS: Extended Temp., 8LD MSOP pkg. c) MCP6241-E/P: Extended Temp., 8LD PDIP pkg. d) MCP6241RT-E/OT: Tape and Reel, Extended Temp., 5LD SOT-23 pkg e) MCP6241UT-E/OT: Tape and Reel, Extended Temp., 5LD SOT-23 pkg. f) MCP6241UT-E/LT: Tape and Reel, Extended Temp., 5LD SC-70 pkg. g) MCP6241T-E/OT: Tape and Reel, Extended Temp., 5LD SOT-23 pkg.
Temperature Range:	E = -40°C to +125°C			a) MCP6242-E/SN: Extended Temp., 8LD SOIC pkg. b) MCP6242-E/MS: Extended Temp., 8LD MSOP pkg. c) MCP6242-E/P: Extended Temp., 8LD PDIP pkg. d) MCP6242T-E/SN: Tape and Reel, Extended Temp., 8LD SOIC pkg.
Package:	LT = Plastic Package (SC-70), 5-lead (MCP6241U only) MS = Plastic Micro Small Outline (MSOP), 8-lead P = Plastic DIP (300 mil Body), 8-lead OT = Plastic Small Outline Transistor (SOT-23), 5-lead (MCP6241, MCP6241R, MCP6241U) SN = Plastic SOIC, (150 mil Body), 8-lead			

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

MCP6241/2

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, microID, MPLAB, PIC, PICmicro, PICSTART, PRO MATE, PowerSmart, rfPIC, and SmartShunt are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.


AmpLab, FilterLab, MXDEV, MXLAB, PICMASTER, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, dsPICDEM, dsPICDEM.net, dsPICworks, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICkit, PICDEM, PICDEM.net, PICLAB, PICtail, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rfPICDEM, Select Mode, Smart Serial, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2004, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona and Mountain View, California in October 2003. The Company's quality system processes and procedures are for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: www.microchip.com

Atlanta

Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

Addison Plaza
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

Mission Viejo, CA 92691
Tel: 949-462-9523
Fax: 949-462-9608

San Jose

Mountain View, CA 94043
Tel: 650-215-1444
Fax: 650-961-0286

Toronto

Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Sydney, Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Wan Tai Bei Hai Bldg.
Beijing, 100027, China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Ming Xing Financial Tower
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

World Trade Plaza
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Metroplaza
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Far East International Plaza
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

United Plaza
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Foshan City, Guangdong 528303, China
Tel: 86-757-28395507
Fax: 86-757-28395571

China - Qingdao

Fullhope Plaza,
Qingdao 266071, China
Tel: 86-532-5027355
Fax: 86-532-5027205

India

Divyasree Chambers
Bangalore, 560 025, India
Tel: 91-80-22290061 Fax: 91-80-22290062

India

International Trade Tower
New Delhi, 110019, India
Tel: +91-11-5160-8632
Fax: +91-11-5160-8632

Japan

Yokohama, Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166
Fax: 81-45-471-6122

Korea

Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or 82-2-558-5934

Singapore

Singapore, 188980
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
Kaohsiung 806, Taiwan
Tel: 886-7-536-4816
Fax: 886-7-536-4817

Taiwan

Taiwan Branch
Taipei City, 104, Taiwan
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Taiwan

Taiwan Branch
Hsinchu City 300, Taiwan
Tel: 886-3-572-9526
Fax: 886-3-572-6459

EUROPE

Austria

Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Ballerup DK-2750 Denmark
Tel: 45-4420-9895
Fax: 45-4420-9910

France

91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

NL-5152 JR, Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820