FAIRCHILD SEMICONDUCTOR®

March 2007

FAN5182 — Adjustable Output, 1-, 2-, or 3-Phase Synchronous Buck Controller

Features

- Selectable 1-, 2-, or 3-Phase Operation at up to 1MHz per Phase
- Accuracy:
  - FAN5182 2%
  - FAN5182_NA3E229 1%
  - FAN5182_NA3E231 3%
- Externally Adjustable 0.8V to 5V Output from a 12V Supply
- Logic-Level PWM Outputs for Interface to External High-Power Drivers
- Active Current Balancing Between all Phases
- Built-in Power-Good / Crowbar Functions
- Programmable Over-Current Protection with Adjustable Latch-Off Delay

Applications

- Auxiliary Supplies
- DDR Memory Supplies
- Point-of-Load Supplies

Description

The FAN5182 is a highly efficient, multiphase, synchronous buck switching regulator controller optimized for converting a 12V main supply into a high-current, low-voltage supply for use in point-of-load (POL) applications. It uses a multi-loop PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for regulator size and efficiency. The phase relationship of the output signals can be programmed to provide 1-, 2-, or 3-phase operation, allowing for construction of up to three complementary, interleaved buck switching stages.

The FAN5182 provides accurate and reliable over-current protection and adjustable current limiting.

The FAN5182 is specified over the commercial temperature range of 0°C to +85°C and is available in a 20-lead Quarter-Size Outline Package (QSOP).

Ordering Information

Part Number	Temperature Range	Pb-Free	Package	Packing Method	Quantity per Reel
FAN5182QSCX_NL	0°C to 85°C	Yes	QSOP-20L	Tape and Reel	2500
FAN5182QSCX_NA3E229_NL	0°C to 85°C	Yes	QSOP-20L	Tape and Reel	2500
FAN5182QSCX_NA3E231_NL	0°C to 85°C	Yes	QSOP-20L	Tape and Reel	2500

Block Diagram

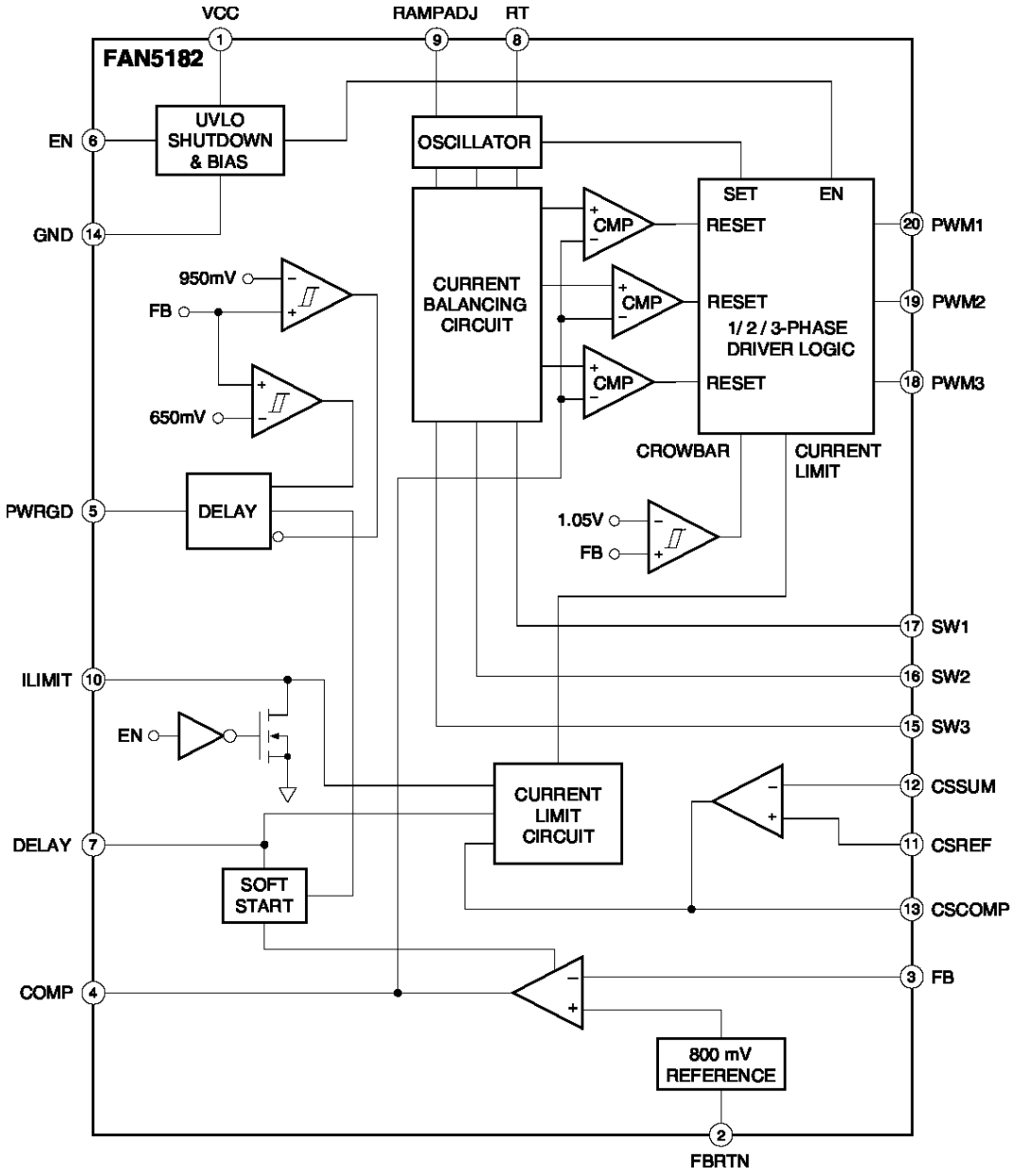

Figure 1. Block Diagram

Pin Assignments

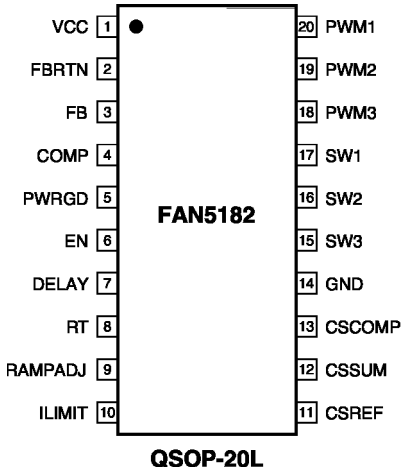

Figure 2. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	VCC	Supply Voltage for the Device.
2	FBRTN	Feedback Return. Voltage error amplifier reference for remote sensing of the output voltage.
3	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor divider between the output and FBRTN connected to this pin sets the output voltage. This pin is also the reference point for the power-good and crowbar comparators.
4	COMP	Error Amplifier Output and Compensation Pin.
5	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside the proper operating range.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	DELAY	Soft-Start Delay and Current Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft-start ramp-up time and the over-current latch-off delay time.
8	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
9	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
10	ILIMIT	Current-Limit Set point / Enable Output. An external resistor connected from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the EN input is low, or when V_{CC} is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low.
11	CSREF	Current-Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current-sense amplifier. Connect this pin to the common point of the output inductors.
12	CSSUM	Current-Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents to measure the total output current.
13	CSCOMP	Current-Sense Compensation Point. A resistor and a capacitor from this pin to CSSUM determine the gain of the current sense amplifier.
14	GND	Ground. All internal biasing and logic output signals are referenced to this ground.
15–17	SW3 - SW1	Current Balance Inputs. These are inputs for measuring the current level in each phase. The SW pins of unused phases should be connected to ground.
18–20	PWM3 - PWM1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver, such as the FAN5109. Connecting the PWM3 output to GND causes that phase to turn off, allowing the FAN5182 to operate as a 1- or 2-phase controller. Do not connect PWM2 to ground for 1-phase operation.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Unless otherwise noted, all voltages are referenced to GND.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	VCC	-0.3	+15	V
	FBRTN	-0.3	+0.3	V
	EN, DELAY, ILIMIT, RT, PWM1-PWM3, COMP	-0.3	5.5	V
	SW1-SW3	-5	+25	V
	All Other Inputs and Outputs	-0.3	V_{CC} + 0.3	V
T_J	Operating Junction Temperature	0	+125	°C
T_{STG}	Storage Temperature	-65	+150	°C
T_L	Lead Soldering Temperature (10 seconds)		300	°C
T_{LI}	Lead Infrared Temperature (15 seconds)		260	°C
Θ_{JC}	Thermal Resistance Junction-to-Case		38	°C/W
Θ_{JA}	Thermal Resistance Junction-to-Ambient[1]		90	°C/W

Note:

1. Junction-to-ambient thermal resistance, Θ_{JA}, is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics. It is measured with the device mounted on a board of FR-4 material, 0.063inch thickness, no copper plane, and zero air flow.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	10.8	12.0	13.2	V
T_A	Operating Ambient Temperature	0		+85	°C

Electrical Characteristics

V_{CC} = 12V, FBRTN = GND, • indicates specifications over operating ambient temperature range.[2]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Oscillator							
f_{OSC}	Frequency Range		•	0.25		3.00	MHz
T_{PHASE}	Frequency Variation	R_T = 332kΩ, 3-phase	•	155	200	245	kHz
		T_A = 25°C, R_T = 154kΩ, 3-phase	•	155	400	245	
		T_A = 25°C, R_T = 100kΩ, 3-phase	•	155	600	245	
V_{RT}	Output Voltage	R_T = 100kΩ to GND	•		2.0		V
$V_{RAMPADJ}$	RAMPADJ Output Voltage	RAMPADJ - FB - 2KΩ x $I_{RAMPADJ}$ (with $I_{RAMPADJ}$ set to 20µA)	•	-50		+50	mV
$I_{RAMPADJ}$	RAMPADJ Input Current Range[3]			0		100	µA
Voltage Error Amplifier							
V_{OL}	Output Voltage Low					0.3	V
V_{OH}	Output Voltage High			3.1			V
V_{FB}	Accuracy (Referenced to FBRTN)	FAN5182 2%	•	784	800	816	mV
		FAN5182_NA3E229 1%	•	792	800	808	mV
		FAN5182_NA3E231 3%	•	786	800	824	mV
I_{FB}	Input Bias Current	FB = 800mV	•	-4	±1	+4	µA
ΔV_{FB}	Line Regulation	V_{CC} = 10V to 14V			0.05		%
I_{FBRTN}	FBRTN Current		•		100	140	µA
$I_{O(ERR)}$	Output Current	FB forced to V_{OUT} - 3%			500		µA
	DC Gain[3]				87		dB
$G_{BW(ERR)}$	Gain Bandwidth Product[3]	COMP = FB			20		MHz
	Slew Rate[3]	C_{COMP} = 10pF			10		V/µs
Current-Sense Amplifier							
$V_{OS(CSA)}$	Offset Voltage	CSSUM-CSREF (See Figure 3)	•	-5.5		+5.5	mV
$I_{BIAS(CSSUM)}$	Input Bias Current		•	-50		+50	nA
	DC Gain[3]				70		dB
$G_{BW(CSA)}$	Gain Bandwidth Product[3]				10		MHz
	Slew Rate[3]	C_{CSCOMP} = 10pF			10		V/µs
	Input Common-Mode Range	C_{SSUM} & C_{SREF}		0		V_{CC}-2.5	V
V_{OL}	Output Voltage Low					0.1	V
V_{OH}	Output Voltage High			V_{CC}-2.5			V
I_{CSCOMP}	Output Current				500		µA
Current-Balance Circuit							
$V_{SW(X)CM}$	Common-Mode Range[3]			-600		+200	mV
$R_{sw(X)}$	Input Resistance	SW(X) = 0V	•	20	30	40	kΩ
$I_{SW(X)}$	Input Current	SW(X) = 0V	•	4	7	10	µA
$\Delta I_{SW(X)}$	Input Current Matching	SW(X) = 0V	•	-7		+7	%
$\Delta V_{OS\ Match}$	Offset Voltage Matching (Difference between phases)	FAN5182				11	mV
		FAN5182_NA3E229				8	mV
		FAN5182_NA3E231				8	mV

Electrical Characteristics (Continued)

V_{CC} = 12V, FBRTN = GND, • indicates specifications over operating ambient temperature range.[2]

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Current-Limit Comparator							
$V_{ILIMIT(NM)}$	Output Voltage: Normal Mode	EN > 2.0V, R_{ILIMIT} = 250kΩ	•	2.9	3.0	3.1	V
$V_{ILIMIT(SD)}$	Output Voltage: In Shutdown	EN < 0.8V, I_{ILIMIT} = -100µA	•			400	mV
$I_{ILIMIT(NM)}$	Output Current: Normal Mode	EN > 2.0V, R_{ILIMIT} = 250kΩ			12		µA
	Maximum Output Current		•	60			µA
V_{CL}	Current Limit Threshold	V_{CSREF} - V_{CSCOMP} , R_{ILIMIT} = 250kΩ		105	125	145	mV
	Current Limit Setting Ratio	V_{CL}/I_{ILIMIT}			10.4		mV/µA
$V_{DELAY(NM)}$	Delay Normal Mode Voltage	R_{DELAY} = 250kΩ		2.9	3.0	3.1	V
$V_{DELAY(OC)}$	Delay Over-Current Threshold	R_{DELAY} = 250kΩ		1.7	1.8	1.9	V
t_{DELAY}	Latch-Off Delay Time[3]	R_{DELAY} = 250kΩ, C_{DELAY} = 12nF			1.5		ms
Soft-Start							
$I_{DELAY(SS)}$	Output Current, Soft-Start Mode	During start-up, Delay < 2.4V	•	15	20	25	µA
$t_{DELAY(SS)}$	Soft-Start Delay Time[3]	R_{DELAY} = 250kΩ, C_{DELAY} = 12nF			500		µs
Enable Input							
$V_{IL(EN)}$	Input Low Voltage		•			0.8	V
$V_{IH(EN)}$	Input High Voltage		•	2.0			V
	Input Hysteresis Voltage				100		mV
$I_{IN(EN)}$	Input Current		•	-1		+1	µA
Power-Good Comparator							
$V_{PWRGD(UV)}$	Under-Voltage Threshold	Relative to FBRTN	•	600	660	720	mV
$V_{PWRGD(OV)}$	Over-Voltage Threshold	Relative to FBRTN	•	880	940	1000	mV
$V_{OL(PWRGD)}$	Output Low Voltage	$I_{PWRGD(SINK)}$ = 4mA	•		225	400	mV
	Power-Good Delay Time				200		ns
$V_{CROWBAR}$	Crowbar Trip Point	Relative to FBRTN	•	0.970	1.050	1.105	V
	Crowbar Reset Point	Relative to FBRTN	•	550	650	750	mV
$t_{CROWBAR}$	Crowbar Delay Point[3]	Over-voltage to PWM going low			400		ns
PWM Outputs							
$V_{OL(PWM)}$	Output Low Voltage	$I_{PWM(SINK)}$ = 400µA	•		160	500	mV
$V_{OH(PWM)}$	Output High Voltage	$I_{PWM(SOURCE)}$ = -400µA	•	4.0	5		V
Supply							
	DC Supply Current		•		5	10	mA
V_{UVLO}	UVLO Threshold Voltage	V_{CC} rising	•	6.5	6.9	7.3	V
	UVLO Hysteresis		•	0.7	0.9	1.1	V

Notes:

2. Limits at operating temperature extremes are guaranteed by design, characterization, and statistical quality control.
3. Guaranteed by design, not tested in production.

Test Circuit

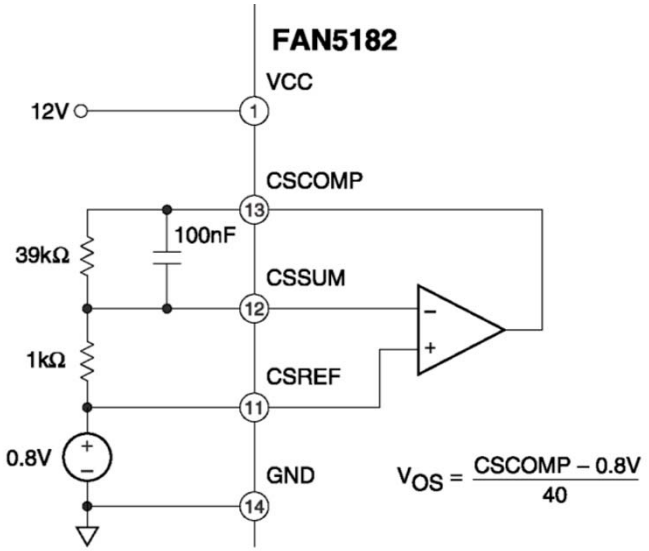

Figure 3. Current-Sense Amplifier

Typical Performance Characteristics

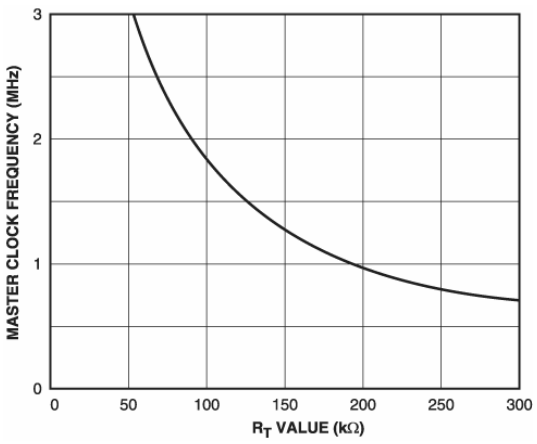

Figure 4. Master Clock Frequency vs. R_T

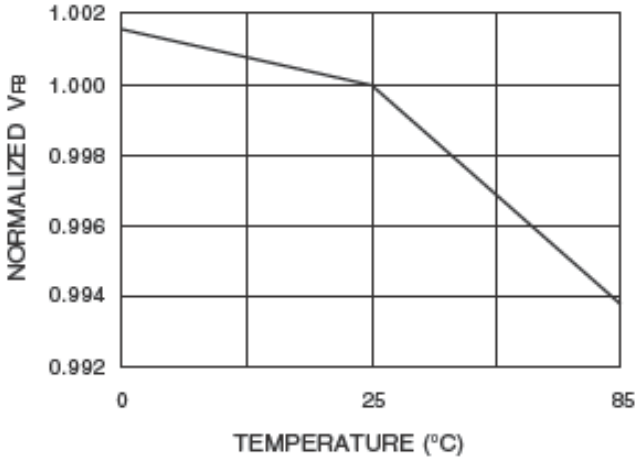

Figure 5. Normalized V_{FB} vs. Temperature

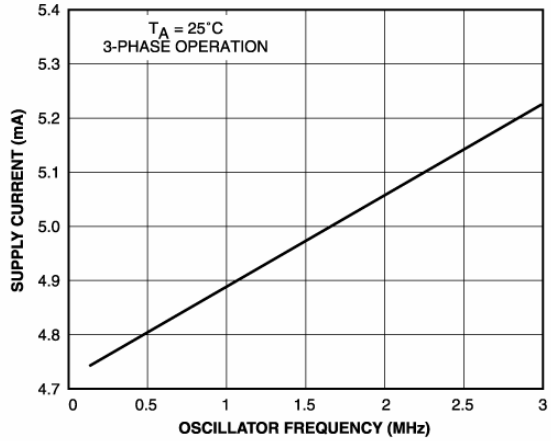

Figure 6. Supply Current vs. Oscillator Frequency

Typical Application Circuit

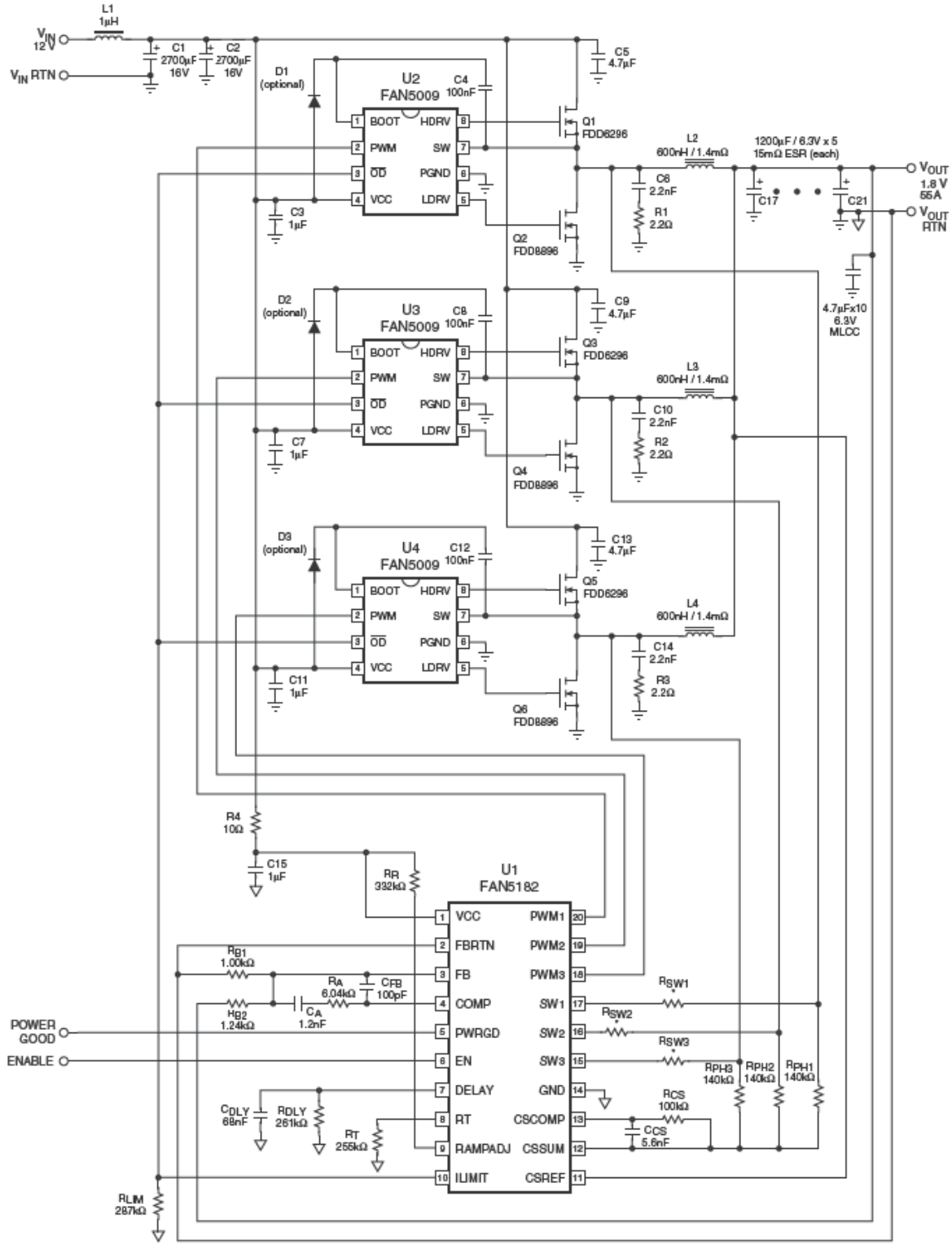

Figure 7. 1.8V, 55A Application Circuit

Theory of Operation

The FAN5182 combines a multi-loop, fixed-frequency PWM control with multi-phase logic outputs for use in 1-, 2-, and 3-phase synchronous buck point-of-load power supplies. Multi-phase operation is important for producing the high current and low voltage demanded by auxiliary supplies in desktop computers, workstations, and servers. Handling high current in a single-phase converter places high thermal stress on components, such as inductors and MOSFETs, and is not preferred.

The multi-loop control of the FAN5182 ensures a stable, high performance topology for:

- Balancing current and thermal between/among phases
- Fast response at the lowest possible switching frequency and output decoupling
- Reducing switching losses due to low-frequency operation
- Tight line and load regulation
- Reducing output ripple due to multiphase cancellation
- Better noise immunity to facilitate PCB layout

Start-up Sequence

During start-up, the number of operational phases and their phase relationship are determined by the internal circuitry that monitors the PWM outputs. Normally, the FAN5182 operates as a 3-phase PWM controller. Grounding the PWM3 pin programs the FAN5182 for 1- or 2-phase operation.

When the FAN5182 is enabled, the controller outputs a voltage on PWM3, which is approximately 675mV. An internal comparator checks this pin's voltage versus a threshold of 300mV. If the PWM3 pin is grounded, it is below the threshold and the phase 3 is disabled. The output resistance of the PWM pin is approximately 5kΩ during this detection period. Any external pull-down resistance connected to the PWM pin should not be less than 25kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase-detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM3 output is not grounded, the 5kΩ resistance is disconnected, and PWM3 switches between 0V and 5V. If the PWM3 output is grounded, the controller operates in 1- and/or 2-phase.

The PWM outputs logic-level signals to interface with external gate drivers, such as the FAN5109. Since each phase is able to operate close to 100% duty cycle, more than one PWM output can be on at the same time.

Master Clock Frequency

The clock frequency is set by an external resistor connected from the RT pin to ground. The frequency / resistor relationship follows the graph in Figure 4. To determine the frequency per phase, divide the clock frequency by the number of phases in use.

NOTE: The exception is single-phase operation, in which the clock frequency must be set twice the single-phase frequency required.

Output Voltage Differential Sensing

The FAN5182 uses a differential low-offset voltage error amplifier to maintain ±2% differential sensing accuracy over temperature. The output voltage is sensed between the FB and FBRTN pins. The power supply output connects to the FB pin through a resistor divider and the FBRTN pin should be connected directly to the remote sense ground. The internal precision reference is referenced to FBRTN, which has a typical current of 100µA to allow accurate remote sensing. The internal error amplifier compares the precision reference to the FB pin to regulate the output voltage.

Output Current Sensing

The FAN5182 uses a current sense amplifier (CSA) to monitor the total output current for current-limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element, such as the low-side MOSFET. This amplifier can be configured according to the objectives of the system design:

- Output inductor DCR sensing without a thermistor (for lowest cost)
- Output inductor DCR sensing with a thermistor (for improved accuracy and moderate cost)
- Discrete resistor sensing (for best accuracy)

The positive input of the CSA is connected to the CSREF pin and the CSREF is tied to the power supply output. The inverting input of the CSA, CSSUM, is the summing node of the load current sense through sensing elements (such as the switch node side of the output inductors). The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. The current information is given as the difference between CSREF and CSCOMP. This “difference” signal is used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have low-input offset voltage. The CSA gain is determined by external resistors, so it can be set very accurately.

Current Control Loop and Thermal Balance

The FAN5182 adopts low-side MOSFET R_{DSON} sensing for phase-current balance. The sensed individual phase current is combined with a fixed internal ramp, then compared with the common voltage error amplifier output to balance phase current. This current-balance information is independent of the average output current information used for the current limit.

The magnitude of the internal ramp can be set to optimize transient response of the system. It also tracks the supply voltage for better line regulation and transient response. A resistor connected from the power supply input to the RAMPADJ pin determines the slope of the internal PWM ramp. Resistors R_{SW1} through R_{SW3} (see Figure 7) can be used to adjust phase current balance. Putting placeholders for these resistors during the initial PCB layout allows phase-current balance fine adjustments on the bench if necessary.

To increase the current in any given phase, increase R_{SW} for that phase (make R_{SW} = 0Ω for the hottest phase as the starting point). Increasing R_{SW} to 500Ω could typically make a substantial increase in this particular phase current. Increase each R_{SW} value by small amounts to optimize phase-current balance, starting with the coolest phase.

Voltage Control Loop

A high gain bandwidth voltage error amplifier is used for the voltage control loop. The non-inverting input of the error amplifier is derived from the internal 800mV reference. The output of the error amplifier, the COMP pin sets the termination voltage for the internal PWM ramps plus sensed phase current.

The inverting input (FB) is tied to the center point of a resistor divider from the output voltage sense point. Closed-loop compensation is realized via compensator networks connecting to the FB and COMP pins.

Soft-Start

The soft-start rise time of the output voltage is set by a parallel capacitor and resistor between the DELAY pin and ground. The resistor capacitor (RC) time constant also determines the current-limit latch-off delay time, as explained in the following section. In UVLO or when EN is logic low, the DELAY pin is held to ground. After the UVLO threshold is reached and EN is in logic high state, the delay capacitor is charged with an internal 20µA current source. The output voltage follows the ramping voltage on the DELAY pin to limit the inrush current. The soft-start time depends on the value of C_{DLY} with a secondary effect from R_{DLY}.

If either EN is logic low or V_{CC} drops below UVLO, the delay capacitor resets to ground and is ready for another soft-start cycle.

Figure 8 shows typical start-up waveforms for a soft-start sequence.

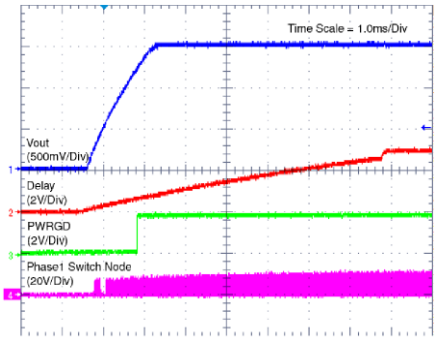

Figure 8. Typical Start-Up Waveforms

Current-Limit and Latch-off Protection

The FAN5182 compares a programmable current-limit set point to the voltage from the output of the current-sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3V. The current through the external resistor is internally scaled to give a current-limit threshold of 10.4mV/µA. If the difference in voltage between CSREF and CSCOMP rises above the current-limit threshold, the internal current-limit amplifier controls the COMP voltage to maintain the power supply output current at the over-current level.

After the limit is reached, the 3V pull-up voltage source on the DELAY pin is disconnected and the external delay capacitor discharges through the external resistor. A comparator monitors the DELAY pin voltage and shuts off the controller when the voltage drops below 1.8V. The current-limit latch-off delay time is therefore set by the RC time constant discharging the delay voltage from 3V to 1.8V. Typical over-current latch-off waveforms are shown in Figure 9.

The controller continues to switch all phases during the latch-off delay time. If the over-current condition is removed before the 1.8V delay threshold is reached, the controller resumes normal operation. The over-current recovery characteristic also depends on the state of PWRGD. If the output voltage is within the PWRGD window during over current, the controller resumes normal operation once the over-current condition is removed. If over-current causes the output voltage to drop below the PWRGD threshold, a soft-start cycle is initiated.

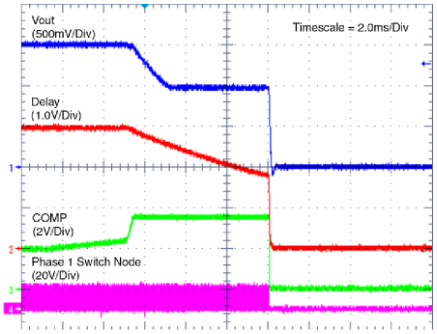

Figure 9. Over-Current Latch-Off Waveforms

The latch-off function can be reset by removing and reapplying V_{CC} or by pulling the EN pin low briefly. To disable the over-current latch-off function, the external resistor connecting the DELAY pin and ground should be removed and a high-value resistor (>1MΩ) should be connected from the DELAY pin to V_{CC}. This prevents the delay capacitor from discharging, so the 1.8V threshold can never be reached. This pull-up resistor has some impact to the soft-start time because the current through this resistor adds additional current to the internal 20µA soft-start current.

During start-up, when the output voltage is below 200mV, a secondary current limit is activated. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit clamps the COMP voltage to 2V.

An inherent, per-phase current limit protects individual phases if one or more phases cease to function because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Power-Good Monitoring

The power-good comparator monitors the output voltage via the FB pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the Electrical Characteristic table. PWRGD goes low if the output voltage is outside the specified range or whenever the EN pin is pulled low. Figure 10 shows the PWRGD response when the input power supply is switched off.

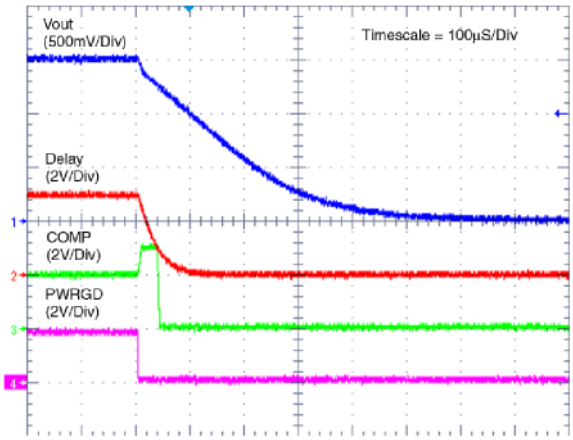

Figure 10. Shutdown Waveforms

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the crowbar trip point. This crowbar action stops once the output voltage falls below the reset threshold of approximately 650mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this crowbar action can trip the input supply over-current protection or blow the input fuse, protecting the load from damage.

Enable and UVLO

To begin switching, the input supply (V_{CC}) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is logic low, the FAN5182 is disabled. This holds the PWM outputs at ground, shorts the delay capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the OD pins of the FAN5109 drivers. Grounding the ILIMIT pin disables the drivers such that both HDRV and LDRV hold low. This feature is important in preventing fast discharge of the output capacitors when the controller shuts off. If the driver outputs are not disabled, a negative output voltage can be generated due to high current discharged from the output capacitors through the inductors.

FAN5182 in Single-Phase Applications

NOTE: When the FAN5182 is configured for single-phase applications, it is actually operating internally as a two-phase controller. It therefore should be configured as a two-phase controller with only one phase populated externally.

To accomplish this, PWM3 needs be grounded (to configure the FAN5182 as a two-phase controller) and the clock frequency set to two times the required phase switching frequency. PWM1 should be used to drive the external phase electronics (driver and MOSFETs). The SW2 and SW3 pins should be connected to ground to minimize any potential spurious noise paths.

WARNING: **Do not connect PWM2 to ground.** As noted above, when using the FAN5182 in single-phase applications, it is actually operating internally as a two-phase controller and PWM2 may be switching.

FAN5182 as a Voltage-Mode Controller

The SW pins are used to measure the current flowing through the bottom FET. This current information is used to balance the phase currents in a multiphase application and create an inner current-feedback loop in the control loop, making the FAN5182 a current-mode controller.

In single-phase applications where phase current balance is not required, the current loop can be defeated by disconnecting the SW pins from the output FETs and shorting the SW pin to ground. This changes the control loop from current-mode control to voltage-mode control.

WARNING: The compensation requirements for a voltage-mode control design differ for current-mode control design. The *Application Information* section of this datasheet is for a current-mode control design. The compensation section “Closed-Loop Compensation Design” does not apply to voltage-mode designs.

Application Information

Design parameters for a typical high-current DC/DC buck converter, as shown in Figure 7, follow. This is a multiphase, current-mode control implementation. The equations shown are interdependent and must be followed in the sequence shown. For other implementations, adjust the design requirements.

NOTE: A complete MathCAD® control design program is available from Fairchild upon request.

Design Requirements:

- Input voltage (V_{IN}) = 12V
- Output voltage (V_{OUT}) = 1.8V
- Duty cycle (D) = 0.15
- Output current I_O = 55A
- Maximum output current (I_{LIM}) = 110A
- Number of phases (n) = 3
- Switching frequency per phase (f_{SW}) = 250kHz

Setting the Clock Frequency

The FAN5182 uses fixed-frequency control architecture. The frequency is set by an external timing resistor (R_T). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and the input and output capacitors. With n = 3 for three phases, a clock frequency of 750kHz sets the switching frequency, f_{SW}, of each phase to 250kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components.

Equation 1 shows that to achieve a 750kHz oscillator frequency, the correct value for R_T is 255kΩ. Alternatively, the value for R_T can be calculated using:

$$R_T = \frac{1}{n \times f_{SW} \times 4.7pF} - 27K\Omega$$
$$R_T = \frac{1}{3 \times 250kHz \times 4.7pF} - 27K\Omega = 256K\Omega \quad \text{EQ. 1}$$

where 4.7pF and 27kΩ are internal IC component values. For good initial accuracy and frequency stability, a 1% resistor is recommended. The closest standard 1% value for this design is 255kΩ.

NOTE: For a single-phase application, set the oscillator frequency to two times the required per-phase switching frequency. This can be done buy substituting "2 x f_{SW}" for "f_{SW}" in Equation 1.

Soft-Start and Current-Limit Latch-off Delay Time

Because the soft-start and current-limit latch-off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set C_{DLY} for the soft-start ramp. This ramp is generated with a 20µA internal current source. The value of R_{DLY} has a second-order impact on the soft-start time because it sinks part of the current source to ground. As long as R_{DLY} is greater than 200kΩ, this effect is minor.

The value for C_{DLY} can be approximated using:

$$C_{DLY} = \left(20\mu A - \frac{V_{REF}}{2 \times R_{DLY}}\right) \times \frac{t_{SS}}{V_{REF}} \quad \text{EQ. 2}$$

where t_{SS} is the desired soft-start time. Assuming an R_{DLY} of 390kΩ and a desired soft-start time of 3ms, C_{DLY} is 71nF. The closest standard value for C_{DLY} is 68nF. Once C_{DLY} is chosen, R_{DLY} can be calculated for the current-limit latch-off time, using:

$$R_{DLY} = \frac{1.96 \times t_{DELAY}}{C_{DLY}} \quad \text{EQ. 3}$$

If the result for R_{DLY} is less than 200kΩ, a smaller soft-start time should be considered, by recalculating the equation for C_{DLY}, or a longer latch-off time should be used. R_{DLY} should never be less than 200kΩ. In this example, a delay time of 9ms results in R_{DLY} = 259kΩ. The closest standard 1% value is 261kΩ.

Inductor Selection

The inductance determines the ripple current in the inductor. Small inductance leads to high ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs and vise versa. In any multiphase converter, it's recommended to design the peak-to-peak inductor ripple current to be less than 50% of the maximum inductor DC current.

Equation 4 shows the relationship among the inductance, oscillator frequency, and peak-to-peak ripple current:

$$I_R = \frac{V_{OUT} \times (1 - D)}{f_{SW} \times L} \quad \text{EQ. 4}$$

Equation 5 can be used to determine the minimum inductance based on a given output ripple voltage:

$$L \geq \frac{V_{OUT} \times R_x \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad \text{EQ. 5}$$

where R_X is the ESR of output bulk capacitors.

Solving Equation 5 for a 20mV peak-to-peak output ripple voltage and 3mΩ RX yields:

$$L \geq \frac{1.8V \times 0.7m\Omega \times (1 - (3 \times 0.15))}{250kHz \times 10mV} = 277nH \quad \text{EQ. 6}$$

If the resulting ripple voltage is too low, the inductance can be reduced until the desired ripple voltage is achieved. In this example, a 600nH inductor is a good starting point that produces a calculated ripple current of 6.6A. The inductor should not saturate at the peak current of 21.6A and should be able to handle the total power dissipation created by the copper and core loss.

Another important factor in the inductor design is the Direct Conversion Receiver (DCR), which is used for measuring the phase current. A large DCR can cause excessive power losses, whereas too small DCR can increases measurement error. For this design, a DCR of 1.4mΩ was chosen.

Designing an Inductor

Once the inductance and DCR are known, the next step is to either design an inductor or find a suitable standard inductor if one exists. Inductor design starts with choosing appropriate core material. Some candidate materials that have low core loss at high frequencies are powder cores (e.g. Kool-Mμ® from Magnetics, Inc. or from Micrometals) and gapped soft ferrite cores (e.g. 3F3 or 3F4 from Philips). Powdered iron cores have higher core loss and are used for low-cost applications.

The best choice for a core geometry is a closed-loop type, such as a potentiometer core, a PQ/U/E core, or a toroid core.

Some useful references for magnetics design are:

- Magnetic Designer Software
- Intusoft (www.intusoft.com)
- *Designing Magnetic Components for High-Frequency DC-DC Converters*, by William T. McLyman, Kg Magnetics, Inc., ISBN 1883107008.

Selecting a Standard Inductor

The following power inductor manufacturers can provide design consultation and deliver power inductors optimized for high-power applications upon request:

- BI Technologies, 714-447-2345
  www.bitechnologies.com
- Taiyo Yuden (USA), 408-573-4150
  www.taiyo-yuden.com

Output Current Sense

The output current can be measured by summing the voltage across each inductor and passing the signal through a low-pass filter. The CS amplifier is configured with resistors $R_{PH(X)}$ (for summing the voltage), and R_{CS} and C_{CS} (for the low-pass filter).

The output current IO is set by the following equations:

$$I_O = \frac{R_{PH(x)}}{R_{CS}} \times \frac{V_{DRP}}{R_L} \quad \text{EQ. 7}$$

$$Ccs \geq \frac{L}{R_L \times R_{CS}} \quad \text{EQ. 8}$$

where:

R_L is the DCR of the output inductors,

V_{DRP} is the voltage drop from C_{SCOMP} to C_{SREF}.

When load current reaches its limit, V_{DRP} is at its maximum (V_{DRPMAX}). V_{DRPMAX} can be in the range of 100mV to 200mV. In this example, it is 110mV.

Designers have the flexibility of choosing either R_{CS} or $R_{PH(X)}$. It is recommended to select R_{CS} equal to 100kΩ, and then solve for $R_{PH(X)}$ by rearranging Equation 7 as:

$$R_{PH(x)} = R_L \times R_{CS} \times \frac{I_{LIM}}{V_{DRPMAX}} \quad \text{EQ. 9}$$

$$R_{PH(x)} = 1.4m\Omega \times 100k\Omega \times \frac{110A}{110mV} = 140k\Omega \quad \text{EQ. 10}$$

WARNING: The parallel combination of the all the R_{ph} resistors must be greater than 30kΩ to ensure that the current sense amplifier does not saturate.

Next, use Equation 8 to solve for C_{CS}:

$$Ccs \geq \frac{320nH}{1.4m\Omega \times 100k\Omega} \geq 2.28nF \quad \text{EQ. 11}$$

Choose the closest standard value that is greater than the result given by Equation 8. This example uses a C_{CS} value of 5.6nF.

Output Voltage

FAN5182 has an internal FBRTN referred 800mV reference voltage VREF. The output voltage can be set by using a voltage divider consisting of resistors R_{B1} and R_{B2}:

$$V_{OUT} = \frac{(R_{B1} + R_{B2})}{R_{B1}} \times V_{REF} \quad \text{EQ. 12}$$

Rearranging Equation 12 to solve R_{B2} and assuming a 1%, 1kΩ resistor for RB1 yields

$$R_{B2} = \frac{V_{OUT} - V_{FB}}{V_{FB}} \times R_{B1}$$
$$R_{B2} = \frac{1.8V - 0.8V}{0.8V} \times 1k\Omega = 1.25k\Omega \quad \text{EQ. 13}$$

The closest standard 1% resistor value for R_{B2} is 1.24kΩ.

Power MOSFETs

For this example, one high-side and one low-side N-channel power MOSFET per phase have been selected. The main selection parameters for power MOSFETs are $V_{GS(TH)}$, Q_G, C_{ISS}, C_{RSS}, and $R_{DS(ON)}$. The minimum gate-drive voltage (the supply voltage to the FAN5109) dictates whether standard threshold or logic-level threshold MOSFETs can be used. With V_{GATE} ~10V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5V) are recommended.

The maximum output current (I_O) determines the $R_{DS(ON)}$ requirement for the low-side (synchronous) MOSFETs. With good current balance among phases, the current in each low-side MOSFET is the output current divided by the total number of the low-side MOSFETs (n_{SF}). Since conduction loss is dominant in low-side MOSFET, the following expression can represent total power dissipation in each synchronous MOSFET in terms of the ripple current per phase (I_R) and the total output current (I_O):

$$P_{SF} = (1-D) \times \left[\left(\frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad \text{EQ. 14}$$

Knowing the maximum output current and the maximum allowed power dissipation, determine the required $R_{DS(ON)}$ for the MOSFET. For example, with D-PAK MOSFETs operating up to ambient temperature of 50°C, a safe limit for PSF is around 1W to 1.5W at 120°C junction temperature. Therefore, in this example, $R_{DS(SF)}$ (per MOSFET) < 7.5mΩ. This $R_{DS(SF)}$ is typically measured at junction temperature of about 120°C. In this example, select a lower-side MOSFET with 4.8mΩ at 120°C.

WARNING: The R_{DS} of the bottom FET is also used to measure the current flowing in the phase. This is used for current balance and for the current-feedback loop. Using a FET with too low an R_{DS} can result in poor current balance and too large a ramp resistor calculation in Equation 18.

Another important consideration for choosing the synchronous MOSFET is the input and feedback capacitance. The ratio of feedback to input capacitance must be small (less than 10% is recommended) to prevent accidentally turning on the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non-overlap dead time of the MOSFET driver (40ns typical for the FAN5109). The output impedance of the driver is approximately 2Ω and the typical MOSFET input gate resistances are about 1Ω to 2Ω; therefore, the total gate capacitance should be less than 6000pF. In the event there are two MOSFETs in parallel, the input capacitance for each synchronous MOSFET should be limited to 3000pF.

The high-side (main) MOSFET power dissipation consists of two elements: conduction and switching losses. The switching loss is related to the main MOSFET's turn-on and turn-off time and the current and voltage being switched. Based on the main MOSFET's switching speed (rise and fall time that the gate driver can offer) and MOSFET input capacitance, the following expression provides the approximate switching loss for each main MOSFET:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{ISS} \qquad \text{EQ. 15}$$

where:

n_{MF} is the total number of main MOSFETs;

R_G is the total gate resistance (2Ω for the FAN5109 and about 1Ω for typical logic level N-channel MOSFETs, total RG = 3Ω);

C_{ISS} is the input capacitance of the main MOSFET.

Note that adding more main MOSFETs (n_{MF}) does not help lower the switching loss for each main MOSFET; it can only reduce conduction loss. The most efficient way to reduce switching loss is to use low-gate charge / capacitance devices.

The conduction loss of the main MOSFET is given by:

$$P_{C(MF)} = D \times \left[\left(\frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left(\frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \qquad \text{EQ. 16}$$

where $R_{DS(MF)}$ is the on resistance of the main MOSFET.

Typically, for main MOSFETs, a low gate charge (C_{ISS}) device is preferred, but low gate charge MOSFETs usually have higher on resistance. Select a device that meets total power dissipation around 1.5W for a single D-PAK MOSFET.

In this example, a FDD6296 is selected as the main MOSFET (three total; nMF = 3), with a CISS = 1440pF, and RDS(MF) = 9mΩ (at TJ = 120°C). A FDD8896 is selected as the synchronous MOSFET (three total; nSF = 3), with C_{ISS} = 2525pF and $R_{DS(SF)}$ = 5.4mΩ (at T_J = 120°C). The synchronous MOSFET C_{ISS} is less than 6000pF. Solving for the power dissipation per MOSFET at I_O = 55A and I_R = 6.6A yields 1.56W for each synchronous MOSFET and 1.29W for each main MOSFET. These numbers comply with the power dissipation limit of around 1.5W per MOSFET.

One more item that needs to be considered is the power dissipation in the driver for each phase. The gate-drive loss is described in terms of the Q_G for the MOSFETs and is given by the following equation:

$$P_{DRV} = \left[\frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times V_{CC} \qquad \text{EQ. 17}$$

where:

Q_{GMF} is the total gate charge for each main MOSFET,

Q_{GSF} is the total gate charge for each synchronous MOSFET.

$I_{CC} \times V_{CC}$ in Equation 17 represents the driver's standby power dissipation. For the FAN5109, the maximum dissipation should be less than 400mW. In this example, with I_{CC} = 5mA, Q_{GMF} = 25nC, and Q_{GSF} = 50nC; there is 285mW in each driver, which is below the 400mW dissipation limit. See the Thermal Information table in the FAN5109 datasheet for details.

Ramp Resistor Selection

The ramp resistor (R_R) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of phase-current balance, stability, and transient response.

The following expression is used to determine the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS(ON)(SF)} \times C_R} \qquad \text{EQ. 18}$$

$$R_R = \frac{0.2 \times 320\text{nH}}{3 \times 5 \times 2.4\text{m}\Omega \times 5\text{pF}} = 356\text{k}\Omega \qquad \text{EQ. 19}$$

where:

- A_R is the internal ramp amplifier gain,
- A_D is the current balancing amplifier gain,
- $R_{DS(ON)(SF)}$ is the equivalent low-side MOSFET on resistance,
- C_R is the internal ramp capacitor value.

The closest standard 1% resistor value is 332kΩ.

WARNING: The ramp resistor should be less than 1MΩ to ensure that board contaminates don't affect the ramp. If the calculated value is greater than 1MΩ, verify that the R_{DS} of the bottom FET is not too low.

Internal ramp voltage magnitude can be calculated by:

$$V_R = \frac{A_R \times (1-D) \times V_{OUT}}{R_R \times C_R \times f_{SW}} \quad \text{EQ. 20}$$

$$V_R = \frac{0.2 \times (1-0.15) \times 1.8V}{357K\Omega \times 5pF \times 250kHz} = 686mV \quad \text{EQ. 21}$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response improve, but thermal balance degrades. If the ramp is made smaller, thermal balance improves, but transient response and stability degrade. The factor of three in the denominator of Equation 18 sets a ramp size with optimal balance for good stability, transient response, and thermal balance.

Ramp Resistor Selection for Voltage-Mode Control

When configured for single-phase voltage-mode control (SW pin grounded), the ramp resistor is selected to produce a fixed-ramp voltage. For example, to create a ramp voltage of 1V, the following equation is used:

$$R_R = \frac{0.2 \times (Vin - Vref) \times Vout}{Vin \times Fsw \times C_R \times dVr} - 2000 \quad \text{EQ. 22}$$

where:

- R_{RAMP} is the ramp resistor connected between V_{IN} and FAN5182 RAMPADJ pin 9
- 0.2 is the internal current transfer ratio between $R_{RAMPADJ}$ and the PWM ramp current source(s)
- V_{IN} is the input voltage (12V)
- V_{REF} is the internally generated reference (0.8V)
- V_{OUT} is the output voltage
- C is the internal PWM ramp capacitor, 5pF
- f_{sw} is the switching frequency defined as (Master Osc / 2) for single- and dual-phase operation and (Master Osc / 3) for three-phase operation
- d_{Vr} is the target peak ramp voltage; 1V is a typical target voltage.

Current Limit Set Point

The current-limit threshold is set with a 3V source V_{LIM} across R_{LIM} with a gain of 10.4mV/µA (A_{LIM}).

R_{LIM} can be found using:

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{V_{DRPMAX}} \quad \text{EQ. 23}$$

WARNING: Be sure to take into account the peak current ripple current and the increase in inductor DCR at high temperatures if the inductor is not temperature compensated.

If R_{LIM} is greater than 500kΩ, the actual current-limit threshold may be lower than the intended value. Some adjustment for R_{LIM} may be needed. Here, I_{LIM} is the average current limit for the output of the supply. In this example, using the V_{DRPMAX} value of 110mV from Equations 7 and 8 and choosing a peak current limit of 110A for I_{LIM} results in R_{LIM} = 284kΩ, for which 287kΩ is chosen as the nearest 1% value.

The per-phase current limit is determined by:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} + \frac{I_R}{2} \quad \text{EQ. 24}$$

Closed-Loop Compensation Design

NOTE: This section does not apply in a voltage-mode control configuration.

Optimum compensation assures the best possible load regulation and transient response of the regulator. The target of the compensation design is to achieve reasonably high control bandwidth with sufficient phase and gain margin.

The power stage of the synchronous buck converter consists of two poles and one zero. A two-pole, one-zero compensator of the voltage error amplifier is adequate for proper compensation if the output bulk capacitors are electrolytic types (low ESR zero). Equations 25-27 are able to yield an approximate starting point for the design. To further optimize the design, some bench adjustments may be necessary.

$$C_A = \frac{C_X \times R_X}{R_{B2}} \times \left(\frac{n \times R_X}{\left(\frac{V_R}{V_{OUT}} \times R_L \right) + \left(A_D \times R_{DS} \right)} \right) \quad \text{EQ. 25}$$

$$R_A = \frac{R_{B2}}{C_X \times R_X} \times \frac{V_R}{V_{OUT}} \times \left(\frac{L}{n \times R_X} - \frac{A_D \times R_{DS}}{2 \times f_{sw} \times R_X} - C_X \times R_X \right) \quad \text{EQ. 26}$$

$$C_{FB} = \frac{1}{2 \times n \times f_{sw} \times R_A} \quad \text{EQ. 27}$$

If C_X is 6000µF (five 1200µF capacitors in parallel) with an equivalent ESR of 3mΩ, the equations above give the following compensation values:

C_A = 1.33nF, R_A= 6.05kΩ, C_{FB} = 110pF EQ. 28

Selecting the nearest standard value for each of these components yields:

C_A = 1.2nF, R_A = 6.04kΩ, and C_{FB} = 100pF EQ. 29

As mentioned above, this compensation design scheme is typically good for applications using electrolytic type capacitors, where the capacitor ESR zero can roughly cancel one of the power stage poles. However, for all ceramic capacitor types of applications, since the capacitor ESR zero can be very high, a three-pole, two-zero compensator should be used.

Input Capacitor Selection and Input Current di/dt Reduction

In continuous inductor current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to D × V_{OUT}/V_{IN} and an amplitude equal to the output current. To prevent large voltage variation, a low-ESR input capacitor, sized for the maximum rms current, must be used. The maximum rms capacitor current is given by:

$$I_{CRMS} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad \text{EQ. 30}$$

$$I_{CRMS} = 0.15 \times 55A \times \sqrt{\frac{1}{3 \times 0.15} - 1} = 9.1A \quad \text{EQ. 31}$$

Note that manufacturers often specify capacitor ripple current rating based on only 2,000 hours of life. Therefore, it is advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by two 2,700µF, 16V aluminum electrolytic capacitors and three 4.7µF ceramic capacitors.

To reduce the input current di/dt to a level below the system requirement, in this example 0.1A/µs, an additional small inductor (L > 370nH at 10A) can be inserted between the converter and the supply bus. This inductor serves as a filter between the converter and the primary power source.

WARNING: During start-up with a pre-charged output capacitor the capacitor, is discharged prior to the converter starting. The energy that was stored in the output capacitor is transferred to the input voltage through the upper FET. This can cause a momentary increase in V_{IN} that could exceed the V_{IN} maximum specification for the controller or driver if there is insufficient capacitance on V_{IN}.

To ensure that this does not happen, use the following equation to calculate a minimum value of C_{IN}:

$$C_{IN} = C_{OUT} \cdot \frac{V_O^6}{V_{INMax}^2 - V_{INNorm}^2} \quad \text{EQ. 32}$$

Inductor DCR Temperature Correction

With the inductor's DCR being used as the sense element, its necessary to compensate for temperature changes in the inductor's winding if an accurate current-limit set point is desired. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If R_{CS} is designed to have an opposite and equal percentage of change in resistance to that of the inductor wire, it cancels the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors R_{CS1} and R_{CS2} are needed. See Figure 11 for instructions on how to linearize the NTC and produce the desired temperature coefficient.

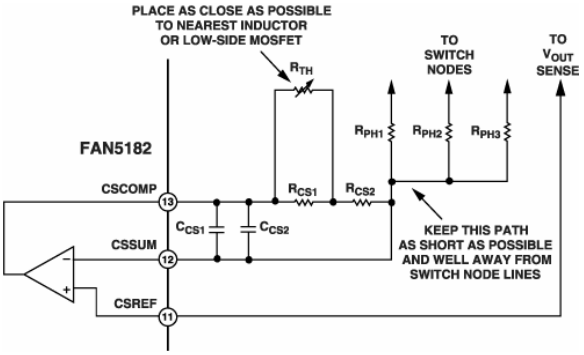

Figure 11. Temperature Compensation Circuit

Follow the procedures and expressions shown below for calculation of R_{CS1}, R_{CS2}, and R_{TH} (the thermistor value at 25°C) based on a given R_{CS} value.

1. Select an NTC according to type and value. With no value yet, start with a thermistor with a value close to R_{CS}. The NTC should also have an initial tolerance of better than 5%.
2. Based on the NTC type, find its relative resistance value at two temperatures. The temperatures that work well are 50°C and 90°C. These resistance values are called A (RTH(50°C)/RTH(25°C)) and B(RTH(90°C)/RTH(25°C)). Note that the NTC's relative value is always 1 at 25°C.
3. Find the relative value of RCS required for each of these temperatures. This is based on the percentage of change needed, which, in this example, is initially 0.39%/°C. These are called r1 (1/ (1 + TC × (T1 - 25))) and r2 (1/ (1 + TC × (T2 - 25))), where TC = 0.0039 for copper. T1 = 50°C and T2 = 90°C are chosen. From this, calculate that r1 = 0.9112 and r2 = 0.7978.
4. Compute the relative values for R_{CS1}, R_{CS2}, and R_{TH} using Equations 33, 34, and 35.

$$r_{CS2} = \frac{(A-B) \times r_1 \times r_2 - A \times (1-B) \times r_2 + B \times (1-A) \times r_1}{A \times (1-B) \times r_1 - B \times (1-A) \times r_2 - (A-B)} \quad \text{EQ. 33}$$

$$r_{CS1} = \frac{(1-A)}{\left(\frac{1}{1-r_{CS2}}\right) - \left(\frac{A}{r_1 - r_{CS2}}\right)} \quad \text{EQ. 34}$$

$$r_{TH} = \frac{1}{\left(\frac{1}{1-r_{CS2}}\right) - \left(\frac{1}{r_1 - r_{CS1}}\right)} \quad \text{EQ. 35}$$

5. Calculate R_{TH} = r_{TH} x R_{CS}, then select the closest thermistor value available. Also, compute a scaling factor k based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad \text{EQ. 36}$$

6. Calculate values for R_{CS1} and R_{CS2} using:

$$R_{CS1} = R_{CS} \times k \times r_{CS1} \quad \text{EQ. 37}$$

$$R_{CS2} = R_{CS} \times ((1-k) + (k \times r_{CS2})) \quad \text{EQ. 38}$$

PCB Layout Guidelines

General Recommendations

To achieve the best performance, a PCB with at least four layers is recommended. When designing the layout, keep in mind that each square unit of 1-ounce copper has resistance of ~0.53mΩ at room temperature.

Whenever high currents must be routed to a different PCB layers, vias should be used properly to create several parallel current paths so the resistance and inductance introduced by these current paths are minimized and via current rating is not exceeded.

If critical signal traces must be routed close to power circuitry, a signal ground plane must be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground island should be used around and under the FAN5182 as a reference for the components associated with the controller. The analog ground should be connected to the power ground at a single point.

The components around the FAN5182 should be close to the controller with short traces. The output capacitors should be placed as close as possible to the load. If the load is distributed, the capacitors should also be distributed in proportion to the respective load.

Power Circuitry Recommendations

The PCB layout starts with high-frequency power component placement. Try to minimize stray inductance of the MOSFET half bridge, which is composed of the input capacitors and top and bottom MOSFETs. A good practice is to use short and wide traces or copper pours to minimize the inductance in the MOSFET half bridge. Failure to do so can lead to severe phase node ringing. A snubber circuit is always recommended to partly kill the phase node switching noise.

Whenever using a power dissipating component; for example, a power MOSFET that is soldered to the PCB; the proper use of vias, both directly on the mounting pad and immediately surrounding the mounting pad is recommended. Make a mirror image of the power pad being used on the component side to heat sink the MOSFETs on the opposite side of the PCB. Use large copper pour for high-current traces to lower the electrical impedance and help dissipate heat. Do not make the switching node copper pour unnecessarily large, since it could radiate noise.

An undisturbed solid power ground plane should be used as one of the inner layers.

Signal Circuitry Recommendations

The output voltage is sensed from the FB and the FBRTN pins. To avoid differential mode noise pickup in these differential sensed traces, the loop area between the FB and FBRTN traces should be minimized. In other words, the FB and FBRTN traces should be routed adjacent to each other with minimum spacing on top of the analog / power ground plane back to the controller.

The signal traces connecting to the switch nodes should be tied as close as possible to the inductor pins. The CSREF sense trace should be connected to the second nearest inductor pin to the controller.

Detailed step-by-step PCB layout instructions are available from Fairchild upon request.

Physical Dimensions

Dimensions are in millimeters (inches) unless otherwise noted.

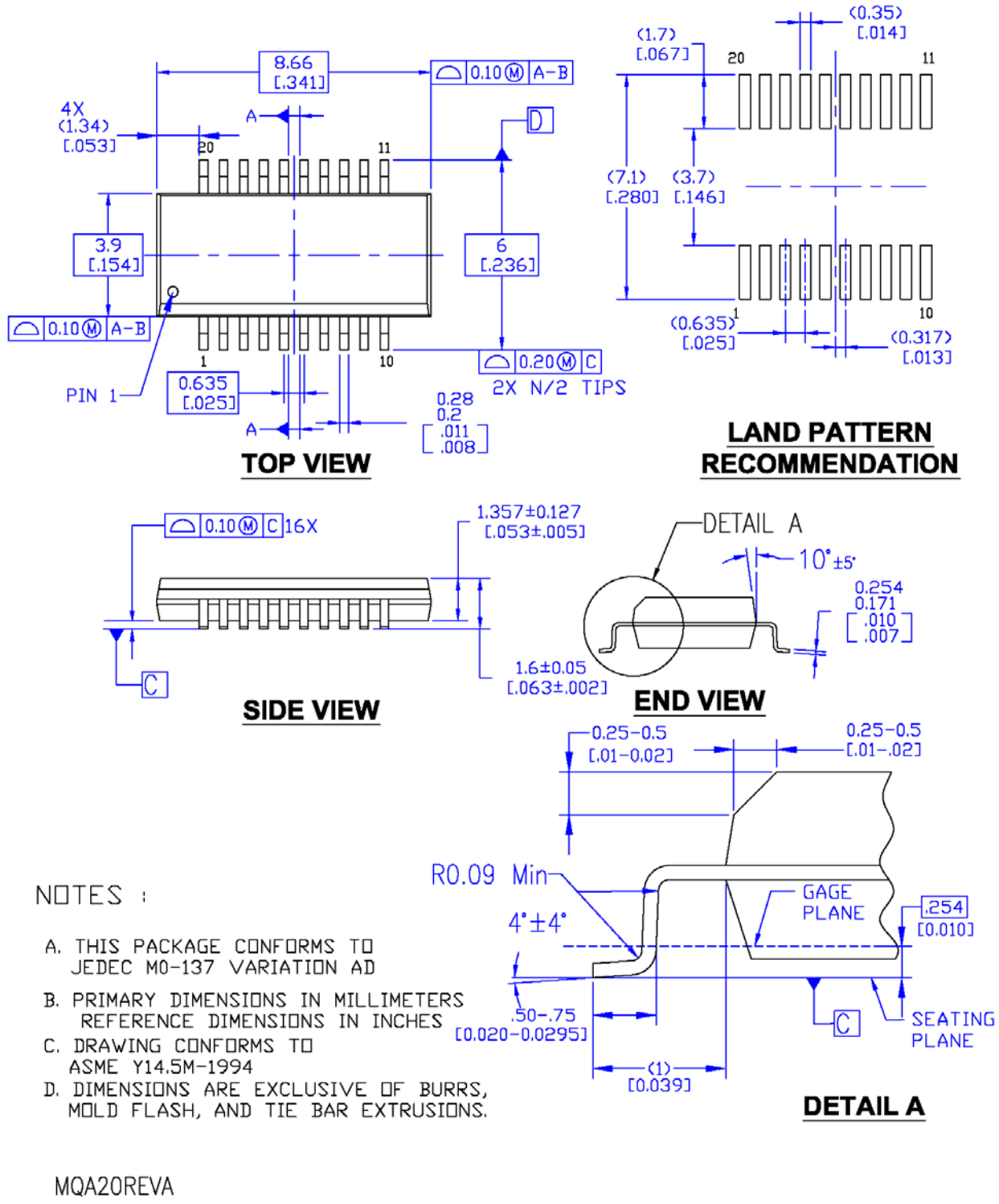

Figure 12. 20-Pin Quarter-Size Outline Package (QSOP)

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