Low Noise, Low Power, SPI® Bus, 128 Taps

The ISL22416 integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the SPI serial interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up the device recalls the contents of the DCP's IVR to the WR.

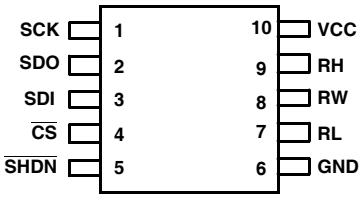
The DCP can be used as three-terminal potentiometer or as two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 128 resistor taps
- SPI serial interface
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical @ 3.3V
- Shutdown mode
- Shutdown current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years @ $T \leq 55$ °C
- 10 Lead MSOP
- Pb-free plus anneal product (RoHS compliant)

Pinout

ISL22416
(10 LD MSOP)
TOP VIEW



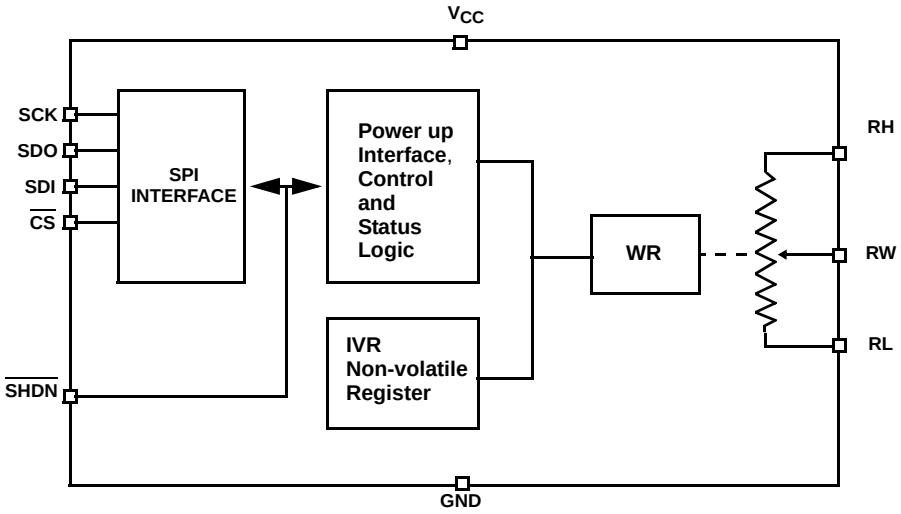
Ordering Information

PART NUMBER	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22416UFU10Z (Notes 1, 2)	416UZ	50	-40 to +125	10 Ld MSOP (Pb-Free)	M10.118
ISL22416WFU10Z (Notes 1, 2)	416WZ	10	-40 to +125	10 Ld MSOP (Pb-Free)	M10.118

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add "-TK" suffix for 1,000 Tape and Reel option

Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	SCK	SPI interface clock input
2	SDO	Push-pull/Open Drain Data Output of the SPI serial interface
3	SDI	Data Input of the SPI serial interface
4	$\overline{CS}$	Chip Select active low input
5	$\overline{SHDN}$	Shutdown active low input
6	GND	Device ground pin
7	RL	“Low” terminal of DCP
8	RW	“Wiper” terminal of DCP
9	RH	“High” terminal of DCP
10	V_{CC}	Power supply pin

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin
with Respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP pin with Respect to GND . . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA
Latchup (Note 4) . . . . . Class II, Level B @+125°C
ESD (HBM) 5kV
(CDM) 1kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
10 Lead MSOP	120

Recommended Operating Conditions

Temperature Range (Extended Industrial) . . . . . -40°C to +125°C
Power Rating 5mW
Maximum Junction Temperature . . . . . 150°C
V_{CC} . . . . . 2.7V to 5.5V
Wiper Current . . . . . ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
4. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the SHDN pin, and using a max negative pulse of -1V for all pins.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
	End-to-End Temperature Coefficient	W option		±50		ppm/°C (Note 19)
		U option		±80		ppm/°C (Note 19)
R_W	Wiper Resistance	V_{CC} = 3.3V @ 25°C, wiper current = V_{CC}/R_{TOTAL}		70	200	Ω
V_{RH}, V_{RL}	V_{RH} and V_{RL} Terminal Voltages	V_{RH} and V_{RL} to GND	0		V_{CC}	V
$C_H/C_L/C_W$ (Note 19)	Potentiometer Capacitance			10/10/25		pF
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}		0.1	1	µA
VOLTAGE DIVIDER MODE (0V @ R_L; V_{CC} @ R_H; measured at R_W, unloaded)						
INL (Note 10)	Integral Non-linearity		-1		1	LSB (Note 6)
DNL (Note 9)	Differential Non-linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 6)
ZSerror (Note 7)	Zero-scale Error	W option	0	1	5	LSB (Note 6)
		U option	0	0.5	2	
FSerror (Note 8)	Full-scale Error	W option	-5	-1	0	LSB (Note 6)
		U option	-2	-1	0	
TC_V (Note 11, 19)	Ratiometric Temperature Coefficient	DCP register set to 40 hex for W and U option		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 15)	Integral Non-linearity	DCP register set between 10 hex and 70 hex; monotonic over all tap positions; W and U option	-1		1	MI (Note 12)
RDNL (Note 14)	Differential Non-linearity	W option	-1		1	MI (Note 12)
		U option	-0.5		0.5	MI (Note 12)

Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
Roffset (Note 13)	Offset	W option	0	1	5	MI (Note 12)
		U option	0	0.5	2	MI (Note 12)

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	f_{SCK} = 5MHz; (for SPI Active, Read and Volatile Write states only)			0.5	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	f_{SCK} = 5MHz; (for SPI Active, Read and Non-volatile Write states only)			3	mA
I_{SB}	V_{CC} Current (standby)	V_{CC} = +5.5V @ +85°C, SPI interface in standby state			5	µA
		V_{CC} = +5.5V @ +125°C, SPI interface in standby state			7	µA
		V_{CC} = +3.6V @ +85°C, SPI interface in standby state			3	µA
		V_{CC} = +3.6V @ +125°C, SPI interface in standby state			5	µA
I_{SD}	V_{CC} Current (shutdown)	V_{CC} = +5.5V @ +85°C, SPI interface in standby state			3	µA
		V_{CC} = +5.5V @ +125°C, SPI interface in standby state			5	µA
		V_{CC} = +3.6V @ +85°C, SPI interface in standby state			2	µA
		V_{CC} = +3.6V @ +125°C, SPI interface in standby state			4	µA
I_{LkgDig}	Leakage Current, at Pins $\overline{SHDN}$, SCK, SDI, SDO and $\overline{CS}$	Voltage at pin from GND to V_{CC}, SDO is inactive	-1		1	µA
t_{WRT} (Note 17)	Wiper Response Time	Wiper Response Time after SPI write to WR register		1.5		µs
$t_{ShdnRec}$ (Note 19)	DCP Recall Time from Shutdown Mode	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection		1.5		µs
		SCK rising edge of last bit of ACR data byte to wiper stored position and RH connection		1.5		µs
V_{POR}	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs	2.0		2.6	V
V_{CC} Ramp	V_{CC} Ramp Rate		0.2			V/ms
t_D	Power-up Delay	V_{CC} above V_{POR}, to DCP Initial Value Register recall completed, and SPI Interface in standby state			3	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ 55 °C	50			Years
t_{WC} (Note 17)	Non-volatile Write Cycle Time			12	20	ms
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer LOW Voltage		-0.3		$0.3*V_{CC}$	V
V_{IH}	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer HIGH Voltage		$0.7*V_{CC}$		$V_{CC}+0.3$	V

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

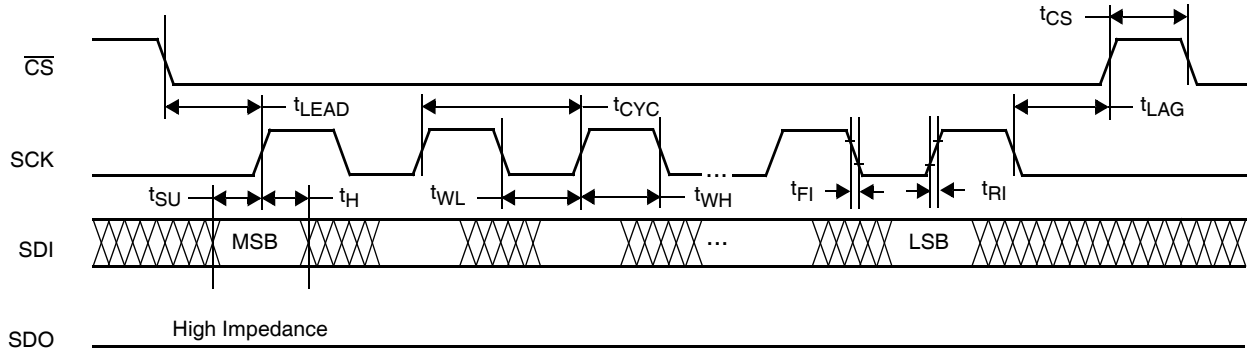
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 5)	MAX	UNIT
Hysteresis	$\overline{SHDN}$, SCK, SDI, and $\overline{CS}$ Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL}	SDO Output Buffer LOW Voltage	I_{OL} = 4mA	0		0.4	V
R_{pu} (Note 18)	SDO Pull-up Resistor Off-chip	Maximum is determined by t_{RO} and t_{FO} with maximum bus load Cb = 30pF, f_{SCK} = 5MHz			2	kΩ
Cpin (Note 19)	$\overline{SHDN}$, SCK, SDI, SDO and $\overline{CS}$ Pin Capacitance				10	pF
f_{SCK}	SPI Frequency				5	MHz
t_{CYC}	SPI Clock Cycle Time		200			ns
t_{WH}	SPI Clock High Time		100			ns
t_{WL}	SPI Clock Low Time		100			ns
t_{LEAD}	Lead Time		250			ns
t_{LAG}	Lag Time		250			ns
t_{SU}	SDI, SCK and $\overline{CS}$ Input Setup Time		50			ns
t_H	SDI, SCK and $\overline{CS}$ Input Hold Time		50			ns
t_{RI}	SDI, SCK and $\overline{CS}$ Input Rise Time		10			ns
t_{FI}	SDI, SCK and $\overline{CS}$ Input Fall Time		10		20	ns
t_{DIS}	SDO Output Disable Time		0		100	ns
t_V	SDO Output Valid Time				350	ns
t_{HO}	SDO Output Hold Time		0			ns
t_{RO}	SDO Output Rise Time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{FO}	SDO Output Fall Time	R_{pu} = 2k, Cbus = 30pF			60	ns
t_{CS}	CS Deselect Time		2			µs

Notes:

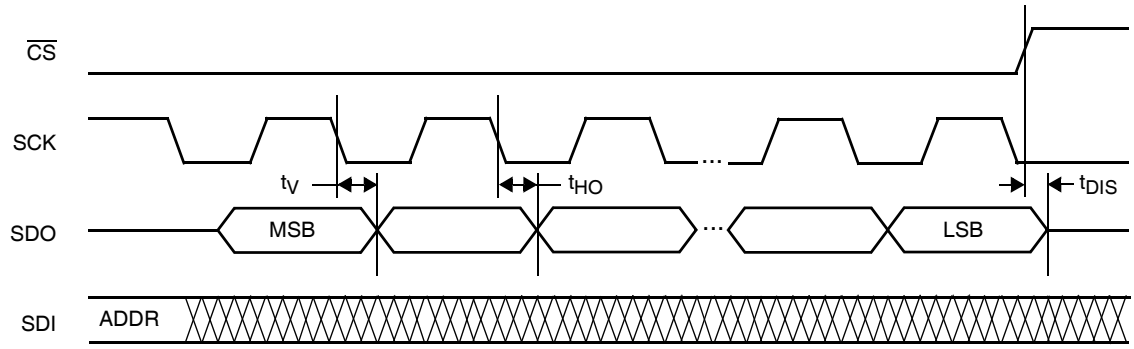
5. Typical values are for T_A = 25°C and 3.3V supply voltage.
6. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. ZS error = $V(RW)_0$/LSB.
8. FS error = $[V(RW)_{127} – V_{CC}]$/LSB.
9. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 127. i is the DCP register setting.
10. INL = $[V(RW)_i – (i • LSB) – V(RW)_0]$/LSB for i = 1 to 127
11. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 127 decimal, T = -40°C to 125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
12. MI = $|RW_{127} – RW_0|$/127. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
13. Roffset = RW_0/MI, when measuring between RW and RL.
    Roffset = RW_{127}/MI, when measuring between RW and RH.
14. RDNL = $(RW_i – RW_{i-1})$/MI -1, for i = 1 to 127.
15. RINL = $[RW_i – (MI • i) – RW_0]$/MI, for i = 1 to 127.
16. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{165°C}$ for i = 16 to 127, T = -40°C to 125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
17. t_{WC} is the time from the end of a Write sequence of SPI serial interface, to the end of the self-timed internal non-volatile write cycle.
18. R_{pu} is specified for the highest data rate transfer for the device. Higher value pull-up can be used at lower data rates.
19. This parameter is not 100% tested.

Timing Diagrams

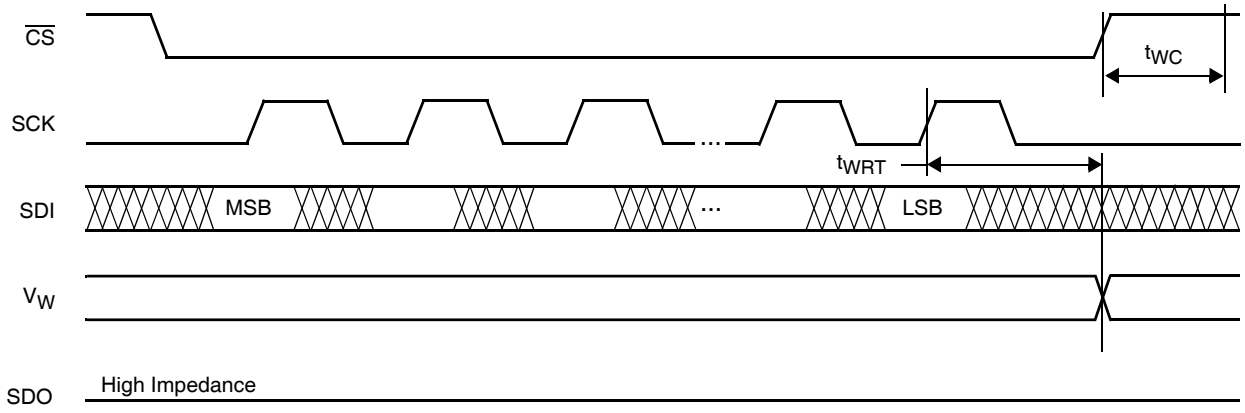
Input Timing



Output Timing



XDCP Timing (for All Load Instructions)



Typical Performance Curves

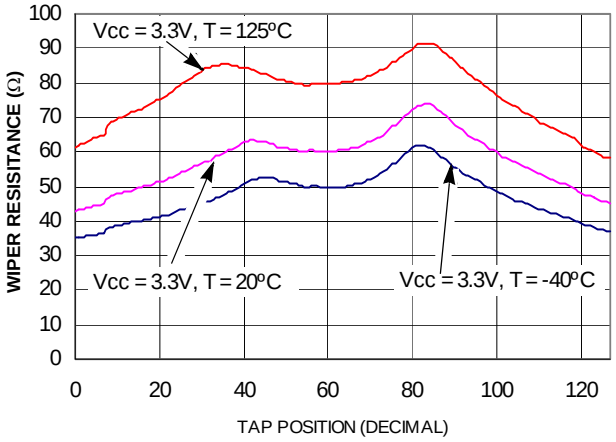


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

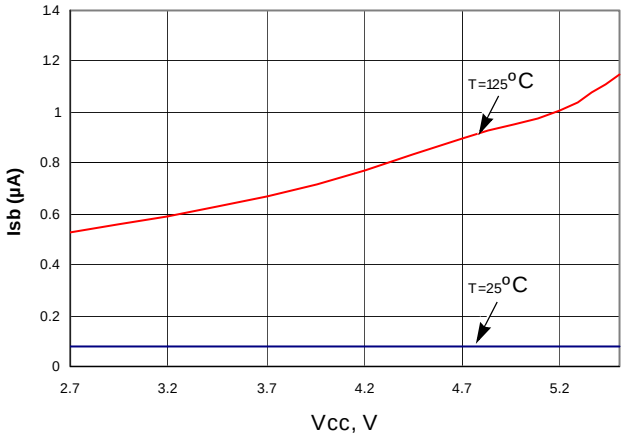


FIGURE 2. STANDBY I_{CC} vs V_{CC}

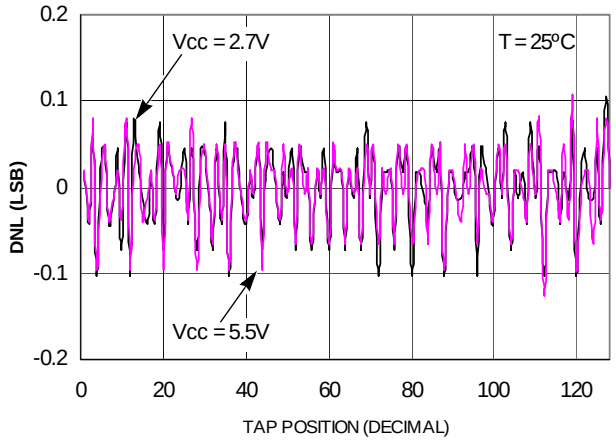


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

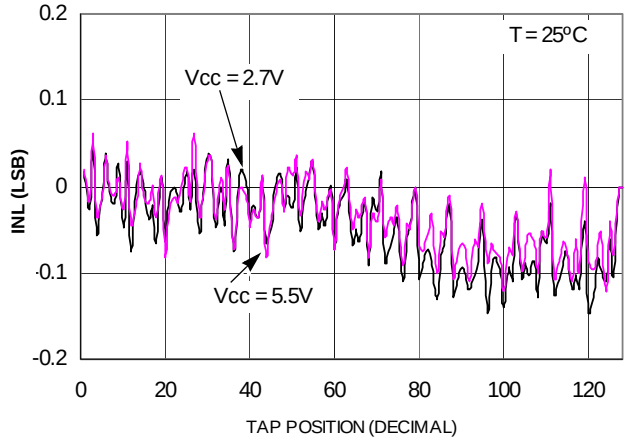


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

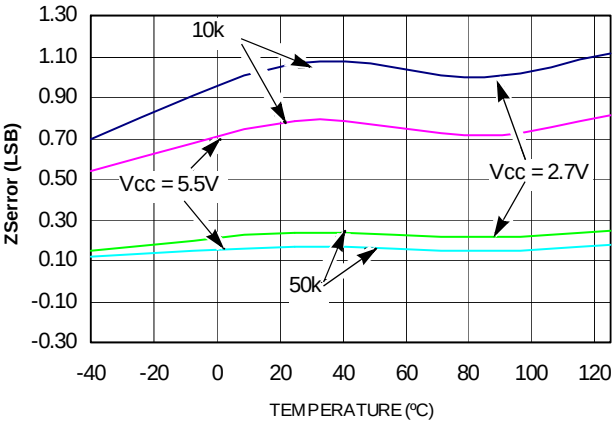


FIGURE 5. ZSerror vs TEMPERATURE

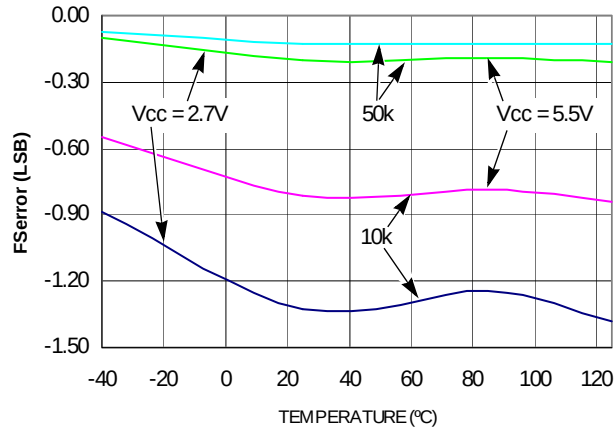


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

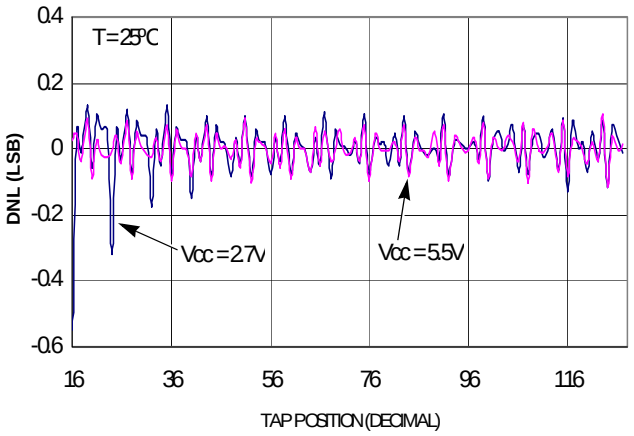


FIGURE 7. DNL vs TAP POSITION IN Rheostat MODE FOR 10kΩ (W)

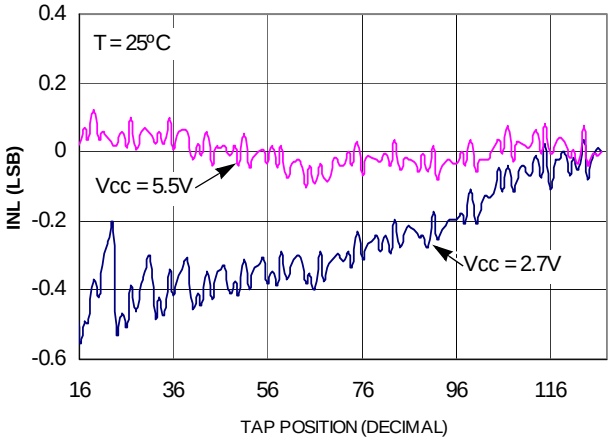


FIGURE 8. INL vs TAP POSITION IN Rheostat MODE FOR 10kΩ (W)

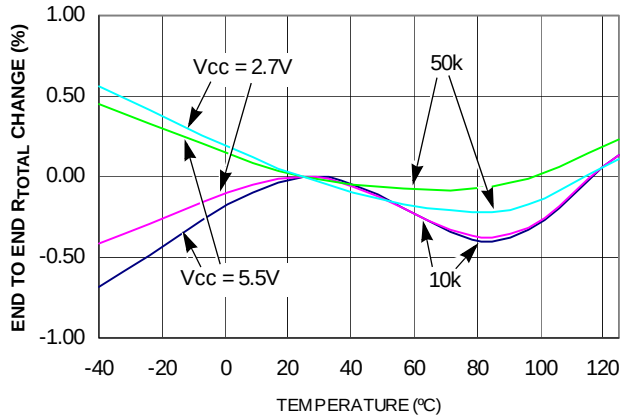


FIGURE 9. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

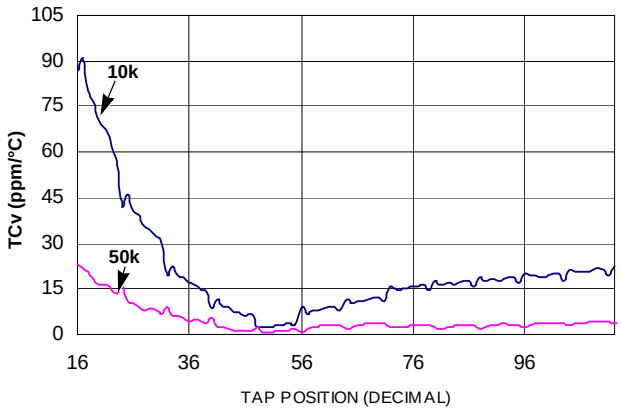


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm FOR 10kΩ (W)

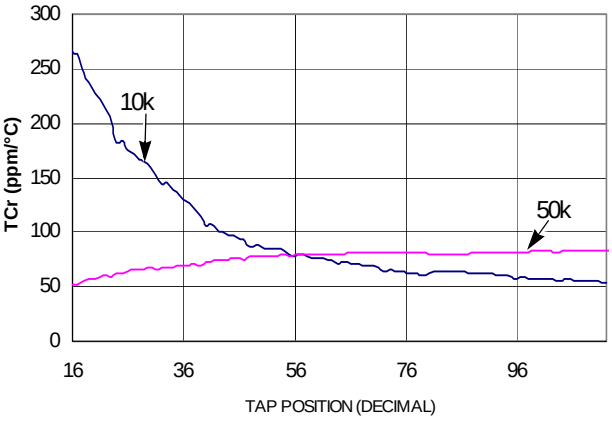


FIGURE 11. TC FOR Rheostat MODE IN ppm FOR 50kΩ (U)

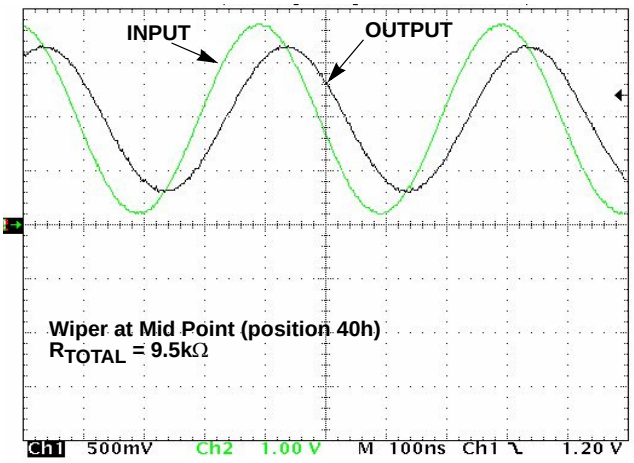


FIGURE 12. FREQUENCY RESPONSE (2.6MHz)

Typical Performance Curves (Continued)

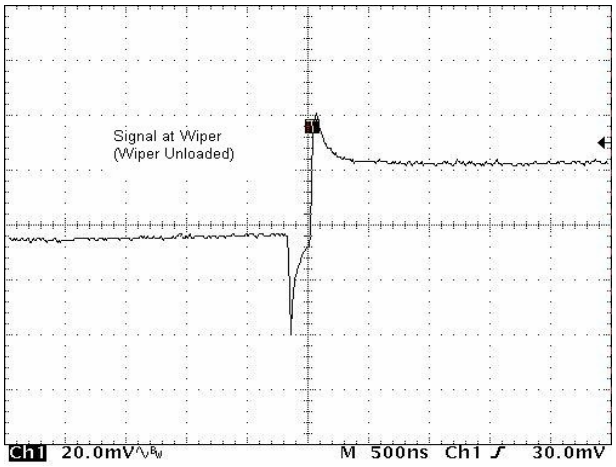


FIGURE 13. MIDSCALE GLITCH, CODE 80h TO 7Fh (WIPER 0)

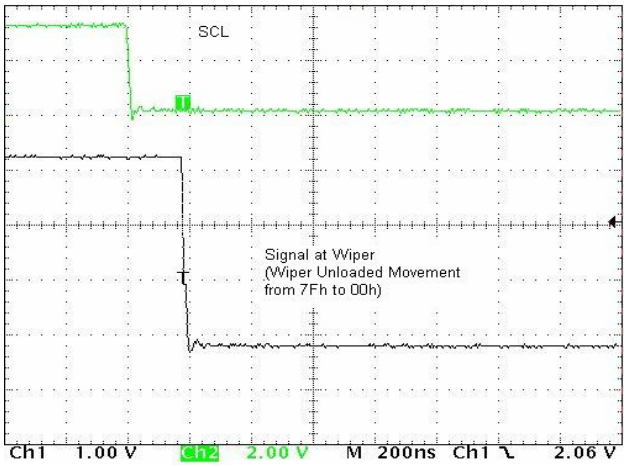


FIGURE 14. LARGE SIGNAL SETTLING TIME

Pin Description

Potentiometer Pins

RH and RL

The high (RH) and low (RL) terminals of the ISL22416 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 127 decimal, the wiper will be closest to RH, and with the WR set to 0, the wiper is closest to RL.

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

$\overline{\text{SHDN}}$

The $\overline{\text{SHDN}}$ pin forces the resistor to end-to-end open circuit condition on RH and shorts RW to RL. When $\overline{\text{SHDN}}$ is returned to logic high, the previous latch settings put RW at the same resistance setting prior to shutdown. This pin is logically OR'd with SHDN bit in ACR register. SPI interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

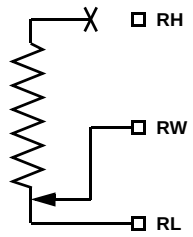


FIGURE 15. DCP CONNECTION IN SHUTDOWN MODE

Bus Interface Pins

Serial Clock (SCK)

This is the serial clock input of the SPI serial interface.

Serial Data Output (SDO)

The SDO is an open drain serial data output pin. During a read cycle, the data bits are shifted out at the falling edge of the serial clock SCK, while the $\overline{\text{CS}}$ input is low.

SDO requires an external pull-up resistor for proper operation.

Serial Data Input (SDI)

The SDI is the serial data input pin for the SPI interface. It receives device address, operation code, wiper address and data from the SPI external host device. The data bits are shifted in at the rising edge of the serial clock SCK, while the $\overline{\text{CS}}$ input is low.

Chip Select ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ LOW enables the ISL22416, placing it in the active power mode. A HIGH to LOW transition on $\overline{\text{CS}}$ is required prior to the start of any operation after power up. When $\overline{\text{CS}}$ is HIGH, the ISL22416 is deselected and the SDO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state.

Principles of Operation

The ISL22416 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and the SPI serial interface providing direct communication between host and potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR<6:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR<6:0>: 7Fh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22416 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the SPI serial interface as described in the following sections.

Memory Description

The ISL22416 contains one non-volatile 7-bit register, known as the Initial Value Register (IVR), volatile 7-bit Wiper Register (WR), and volatile 8-bit Access Control Register (ACR). The memory map of ISL22416 is on Table 1. The non-volatile register (IVR) at address 0, contain initial wiper position and volatile registers (WR) contain current wiper position.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	—	ACR
1	Reserved	
0	IVR	WR

The non-volatile IVR and volatile WR registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described below in Table 2.

The VOL bit (ACR<7>) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

BIT #	7	6	5	4	3	2	1	0
BIT NAME	VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR<6>) disables or enables Shutdown mode. This bit is logically OR’d with $\overline{SHDN}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR<5>) is read only bit. It indicates that non-volatile write operation is in progress. The WIP bit can be read repeatedly after a non-volatile write to determine if the write has been completed. It is impossible to write to the WR or ACR while WIP bit is 1.

SPI Serial Interface

The ISL22416 supports an SPI serial protocol, mode 0. The device is accessed via the SDI input and SDO output with data clocked in on the rising edge of SCK, and clocked out on the falling edge of SCK. $\overline{CS}$ must be LOW during communication with the ISL22416. SCK and $\overline{CS}$ lines are controlled by the host or master. The ISL22416 operates only as a slave device.

All communication over the SPI interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

The first byte sent to the ISL22416 from the SPI host is the Identification Byte. A valid Identification Byte contains 0101 as the four MSBs, with the following four bits set to 0.

TABLE 3. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	0
(MSB)							(LSB)

The next byte sent to the ISL22416 contains the instruction and register pointer information. The four MSBs are the instruction and two LSBs are register address (see Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

7	6	5	4	3	2	1	0
I3	I2	I1	I0	0	0	R1	R0

There are only two valid instruction sets:

1011(binary) - is a Read operation

1100(binary) - is a Write operation

There are only two registers address possible for this DCP. If the R1, R0 bits are zero, then the read or write is to either

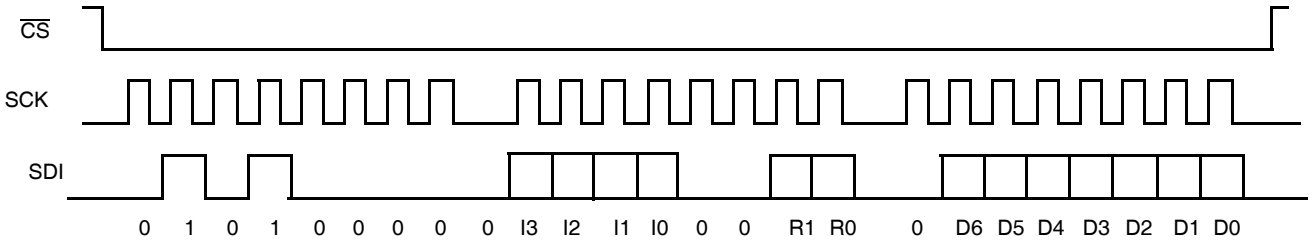


FIGURE 16. THREE BYTE WRITE SEQUENCE

the IVR or the WR register (depends of VOL bit at ACR). If the R1 bit is 1 and R0 bit is 0, then the operation is on the ACR.

Write Operation

A Write operation to the ISL22416 is a three-byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW, then a valid Identification Byte, then a valid instruction byte followed by Data Byte is sent to SDI pin. The host terminates the write operation by pulling the $\overline{CS}$ pin from LOW to HIGH. For a write to address 0 (WR), the byte at address 2 (ACR<7>) determines if the Data Byte is to be written to volatile or both volatile and non-volatile registers. Refer to “Memory Description” and Figure 16.

The internal non-volatile write cycle starts after rising edge of $\overline{CS}$ and takes up to 20ms.

Read Operation

A read operation to the ISL22416 is a three byte operation. It requires first, the $\overline{CS}$ transition from HIGH to LOW, then a valid Identification Byte, then a valid instruction byte followed by “dummy” Data Byte is sent to SDI pin. The SPI host reads the data from SDO pin on falling edge of SCK. The host terminates the read operation by pulling the $\overline{CS}$ pin from LOW to HIGH (see Figure 17).

In order to read back the non-volatile IVR, it is reccomended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Applications Information

Communicating with ISL22416

Communication with ISL22416 proceeds using SPI interface through the ACR (address 10b), IVR (address 00b) and WR (address 00b) registers.

The wiper of the potentiometer is controlled by the WR register. Writes and reads can be made directly to this register to control and monitor the wiper position without any non-volatile memory changes. This is done by setting MSB bit at address 10b to 1.

The non-volatile IVR stores the power up value of the wiper. IVR is accessible when MSB bit at address 10b is set to 0. Writing a new value to the IVR register will set a new power up position for the wiper. Also, writing to this register will load the same value into the WR as the IVR. Reading from the IVR will not change the WR, if its contents are different.

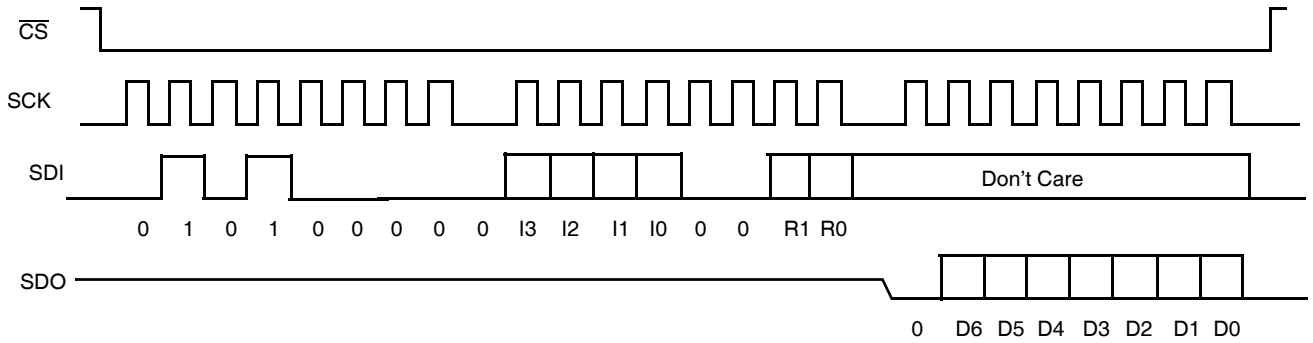


FIGURE 17. THREE BYTE READ SEQUENCE

Examples:

A. Writing to the IVR:

This sequence will write a new value (77h) to the IVR(non-volatile):

Set the ACR (Addr 02h) for NV write (40h)

Send the ID byte, Instruction Byte, then the Data byte

0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	
																(Sent to DI)								

Set the IVR (Addr 00h) to 77h

Send the ID byte, Instruction Byte, then the Data byte

0	1	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	1	1	1	0	1	1	1	
																(Sent to DI)								

B. Reading from the WR:

This sequence will read the value from the WR (volatile):

Write to ACR first to access the WR

Send the ID byte, Instruction Byte, then the Data byte

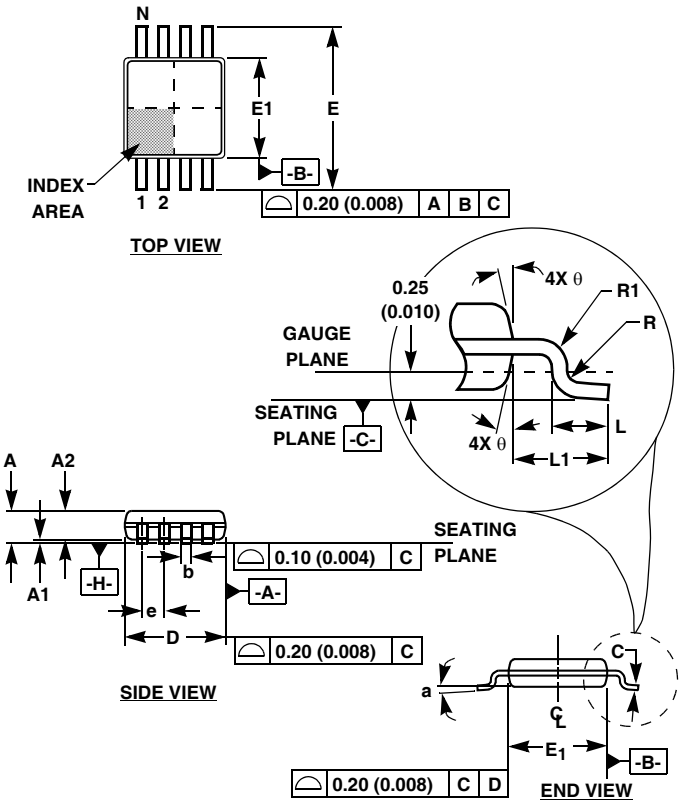
0	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0	
																(Sent to DI)								

Read the data from WR (Addr 00h)

Send the ID byte, Instruction Byte, then Read the Data byte

0	1	0	1	0	0	0	0	1	0	1	1	0	0	0	0	x	x	x	x	x	x	x	x	
																(Out on DO)								

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only