2 Port 10M/100M Switch With Build_in Memory

FEATURES

- IEEE802.3 and IEEE802.3u compliant.
- Single chip, low cost, two port switch controller.
- Build_in embedded memory on chip for packet buffering.
- Provide 2 MII/RMII (Reduced Media Independent Interface) ports.
- A flexible MII interface design can directly connect with standard MII or pseudo MII.
- Support half/full duplex operation per port.
- Optional back_pressure control for half_duplex mode.
- Provide “store and forward” switching, and forwarding rate at full_wire speed.
- Support up to 2048 MAC addresses filtering database, and automatical address aging_out function (300 secs).
- Low power CMOS design, with single 3.3V supply voltage, 50 MHZ operation.
- Provide 128 pin PQFP package (MTD502EF), and 80 pin LQFP package (MTD502EG).

GENERAL DESCRIPTION

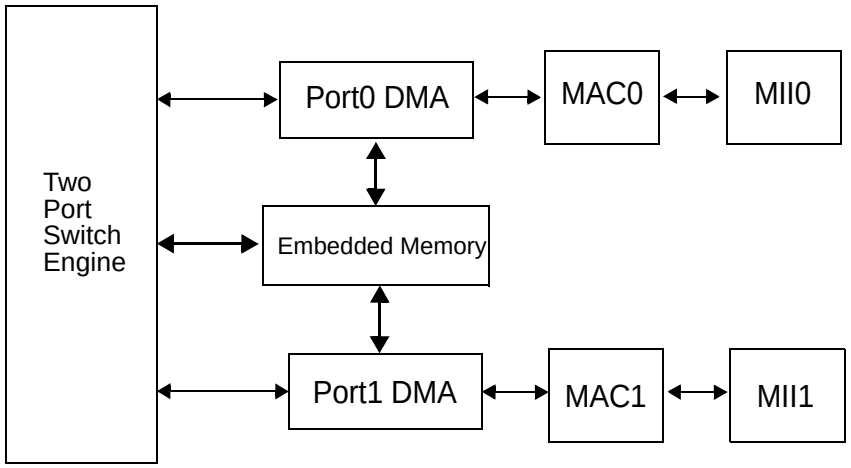
The MTD502E is a highly integrated, 10M/100M two port switch controller with build_in embedded memory. It supports 2 MII/RMII ports for 10M/100M operation, and both can operate under half or full duplex mode.

The MTD502E is an ideal solution for two port bridge or dual speed hub application, and no need any external memory buffers in application design. The flexible MII interface design can directly connect with pseudo MII interface (Am79c901, HomePNA PHY).

The MTD502E provides packet forwarding, address filtering, learning, and aging function, and have an optional back_presure control implemented in half duplex mode.

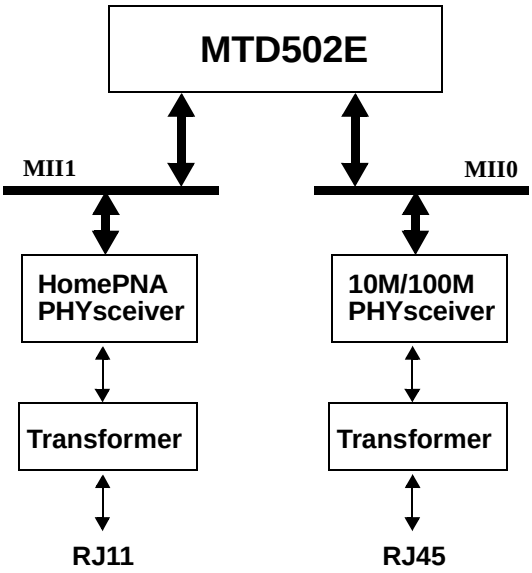
The MTD502E supports an effective address filtering database, which can recognize up to 2048 MAC addresses. It also support an automatical aging function for address table updating (aging time is 300 secs default).

BLOCK DIAGRAM

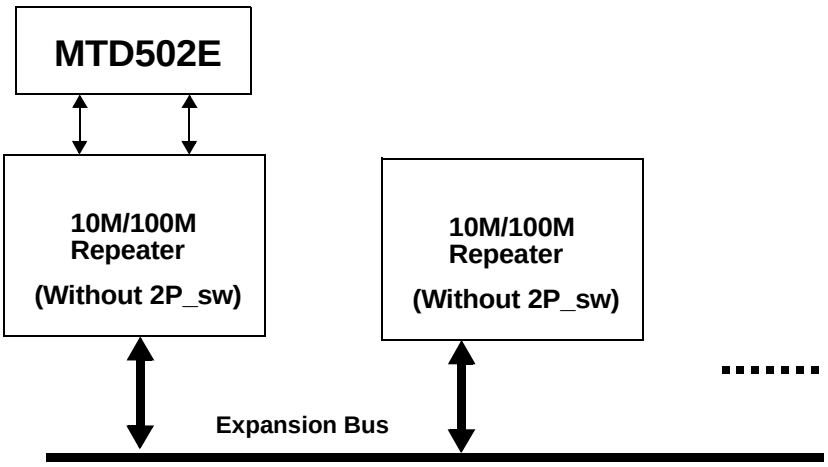


SYSTEM DIAGRAM

1). Two Port Switch Application (HomePNA to LAN)

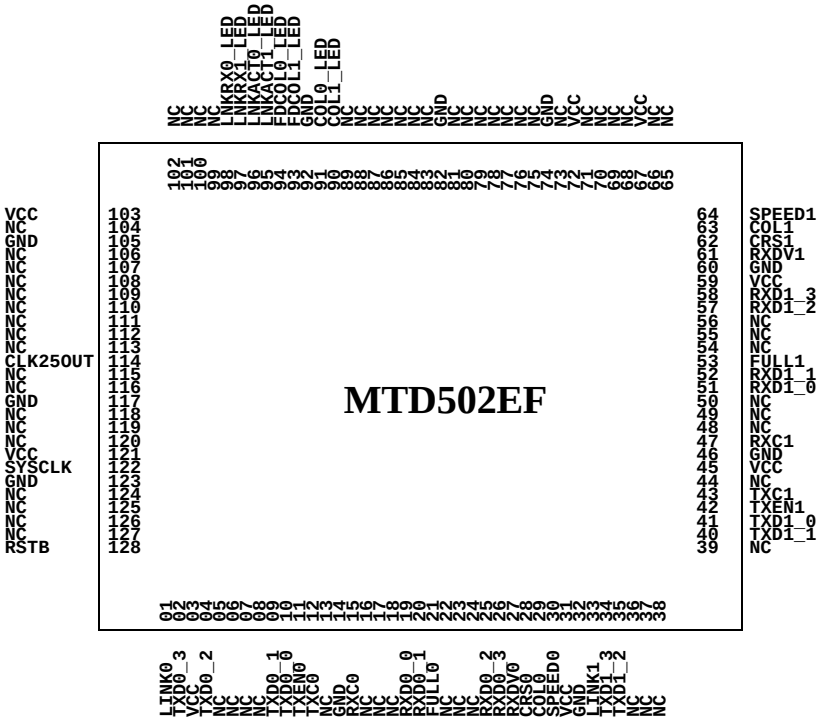


2). Dual Speed Hub Application

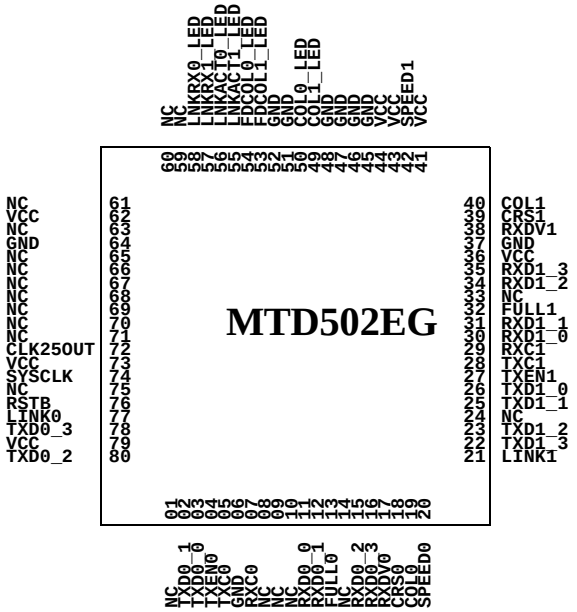


1.0 PIN CONNECTION (under MII mode)

1) 128 Pin PQFP (MTD502EF)



2) 80 Pin LQFP (MTD502EG)



2.0 PIN DESCRIPTIONS

MTD502EF (128PQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
1	I	LINK0	(NC)	LINK0	(NC)	Pin 1~32 for Port0, suitable for connecting with 10/100PHY , RISC_CPU, Switch,....
2	O	TXD0_3	RXD0_3	(NC)	(NC)	
3	VCC					
4	O	TXD0_2	RXD0_2	(NC)	(NC)	
5	O	(NC)	CRS0	(NC)	(NC)	
6~8	I	(NC)	(NC)	(NC)	(NC)	
9	O	TXD0_1	RXD0_1	(NC)	(NC)	
10	O	TXD0_0	RXD0_0	(NC)	(NC)	
11	O	TXEN0	RXDV0	(NC)	(NC)	
12	I	TXC0	(NC)	(NC)	(NC)	
13	I	(NC)	(NC)	(NC)	(NC)	
14	GND					
15	I	RXC0	(NC)	CRSDV0	TXEN0	
16	O	(NC)	RXC0	TXD0_1	RXD0_1	
17	O	(NC)	COL0	TXD0_0	RXD0_0	
18	O	(NC)	TXC0	TXEN0	CRSDV0	
19	I	RXD0_0	TXD0_0	RXD0_0	TXD0_0	
20	I	RXD0_1	TXD0_1	RXD0_1	TXD0_1	
21	I	FULL0	FULL0	FULL0	(NC)	
22~24	O	(NC)	(NC)	(NC)	(NC)	
25	I	RXD0_2	TXD0_2	(NC)	(NC)	
26	I	RXD0_3	TXD0_3	(NC)	(NC)	
27	I	RXDV0	TXEN0	(NC)	(NC)	
28	I	CRS0	SPEED0	SPEED0	(NC)	
29	I	COL0	(NC)	(NC)	(NC)	
30	I	SPEED0	(NC)	(NC)	(NC)	
31	VCC					
32	GND					
33	I	LINK1	(NC)	LINK1	(NC)	Pin 33~64 for Port1, suitable for connecting with HomePNA PHY.
34	O	TXD1_3	(NC)	(NC)	(NC)	
35	O	TXD1_2	(NC)	(NC)	(NC)	
36	O	(NC)	(NC)	(NC)	(NC)	
37,38	I	(NC)	(NC)	(NC)	(NC)	
39	I	(NC)	(NC)	CRSDV1	(NC)	
40	O	TXD1_1	(NC)	TXD1_1	(NC)	
41	O	TXD1_0	(NC)	TXD1_0	(NC)	
42	O	TXEN1	(NC)	TXEN1	(NC)	
43	I	TXC1	(NC)	RXD1_0	(NC)	
44	I	(NC)	(NC)	RXD1_1	(NC)	
45	VCC					

MTD502EF (128PQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
46	GND					
47	I	RXC1	(NC)	FULL1	(NC)	
48~50	O	(NC)	(NC)	(NC)	(NC)	
51	I	RXD1_0	(NC)	(NC)	(NC)	
52	I	RXD1_1	(NC)	(NC)	(NC)	
53	I	FULL1	(NC)	SPEED1	(NC)	
54~56	O	(NC)	(NC)	(NC)	(NC)	
57	I	RXD1_2	(NC)	(NC)	(NC)	
58	I	RXD1_3	(NC)	(NC)	(NC)	
59	VCC					
60	GND					
61	I	RXDV1	(NC)	(NC)	(NC)	
62	I	CRS1	(NC)	(NC)	(NC)	
63	I	COL1	(NC)	(NC)	(NC)	
64	I	SPEED1	(NC)	(NC)	(NC)	
65~66	I	(NC)	(NC)	(NC)	(NC)	
67	VCC					*
68~71	IO	(NC)	(NC)	(NC)	(NC)	
72	VCC					
73	IO	(NC)	(NC)	(NC)	(NC)	
74	GND					
75,76	IO	(NC)	(NC)	(NC)	(NC)	
77~79	I	(NC)	(NC)	(NC)	(NC)	
80	O	(NC)	(NC)	(NC)	(NC)	
81	IO	(NC)	(NC)	(NC)	(NC)	
82	GND					
83~85	IO	(NC)	(NC)	(NC)	(NC)	
86~88	I	(NC)	(NC)	(NC)	(NC)	
89	O	(NC)	(NC)	(NC)	(NC)	
90	IO	Co1_D	Co1_D	Co1_D	Co1_D	Port1: COL LED display, low_active. * when in half duplex mode: this LED pin present port1's collision event.
91	IO	Co0_D	Co0_D	Co0_D	Co0_D	Port0: COL LED display, low_active. * when in half duplex mode: this LED pin present port0's collision event.
92	GND					
93	IO	FdCo1_D	FdCo1_D	FdCo1_D	FdCo1_D	Port1: FULL/COL LED display, low_active. * when in full duplex mode: this LED pin is always in low_active. when in half duplex mode: this LED pin present port1's collision event, using flash style for display.

MTD502EF (128PQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
94	IO	FdCo0_D	FdCo0_D	FdCo0_D	FdCo0_D	Port0: FULL/COL LED display, low_active. * when in full duplex mode: this LED pin is always in low_active. when in half duplex mode: this LED pin present port0's collision event, using flash style for display.
95	IO	LnAc1_D	LnAc1_D	LnAc1_D	LnAc1_D	Port1: Link_Activity LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Tx or Rx activity in this port : this LED pin present port1's Tx/Rx activity, using flash style for display.
96	IO	LnAc0_D	LnAc0_D	LnAc0_D	LnAc0_D	Port0: Link_Activity LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Tx or Rx activity in this port : this LED pin present port0's Tx/Rx activity, using flash style for display.
97	IO	LnRx1_D	LnRx1_D	LnRx1_D	LnRx1_D	Port1: Link_Rx LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Rx activity in this port : this LED pin present port1's Rx activity, using flash style for display.
98	IO	LnRx0_D	LnRx0_D	LnRx0_D	LnRx0_D	Port0: Link_Rx LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Rx activity in this port : this LED pin present port0's Rx activity, using flash style for display.
99~102	IO	(NC)	(NC)	(NC)	(NC)	
103	VCC					
104	IO	(NC)	(NC)	(NC)	(NC)	
105	GND					
106~110	IO	(NC)	(NC)	(NC)	(NC)	
111	IO	(NC)	P0MDIO	(NC)	P0MDIO	
112	IO	(NC)	P0MDC	(NC)	P0MDC	
113	IO	(NC)	(NC)	(NC)	(NC)	
114	IO	CLK25O	CLK25O	CLK25O	CLK25O	clock 25Mhz output.
115~116	IO	(NC)	(NC)	(NC)	(NC)	
117	GND					
118~120	IO	(NC)	(NC)	(NC)	(NC)	
121	VCC					
122	I	SYSCLK	SYSCLK	SYSCLK	SYSCLK	system clock input, 50Mhz operation.
123	GND					

MTD502EF (128PQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	I/O	MII mode	Phy_MII mode	Rmii mode	Phy_Rmii mode	Descriptions
124~127	IO	(NC)	(NC)	(NC)	(NC)	
128	I	RSTB	RSTB	RSTB	RSTB	system resetb input, low_active.

note: input signal LINK,SPEED,FULL from PHY device are low_active definnition.

MTD502EF(128PQFP) Jumper Setting Table After Power On Reset			
Pin No.	IO	Setting Function	Descriptions
5	IO	2P_Sw Enable	Jumper setting function after power on reset. -external pull_high = 1, means enter 2 port switch mode. -external pull_low = 0, means an internal test mode. -external floating : default is 0. For MTD502E application, this pin must always use “external pull_hgih” for well operation.
18	IO	Back Pressure Disable	Jumper setting function after power on reset. -external pull_high = 1, means back_pressure function (under half_duplex) is disabled for two ports both. -external pull_low = 0, means back_pressure function enable. -external floating : default is 0.
95	IO	P1_Rmii Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 1 RMII interface enable.. -external pull_low = 0, means Port 1 is MII interface. -external floating : default is 0.
97	IO	P0_Rmii Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 RMII interface enable.. -external pull_low = 0, means Port 0 is MII interface. -external floating : default is 0.
98	IO	P0_Phy_Mode Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 interrface enter PHY mode. -external pull_low = 0, means Port 0 interface is using MAC mode. -external floating : default is 0.
100	IO	P1_Bkoff_4 Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 1 MAC backoff engine is using limit_4 modified method. -external pull_low = 0, means Port 1 MAC backoff engine is using specification defined method. -external floating : default is 0.

MTD502EF(128PQFP) Jumper Setting Table After Power On Reset			
Pin No.	**IO**	**Setting Function**	**Descriptions**
101	IO	P0_Bkoff_4 Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 MAC backoff engine is using limit_4 modified method. -external pull_low = 0, means Port 0 MAC backoff engine is using specification defined method. -external floating : default is 0.
102	IO	DeviceID[4]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
104	IO	DeviceID[3]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
106	IO	DeviceID[2]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
107	IO	DeviceID[1]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
108	IO	DeviceID[0]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
109	IO	P1_CRCchk Disable	Jumper setting function after power on reset. -external pull_high = 1, means Port1 CRC check and drop function is disabled. -external pull_low = 0, means Port1 CRC check and drop function is enabled. -external floating : default is 0.

MTD502EF(128PQFP) Jumper Setting Table After Power On Reset			
Pin No.	**IO**	**Setting Function**	**Descriptions**
110	IO	P0_CRCchk Disable	Jumper setting function after power on reset. -external pull_high = 1, means Port0 CRC check and drop function is disabled. -external pull_low = 0, means Port0 CRC check and drop function is enabled. -external floating : default is 0.
126	IO	VLAN tag Enable	Jumper setting function after power on reset. -external pull_high = 1, means MAC receiving accept 1522 Bytes packet (VLAN tag enable). -external pull_low = 0, means MAC receiving reject 1522 Bytes packet (VLAN tag disable). -external floating : default is 0.

3.0 MTD502EG (80LQFP) PIN DESCRIPTIONS

MTD502EG(80LQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
1	O	(NC)	CRS0	(NC)	(NC)	Pin 77~80, 1~20 for Port0, suitable for connecting with 10/100PHY , RISC_CPU, Switch,....
2	O	TXD0_1	RXD0_1	(NC)	(NC)	
3	O	TXD0_0	RXD0_0	(NC)	(NC)	
4	O	TXEN0	RXDV0	(NC)	(NC)	
5	I	TXC0	(NC)	(NC)	(NC)	
6	GND					
7	I	RXC0	(NC)	CRSDV0	TXEN0	
8	O	(NC)	RXC0	TXD0_1	RXD0_1	
9	O	(NC)	COL0	TXD0_0	RXD0_0	
10	O	(NC)	TXC0	TXEN0	CRSDV0	
11	I	RXD0_0	TXD0_0	RXD0_0	TXD0_0	
12	I	RXD0_1	TXD0_1	RXD0_1	TXD0_1	
13	I	FULL0	FULL0	FULL0	(NC)	
14	O	(NC)	(NC)	(NC)	(NC)	
15	I	RXD0_2	TXD0_2	(NC)	(NC)	
16	I	RXD0_3	TXD0_3	(NC)	(NC)	
17	I	RXDV0	TXEN0	(NC)	(NC)	
18	I	CRS0	SPEED0	SPEED0	(NC)	
19	I	COL0	(NC)	(NC)	(NC)	
20	I	SPEED0	(NC)	(NC)	(NC)	
21	I	LINK1	(NC)	(NC)	(NC)	Pin 21~41 for Port1, suitable for connecting with HomePNA PHY.
22	O	TXD1_3	(NC)	(NC)	(NC)	
23	O	TXD1_2	(NC)	(NC)	(NC)	
24	O	(NC)	(NC)	(NC)	(NC)	
25	O	TXD1_1	(NC)	(NC)	(NC)	
26	O	TXD1_0	(NC)	(NC)	(NC)	
27	O	TXEN1	(NC)	(NC)	(NC)	
28	I	TXC1	(NC)	(NC)	(NC)	
29	I	RXC1	(NC)	(NC)	(NC)	
30	I	RXD1_0	(NC)	(NC)	(NC)	
31	I	RXD1_1	(NC)	(NC)	(NC)	
32	I	FULL1	(NC)	(NC)	(NC)	
33	O	(NC)	(NC)	(NC)	(NC)	
34	I	RXD1_2	(NC)	(NC)	(NC)	
35	I	RXD1_3	(NC)	(NC)	(NC)	
36	VCC					
37	GND					
38	I	RXDV1	(NC)	(NC)	(NC)	
39	I	CRS1	(NC)	(NC)	(NC)	

MTD502EG(80LQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
40	I	COL1	(NC)	(NC)	(NC)	
41	VCC					*
42	I	SPEED1	(NC)	(NC)	(NC)	
43	VCC					
44	VCC					
45	GND					
46	GND					
47	GND					
48	GND					
49	IO	Co1_D	Co1_D	Co1_D	Co1_D	Port1: COL LED display, low_active. * when in half duplex mode: this LED pin present port1's collision event.
50	IO	Co0_D	Co0_D	Co0_D	Co0_D	Port0: COL LED display, low_active. * when in half duplex mode: this LED pin present port0's collision event.
51	GND					
52	GND					
53	IO	FdCo1_D	FdCo1_D	FdCo1_D	FdCo1_D	Port1: FULL/COL LED display, low_active. * when in full duplex mode: this LED pin is always in low_active. when in half duplex mode: this LED pin present port1's collision event, using flash style for display.
54	IO	FdCo0_D	FdCo0_D	FdCo0_D	FdCo0_D	Port0: FULL/COL LED display, low_active. * when in full duplex mode: this LED pin is always in low_active. when in half duplex mode: this LED pin present port0's collision event, using flash style for display.
55	IO	LnAc1_D	LnAc1_D	LnAc1_D	LnAc1_D	Port1: Link_Activity LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Tx or Rx activity in this port : this LED pin present port1's Tx/Rx activity, using flash style for display.

MTD502EG(80LQFP) Pin Definition Mapping Under Different Configurations						
Pin No.	**I/O**	**MII mode**	**Phy_MII mode**	**Rmii mode**	**Phy_Rmii mode**	**Descriptions**
56	IO	LnAc0_D	LnAc0_D	LnAc0_D	LnAc0_D	Port0: Link_Activity LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Tx or Rx activity in this port : this LED pin present port0's Tx/Rx activity, using flash style for display.
57	IO	LnRx1_D	LnRx1_D	LnRx1_D	LnRx1_D	Port1: Link_Rx LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Rx activity in this port : this LED pin present port1's Rx activity, using flash style for display.
58	IO	LnRx0_D	LnRx0_D	LnRx0_D	LnRx0_D	Port0: Link_Rx LED display, low_active. * when in Link_On state : this LED pin is always in low_active. when have Rx activity in this port : this LED pin present port0's Rx activity, using flash style for display.
59-61	IO	(NC)	(NC)	(NC)	(NC)	
62	VCC					
63	IO	(NC)	(NC)	(NC)	(NC)	
64	GND					
65-69	IO	(NC)	(NC)	(NC)	(NC)	
70	IO	(NC)	P0MDIO	(NC)	P0MDIO	
71	IO	(NC)	P0MDC	(NC)	P0MDC	
72	O	CLK25O	CLK25O	CLK25O	CLK25O	clock 25Mhz output.
73	VCC					
74	I	SYSCLK	SYSCLK	SYSCLK	SYSCLK	system clock input, 50Mhz operation.
75	IO	(NC)	(NC)	(NC)	(NC)	
76	I	RSTB	RSTB	RSTB	RSTB	system resetb input, low_active.
77	I	LINK0	(NC)	LINK0	(NC)	
78	O	TXD0_3	RXD0_3	(NC)	(NC)	
79	VCC					
80	O	TXD0_2	RXD0_2	(NC)	(NC)	

note: input signal LINK,SPEED,FULL from PHY device are low_active definnition.

MTD502EG(80LQFP) Jumper Setting Table After Power On Reset			
Pin No.	**IO**	**Setting Function**	**Descriptions**
1	IO	2P_Sw Enable	Jumper setting function after power on reset. -external pull_high = 1, means enter 2 port switch mode. -external pull_low = 0, means an internal test mode. -external floating : default is 0. For MTD502E application, this pin must always use “external pull_hgih” for well operation.
10	IO	Back Pressure Disable	Jumper setting function after power on reset. -external pull_high = 1, means back_pressure function (under half_duplex) is disabled for two ports both. -external pull_low = 0, means back_pressure function enable. -external floating : default is 0.
57	IO	P0_Rmii Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 RMII interface enable.. -external pull_low = 0, means Port 0 is MII interface. -external floating : default is 0.
58	IO	P0_Phy_Mode Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 interrface enter PHY mode. -external pull_low = 0, means Port 0 interface is using MAC mode. -external floating : default is 0.
59	IO	P1_Bkoff_4 Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 1 MAC backoff engine is using limit_4 modified method. -external pull_low = 0, means Port 1 MAC backoff engine is using specification defined method. -external floating : default is 0.
60	IO	P0_Bkoff_4 Enable	Jumper setting function after power on reset. -external pull_high = 1, means Port 0 MAC backoff engine is using limit_4 modified method. -external pull_low = 0, means Port 0 MAC backoff engine is using specification defined method. -external floating : default is 0.
61	IO	DeviceID[4]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.

MTD502EG(80LQFP) Jumper Setting Table After Power On Reset			
Pin No.	**IO**	**Setting Function**	**Descriptions**
63	IO	DeviceID[3]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
65	IO	DeviceID[2]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
66	IO	DeviceID[1]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
67	IO	DeviceID[0]	Jumper setting function after power on reset. -external pull_high = 1. -external pull_low = 0. -external floating : default is 0.
68	IO	P1_CRCchk Disable	Jumper setting function after power on reset. -external pull_high = 1, means Port1 CRC check and drop function is disabled. -external pull_low = 0, means Port1 CRC check and drop function is enabled. -external floating : default is 0.
69	IO	P0_CRCchk Disable	Jumper setting function after power on reset. -external pull_high = 1, means Port0 CRC check and drop function is disabled. -external pull_low = 0, means Port0 CRC check and drop function is enabled. -external floating : default is 0.
71	IO	VLAN tag Enable	Jumper setting function after power on reset. -external pull_high = 1, means MAC receiving accept 1522 Bytes packet (VLAN tag enable). -external pull_low = 0, means MAC receiving reject 1522 Bytes packet (VLAN tag disable). -external floating : default is 0.

4.0 FUNCTIONAL DESCRIPTIONS

The MTD502E implements a 10/100M two port switch for 10M/100M packet switching. Total 2K address entrys are provided for packets' SA learning and DA routing; and also provide automatic aging function (aging time = 300secs). When using in two port bridge application, the input packets from port0 will be stored in an embedded memory buffers of MTD502E first, while packets is good for forwarding (CRC chech ok, 64Bytes < length > 1518Bytes, and not local packets) , than forward this packet to port1.

4.1 Learning and Routing

The MTD502E supports 2K MAC entries for filtering. Dynamic address learning is performed by each good unicast packet is completely received. The routing process is performed whenever the packet's DA is captured. If the DA get a hit result in self port's address table, this packet will be treated as a " local packet", and then drop the packet forwarding to the other port. On the other hand, if this packet is not a "local packet", then will be forwarded to the other port.

4.2 Aging

The address entries are scheduled in the aging machine. If one station does not transmit any packet for a period of time, the belonging MAC address will be kicked out from the address table. The aging out time value is 300 seconds.

4.3 Buffer Queue Management

The buffer queue manager is implemented to manage the embedded memory packet buffering. The main function of the buffer queue manager is to maintain the linked list consists of buffer IDs, which is used to show the corresponding memory address for each incoming packet. In addition, the buffer queue manager monitors the rested free spaces status of the memory buffers, If the packet storage achieve the predefined threshold value, the buffer queue manager will raise the alarm signal which is used to enable the flow control mechanism for avoiding transmission ID queue overflow happening. MTD502E provide back pressure control scheme in half duplex mode.

4.4 Half Duplex Back Pressure Control

In half duplex mode, MTD502E provide a back pressure control mechanism to avoid dropping packets during network conjection situation. When the "back pressure control enable" bit is set during power on reset (pin_18 is external pull_low), it enables MTD502E supporting back pressure function in half_duplex mode; When output port buffer queue's on_using value reach the initialization setting threshold value, MTD502E will send a JAM pattern in the input port when it senses an incoming packet , thus force a collision to inform the remote node transmission back off and will effectively avoid dropping packets. If the "back pressure control disable" bit is set, and there is no free buffer queue available for the incoming packets, the incoming packets will be dropped.

4.5 MAC and DMA engine

The MTD502E's MAC performs all the functions in IEEE802.3 protocol, such as frame formatting, frame stripping, CRC checking, bad packet dropping, defering to line traffic, and collision handling. The MAC Rx_engine checks incoming packets and drops the bad packet which include CRC error, alignment error, short packet (less than 64 bytes), and long packet(more than 1518 bytes or 1522 bytes when the "VLAN tag 1522 bytes receive enable" bit is set during power on reset). Before transmission, The MAC Tx_engine will constantly monitor the line traffic using derfering precedure. Only if it has been idle for a 96 bits time (a minimum interpacket gap time, IPG time), actual transmmission can be started. For the half duplex mode, MAc engine will detect collision; if a collision is detected, the MAC Tx_engine will transmit a JAM pattern and then delay the re_transmission for a random time period determined by the back_off algorithm (MTD502E implements the truncated exponential back_off algorithm defined in IEEE 802.3 standard). For the full duplex mode, collision signal is ignored.

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Symbol	Parameter	RATING	Unit
V_{CC}	Power Supply Voltage	-0.3 to 3.6	V
V_{IN}	Input Voltage	-0.3 to Vcc+0.3	V
V_{OUT}	Output Voltage	-0.3 to Vcc+0.3	V
T_{STG}	Storage Temperature	-55 to 150	^{o}C

5.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage	0	-	Vcc	V
T_j	Commercial Junction Operating Temperature	0	25	115	^{o}C
	Industrial Junction Operating Temperature	-40	25	125	^{o}C

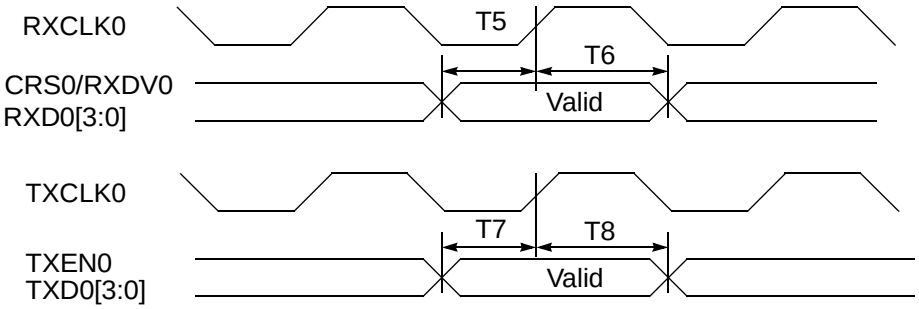
5.3 DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current	no pull-up or down	-1		1	uA
I_{OZ}	Tri-state Leakage Current		-1		1	uA
C_{IN}	Input Capacitance			2.8		pF
C_{OUT}	Output Capacitance		2.7		4.9	pF
C_{BID3}	Bi-direction buffer Capacitance		2.7		4.9	pF
V_{IL}	Input Low Voltage	CMOS			0.3*Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7*Vcc			V
V_{OH}	Output High Voltage	I_{OL}=2,4,8,12,16,24mA			0.4	V
V_{OL}	Output Low Voltage	I_{OH}=2,4,8,12,16,24mA	2.4			V
R_I	Input Pull-up/down resistance	V_{IL}=0V or V_{IH}=V_{CC}		75		KOhm

(Under recommended operating conditions and Vcc = 3.0 ~ 3.6V, Tj = 0 to +115 ^{o}C)

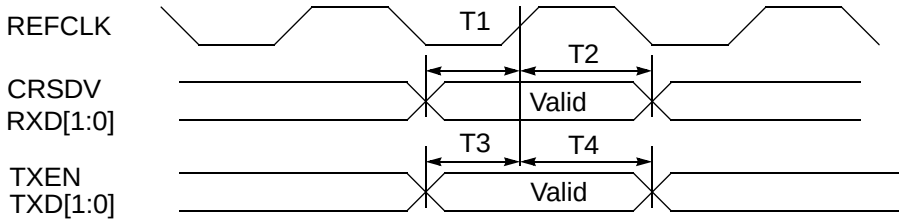
5.4 Electrical Characteristics

FIGURE 1. MII timing



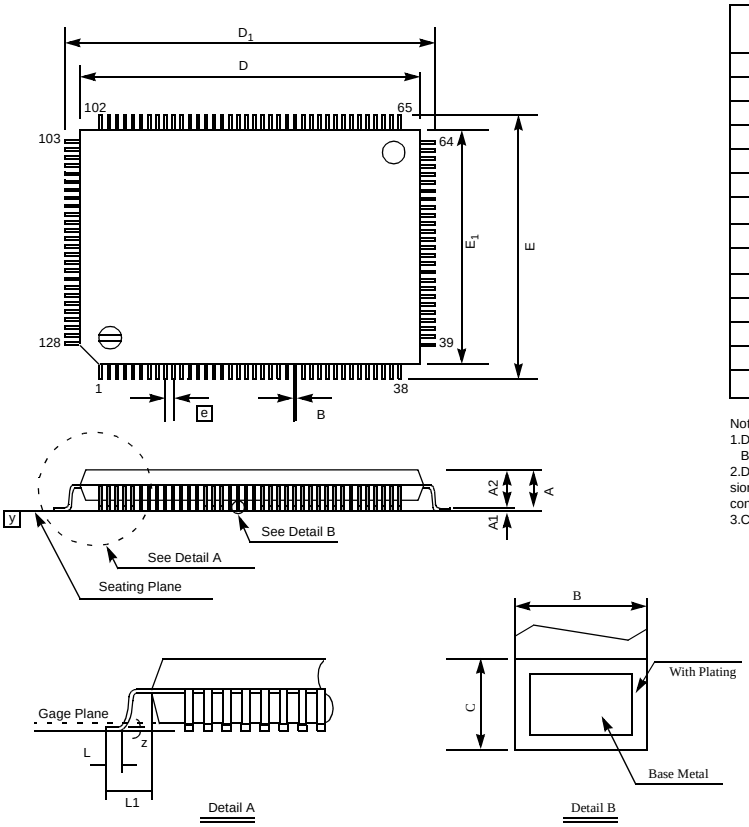
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T5	MII input setup time	10			nS	
T6	MII input hold time	10			nS	
T7	MII output setup time	3			nS	
T8	MII output hold time	5			nS	

FIGURE 2. RMII timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
T1	RMII input setup time	1			nS	
T2	RMII input hold time	1			nS	
T3	RMII output setup time	3			nS	
T4	RMII output hold time	5			nS	

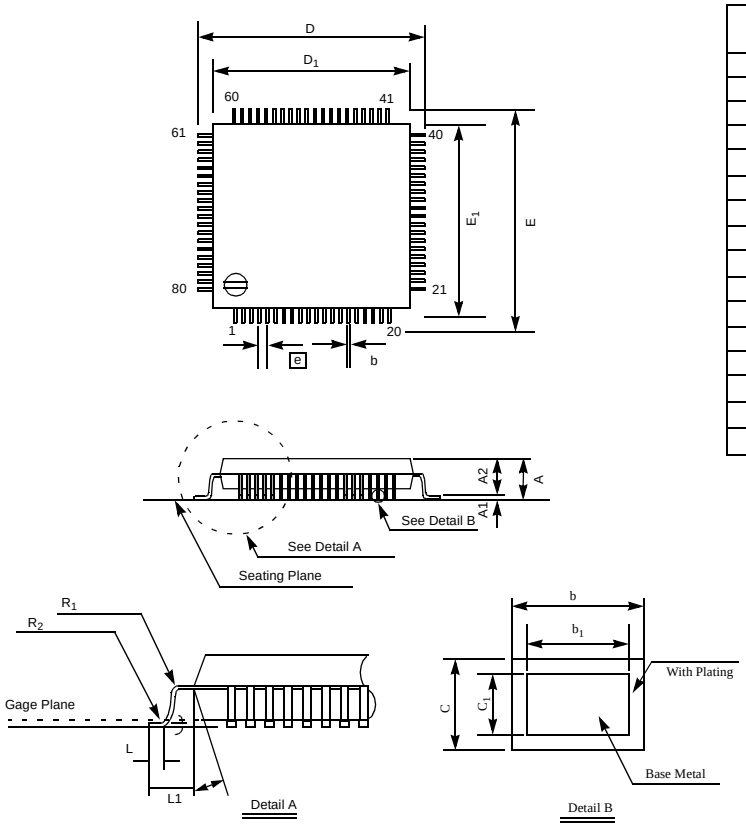
6.0 128 pin PQFP Package Data



Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
z	0^o	-	7^o	0^o	-	7^o

Note:
1.Dimension D1 & E1 do not include mold protrusion.
But mold mismatch is included. Allowable protrusion is .25mm/.010" per side.
2.Dimension B does not include dambar protrusion. Allowable dambar protrusion .08mm/.003". Total in excess of the B dimemsion at maximum material condition. Dambar cannot be located on the lower radius or the foot.
3.Controlling dimension : Millimeter.

7.0 80 pin LQFP Package Data



Symbol	Dimension in inch			Dimension in mm		
	Min	Norm	Max	Min	Norm	Max
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.4	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
b_1	0.007	0.008	0.009	0.17	0.20	0.23
C	0.004	-	0.008	0.09	-	0.20
C_1	0.004	-	0.006	0.09	-	0.16
D	0.551 BSC			14.00 BSC		
D_1	0.472 BSC			12.00 BSC		
E	0.551 BSC			14.00 BSC		
E_1	0.472 BSC			12.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
R_1	0.003	-	-	0.08	-	-
R_2	0.003	-	0.008	0.08	-	0.2