

LOW CAPACITANCE TVS ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ Cellular Phones
- ✓ Audio & Video Inputs
- ✓ FireWire, SCSI & USB Interfaces

IEC COMPATIBILITY (EN61000-4)

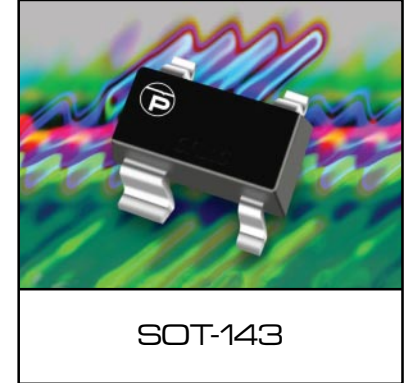
- ✓ 61000-4-2 (ESD): Air - 15kV, Contact - 8kV
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 12A, 8/20 μ s - Level 1(Line-Gnd) & Level 2(Line-Line)

FEATURES

- ✓ 500 Watts Peak Pulse Power per Line (tp=8/20 μ s)
- ✓ Unidirectional & Bidirectional Configurations
- ✓ Available in Multiple Voltage Types Ranging From 3V to 24V
- ✓ Protects One Line
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Leakage
- ✓ **LOW CAPACITANCE: 5pF PER LINE PAIR**
- ✓ RoHS Compliant in Lead-Free Versions

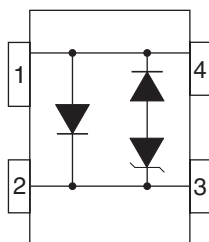
MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SOT-143 Package
- ✓ Weight 9 milligrams (Approximate)
- ✓ Available in Tin-Lead or Lead-Free Pure-Tin Plating(Annealed)
- ✓ Solder Reflow Temperature:
 - Tin-Lead - Sn/Pb, 85/15: 240-245°C
 - Pure-Tin - Sn, 100: 260-270°C
- ✓ Flammability Rating UL 94V-0
- ✓ 8mm Tape and Reel Per EIA Standard 481
- ✓ Marking: Marking Code

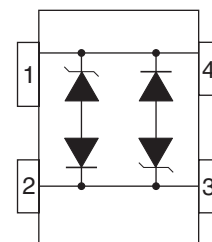


PIN CONFIGURATIONS

UNIDIRECTIONAL



BIDIRECTIONAL



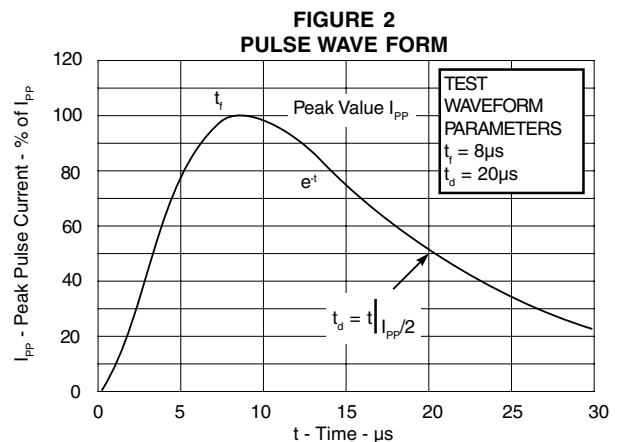
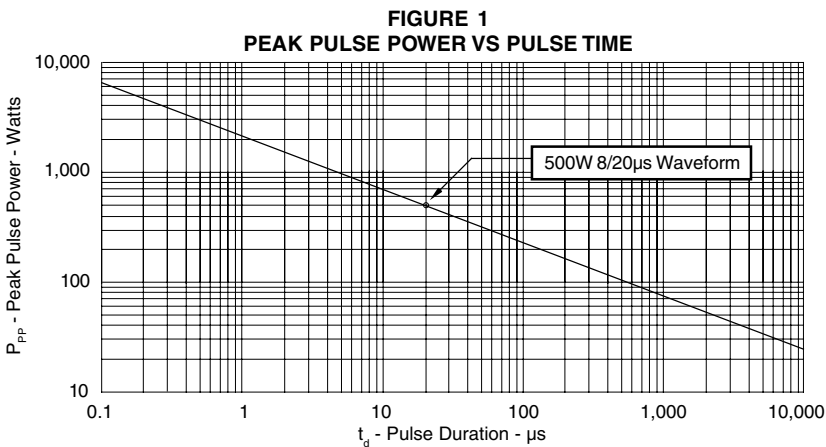
DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified			
PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power ($t_p = 8/20\mu s$) - See Figure 1	P_{PP}	500	Watts
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

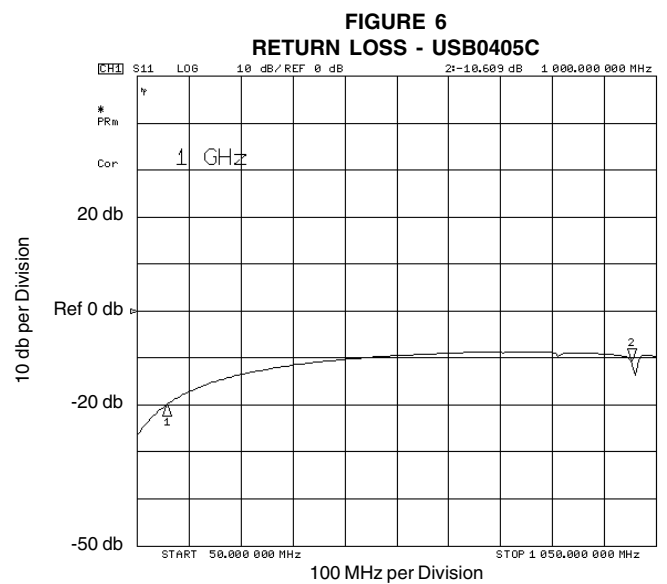
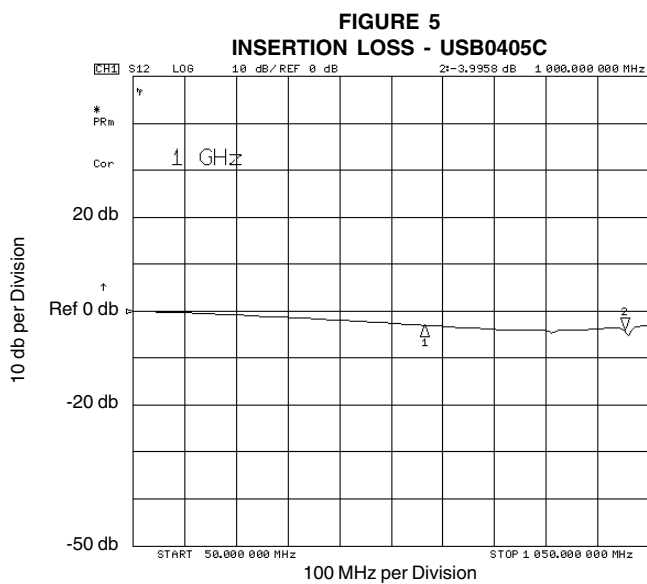
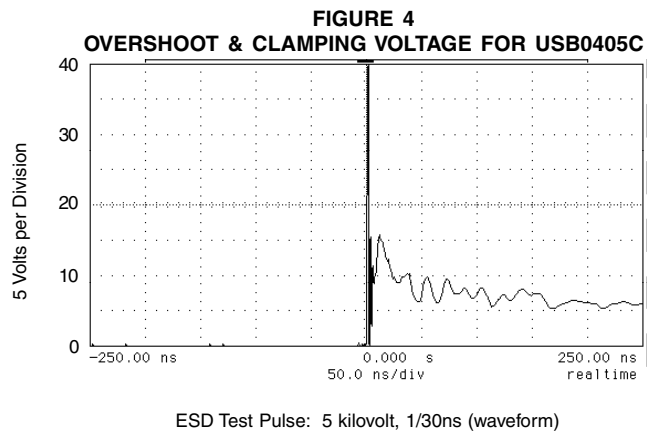
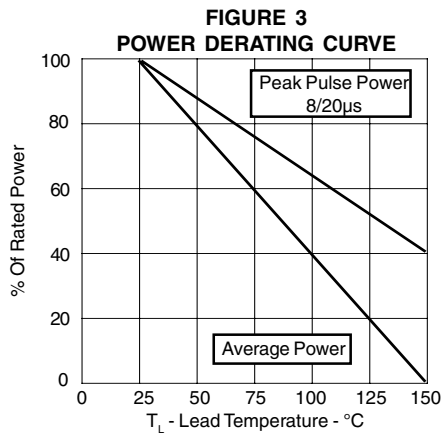
ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified							
PART NUMBER (See Notes 1-2)	DEVICE MARKING	RATED STAND-OFF VOLTAGE	MINIMUM BREAKDOWN VOLTAGE	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM CLAMPING VOLTAGE (See Fig. 2)	MAXIMUM LEAKAGE CURRENT	MAXIMUM CAPACITANCE
USB0403	3U	3.3	4.0	9.0	19.0V @ 20.0A	125	5
USB0403C	3B	3.3	4.0	9.0	19.0V @ 20.0A	125	5
USB0405	5U	5.0	6.0	11.0	18.3V @ 17.0A	20	5
USB0405C	5B	5.0	6.0	11.0	18.3V @ 17.0A	20	5
USB0408	8U	8.0	8.5	16.6	18.5V @ 17.0A	10	5
USB0408C	8B	8.0	8.5	16.6	18.5V @ 17.0A	10	5
USB0412	12U	12.0	13.3	24.0	28.6V @ 11.0A	1	5
USB0412C	12B	12.0	13.3	24.0	28.6V @ 11.0A	1	5
USB0415	15U	15.0	16.6	30.0	31.8V @ 10.0A	1	5
USB0415C	15B	15.0	16.6	30.0	31.8V @ 10.0A	1	5
USB0424	24U	24.0	26.7	N/A	56.0V @ 6.0A	1	5
USB0424C	24B	24.0	26.7	N/A	56.0V @ 6.0A	1	5

Note 1: Part numbers with an additional "C" suffix are bidirectional devices, i.e., USB0405C.

Note 2: *Unidirectional Only:* Positive potential is applied from pin 2 to 1 or pin 3 to 4.



GRAPHS



APPLICATION NOTE

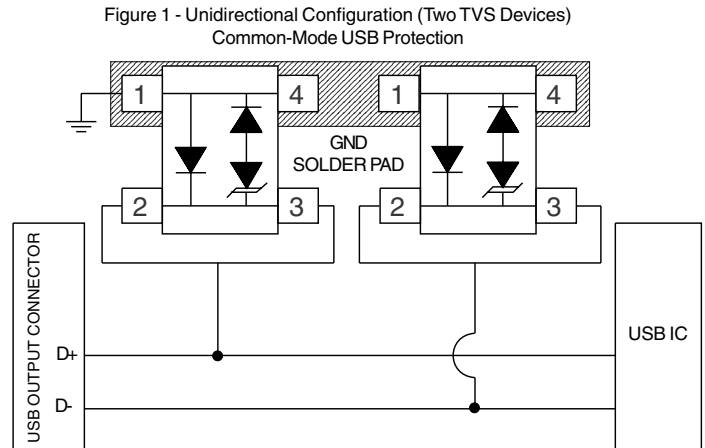
The USB04 Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD and EFT. This product series provides both unidirectional and bidirectional protection, with a surge capability of 350 Watts P_{pp} per line for an 8/20 μ s waveform and ESD protection > 40kV.

UNIDIRECTIONAL COMMON-MODE CONFIGURATION (Figure 1)

The two USB04 Series devices provide protection in a common-mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ TVS Device 1: Line 1(D+) is connected to Pins 2 & 3.
- ✓ TVS Device 2: Line 2(D-) is connected to Pins 2 & 3.
- ✓ Both TVS Devices: Pins 1 & 4 connected to ground.



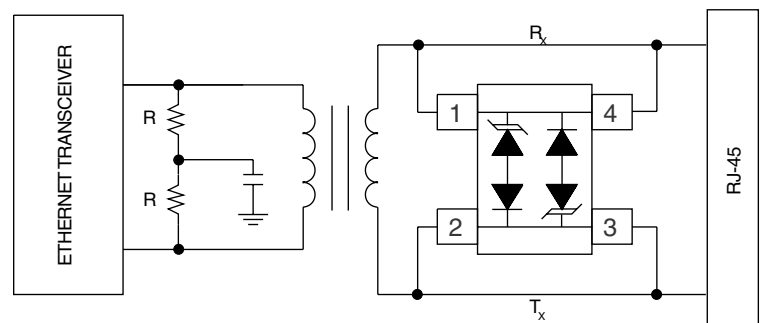
BIDIRECTIONAL DIFFERENTIAL-MODE CONFIGURATION (Figure 2)

The USB04xxC Series provides protection in a differential-mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1(R_x) is connected to Pins 1 & 4.
- ✓ Line 2(T_x) is connected to Pins 2 & 3.

Figure 2 - Bidirectional Configuration
Differential-Mode Ethernet Protection

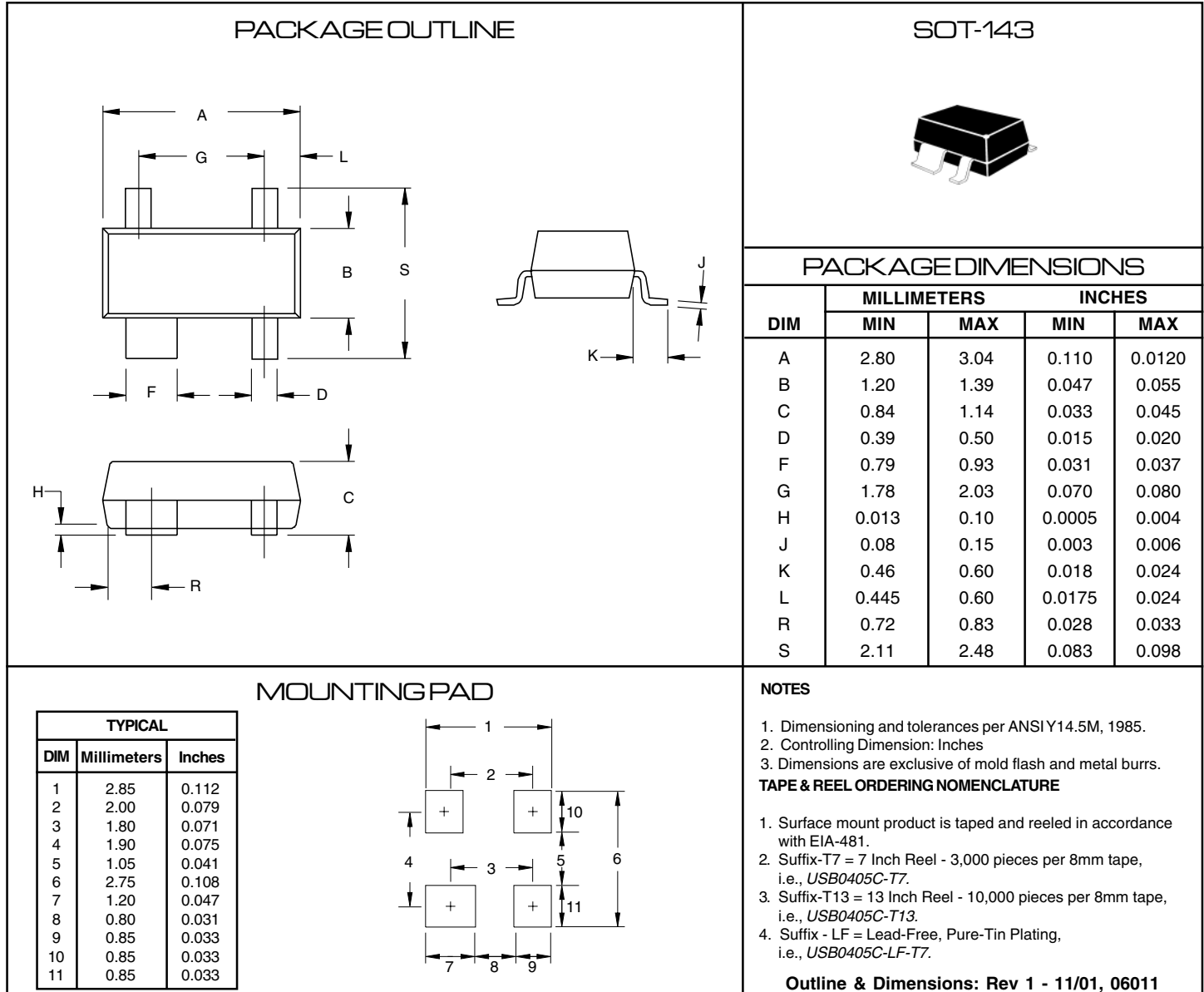


CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

PACKAGE OUTLINE & DIMENSIONS



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