FPM2750QFN

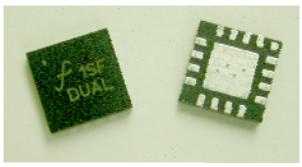
LOW NOISE HIGH LINEARITY BALANCED AMPLIFIER MODULE

Datasheet v2.5

FEATURES:

- Balanced low noise amplifier module
- Excellent Noise figure: 0.4dB at 1850MHz
- Low drive current: 40mA typical (3.0V)
- Combined IP3: 36dBm (100mA)
- Combined P1dB: 23dBm (100mA)
- Small footprint: 4mm x 4mm x 0.9mm QFN
- RoHS compliant: (Directive 2002/95/EC)

PACKAGE:



GENERAL DESCRIPTION:

The FPM2750QFN is a packaged pair of pseudomorphic High Electron Mobility Transistors (pHEMT) specifically optimised for balanced configuration systems. The Filtronic 0.25µm process ensures class-leading noise performance. The use of a small footprint plastic package allows for a cost effective total system implementation.

TYPICAL APPLICATIONS:

- Wireless infrastructure: Tower mounted Amplifiers and front end LNAs for EGSM/PCS/WCDMA/UMTS base stations
- High intercept-point LNAs

ELECTRICAL SPECIFICATIONS (as measured on each device unless otherwise stated):

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Noise Figure	NF	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA		0.4 0.6		dB
Output IP3 in balanced mode	IP3	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA	 33	32 36		dBm
SSG in balanced mode	SSG	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA	 17.5	18.5 20		dB
P1dB in balanced mode	P1dB	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA	 21.5	21 23.5		dBm
Small Signal Gain	SSG	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA		19.0 19.5		dB
Power at 1dB Gain Compression	P1dB	VDS = 3.0 V; IDS = 40mA VDS = 4.0 V; IDS = 100mA		17.5 17.5		dBm
Saturated Drain-Source Current	IDSS	VDS = 1.3 V; VGS = 0 V	185	230	280	mA
Maximum Drain-Source Current	IMAX	VDS = 1.3 V; VGS ≅ +1 V		375		mA
Transconductance	GM	VDS = 1.3 V; VGS = 0 V		200		mS
Gate-Source Leakage Current	IGSO	VGS = -5 V		5		µA
Pinch-Off Voltage	|VP|	VDS = 1.3 V; IDS = 0.75 mA	0.7	1.0	1.3	V
Gate-Source Breakdown Voltage	|VBDGS|	IGS = 0.75 mA		16		V
Gate-Drain Breakdown Voltage	|VBDGD|	IGD = 0.75 mA		16		V
Thermal Resistance	ΘJC	1W dissipation, case temperature 22°C		124		°C/W

Note: $T_{AMBIENT}$ = 22°; RF specification measured at f= 1850MHz using CW signal (except as noted).

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ABSOLUTE MAXIMUM RATING (PER TRANSISTOR)[1]:

PARAMETER	SYMBOL	TEST CONDITIONS	ABSOLUTE MAXIMUM
Drain-Source Voltage	VDS		6V
Gate-Source Voltage	VGS		-3V
Drain-Source Current	IDS	For VDS < 2V	IDSS
Gate Current	IG	Forward or reverse current	7.5mA
RF Input Power (Note 2)	PIN	Under any acceptable bias state	150mW
Channel Operating Temperature	TCH	Under any acceptable bias state	175°C
Storage Temperature	TSTG	Non-Operating Storage	-55°C to 150°C
Total Power Dissipation (Note 3)	PTOT	See De-Rating Note below	1W
Gain Compression	Comp.	Under any bias conditions	5dB

Notes:

1. $T_{Ambient}$ = 22°C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device
2. RF Input must be further limited if input VSWR > 2.5:1
3. Total Power Dissipation is defined as: $P_{TOT} = P_{DC} + P_{IN} – P_{OUT}$
   where P_{DC} = DC Bias Power, P_{IN} = RF Input Power, P_{OUT} = RF Output Power
   Total Power Dissipation shall be de-rated above 22°C as follows:
   $P_{TOT} = (150 – T_{CASE}) / \Theta_{JC}$ W
   where T_{CASE} = Temperature of the thermal pad on the underside of the package
4. Θ_{JC} increases linearly from 124°C/W at a T_{CASE} of 22°C to 145°C/W at a T_{CASE} of 145°C
5. Information on the mounting of QFN style packages for optimum thermal performance is available on request.

BIASING GUIDELINES:

- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices used in the FPM2750QFN
- Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 4 Ω for a 50% of IDSS operating point.
- For standard Class A operation, a 50% of IDSS bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Class A/B bias of 25-33% offers an optimised solution for NF and OIP3.

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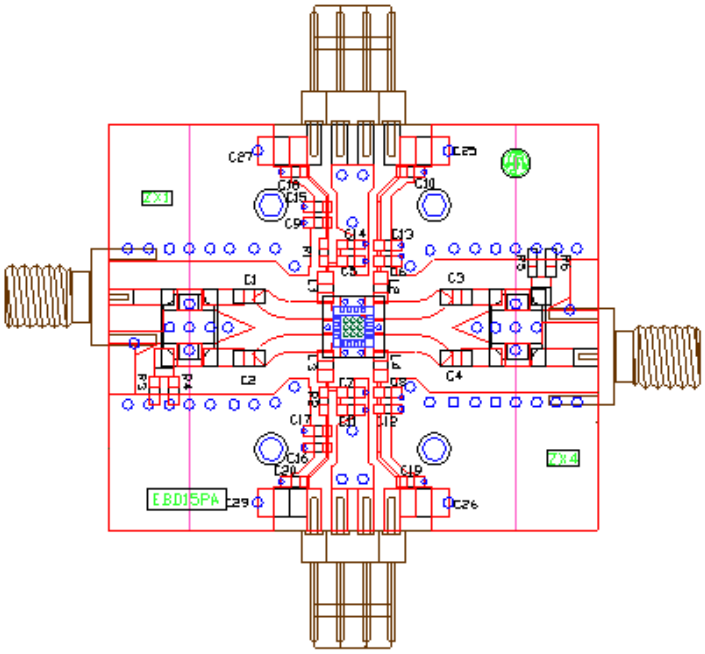
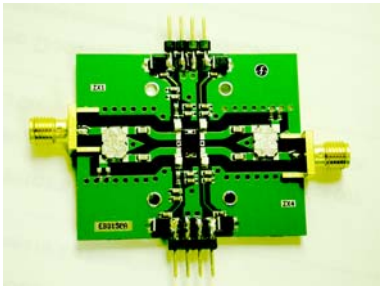
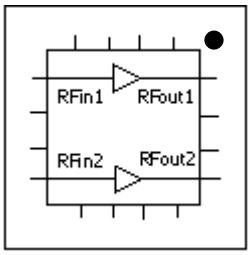
REFERENCE DESIGN 1850MHZ (BALANCED OPERATION):







Note: Package Schematic

Note: Evaluation board drawing available upon request.

BILL OF MATERIALS:

DESIGNATOR	SUPPLIER	PART NUMBER	DESCRIPTION	QUANTITY
C1, C2, C3, C4	RS Components	464-6587	CAP-20pF-0805-+/-5%-50V(MIN)-LOW_ESR	4
C5, C6, C7, C8, C9, C17	RS Components	464-6385	CAP-10pF-0603-5%-50V-COG	6
C10, C18, C19, C20	RS Components	264-4602	CAP-22nF-0603-10%-50V	4
C11, C12, C13, C14, C15, C16	RS Components	464-6543	CAP-47nF-0603-+80/-20%-50V-Y5V	6
C25, C26, C27, C29	RS Components	406-0006	CAP-1uF-CASEB-20%-35V-TANT	4
L1, L2, L3, L4	RS Components	484-1372	IND-12nH-2012(0805)-5%-600mA-HQ	4
Q2	FILTRONIC	FPM2750QFN	Dual FPD750-QFN4x4	1
R1, R2	RS Components	213-2042	RESIST-22ohm-1608(0603)-1%-0.1W	2
R3, R4, R5, R6	RS Components	213-2143	RESIST-100ohm-1608(0603)-1%-0.1W	4
W1, W2	ANAREN	1P503	HYBRID COUPLER	2
RF1, RF2	RS Components	363-4707	SMA Side Mount RF Connector	2
(V1, V2)	RS Components	453-173	DC Connector (4 way)	2
Evaluation board	FILTRONIC	EBD15PA	31mil thick FR4 1/2 Ounce Cu on both sides	1

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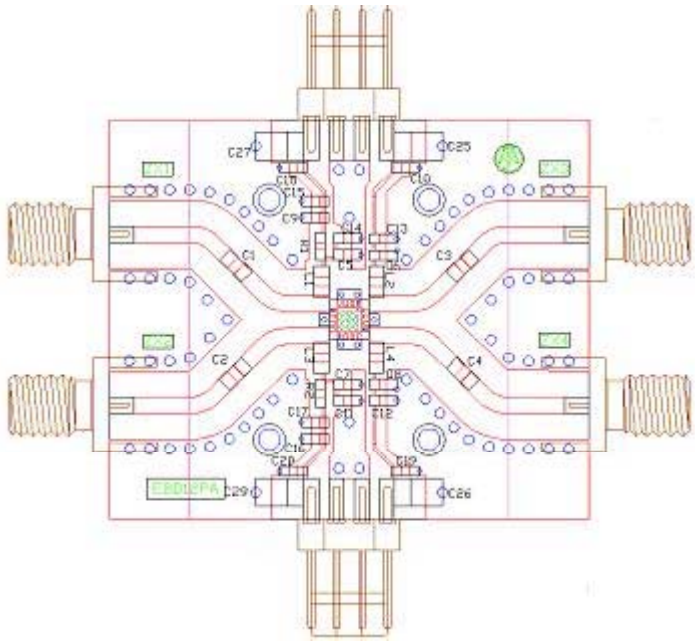
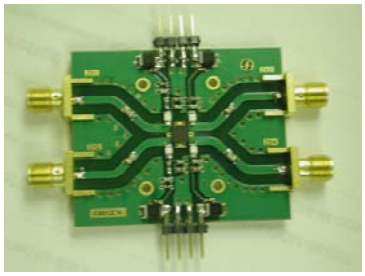
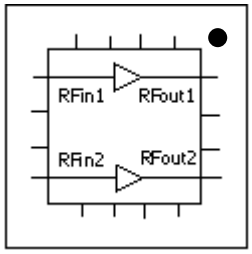
REFERENCE DESIGN 1850MHZ (SINGLE ENDED OPERATION):







Note: Package Schematic

Note: Evaluation board drawing available upon request.

BILL OF MATERIALS:

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C10, C18, C19, C20	RS Components	264-4602	CAP-22nF-0603-10%-50V	4
C11, C12, C13, C14, C15, C16	RS Components	464-6543	CAP-47nF-0603-+80/-20%-50V-Y5V	6
C25, C26, C27, C29	RS Components	406-0006	CAP-1uF-CASEB-20%-35V-TANT	4
L1, L2, L3, L4	RS Components	484-1372	IND-12nH-2012(0805)-5%-600mA-HQ	4
Q2	FILTRONIC	FPM2750QFN	Dual FPD750-QFN4x4	1
R1, R2	RS Components	213-2042	RESIST-22ohm-1608(0603)-1%-0.1W	2
RF1, RF2, RF3, RF4	RS Components	363-4707	SMA Side Mount RF Connector	4
(V1, V2)	RS Components	453-173	DC Connector (4 way)	2
Evaluation board	FILTRONIC	EBD12PA	31mil thick FR4 1/2 Ounce Cu on both sides	1

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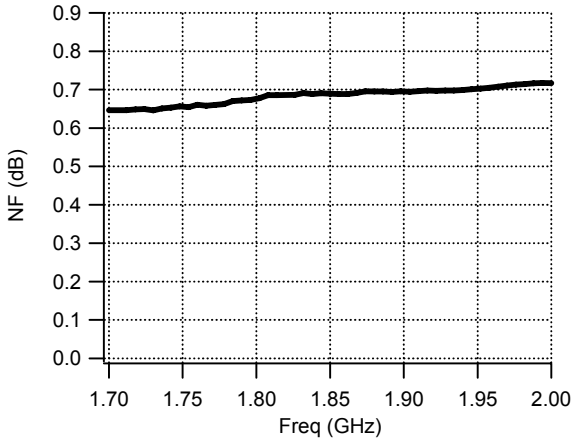
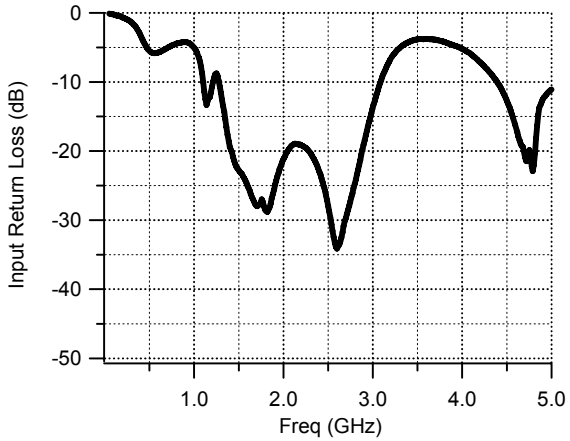
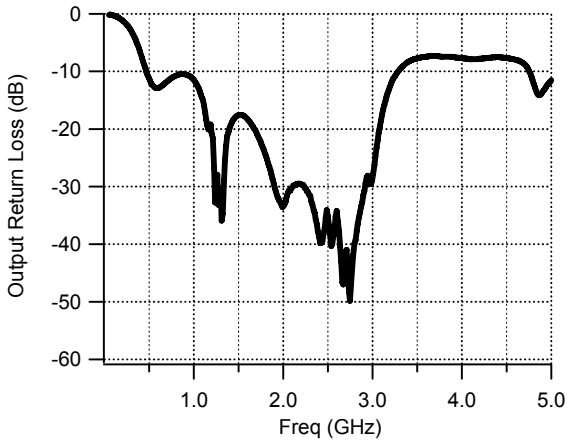
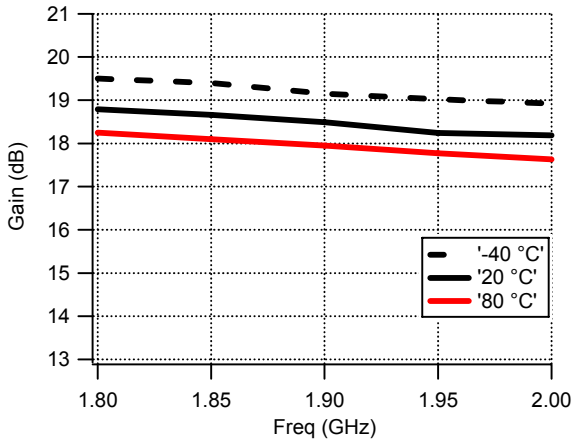
TYPICAL MEASURED PERFORMANCE ON EVALUATION BOARD: BALANCED OPERATION

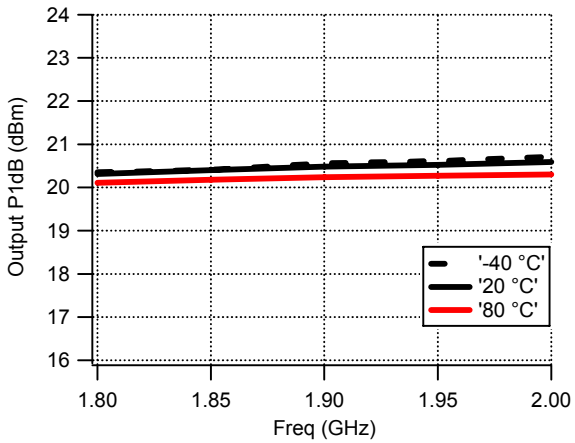
Conditions: Vds = 3V, Ids = 40mA (per device), 50Ω environment and T_A = +22 °C unless stated otherwise. All measurements shown are referenced to evaluation board connectors.

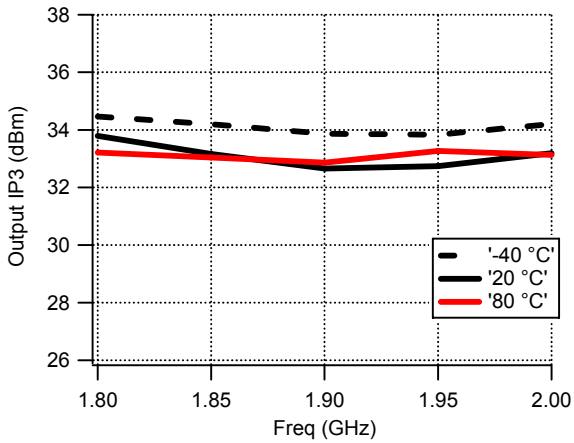












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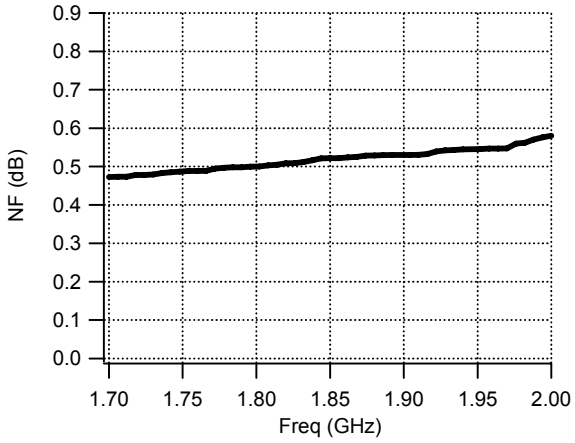
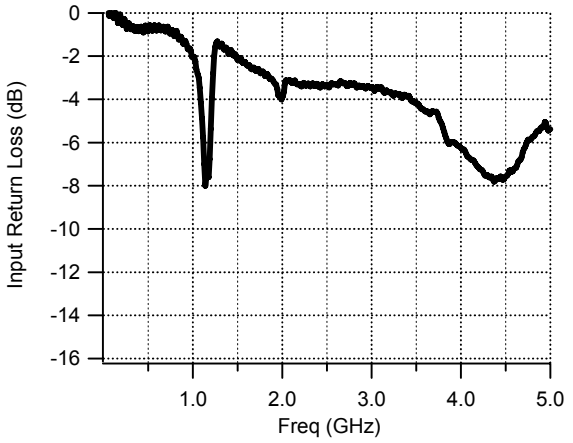
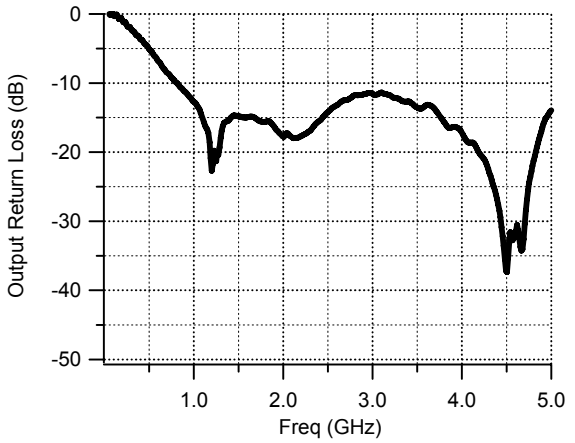
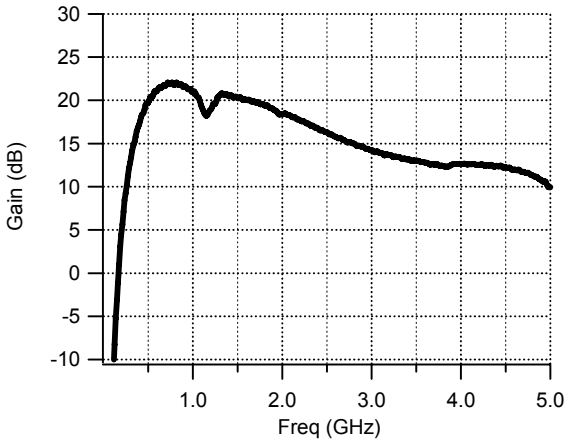
TYPICAL MEASURED PERFORMANCE ON EVALUATION BOARD: SINGLE ENDED OPERATION

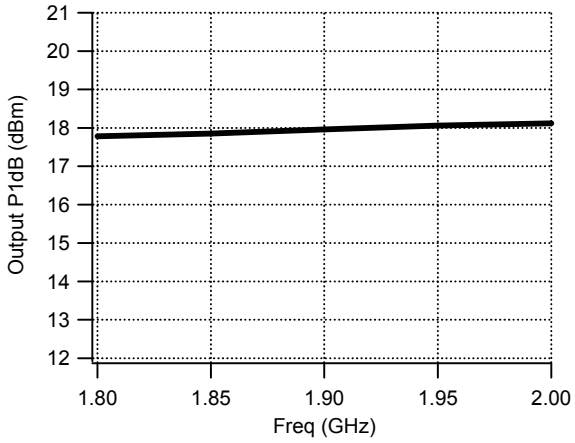
Conditions: Vds = 3V, Ids = 40mA (per device), 50Ω environment and T_A = +22 °C unless stated otherwise. All measurements shown are referenced to evaluation board connectors.

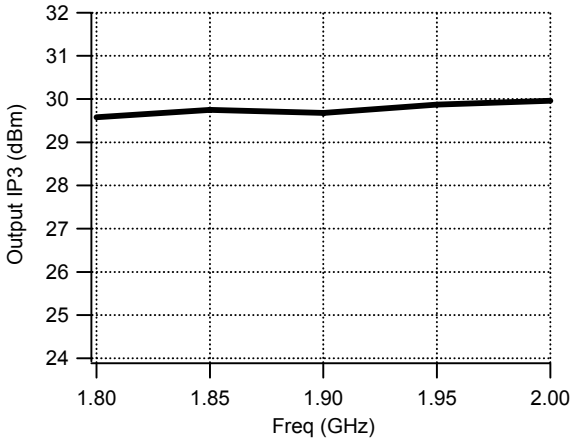












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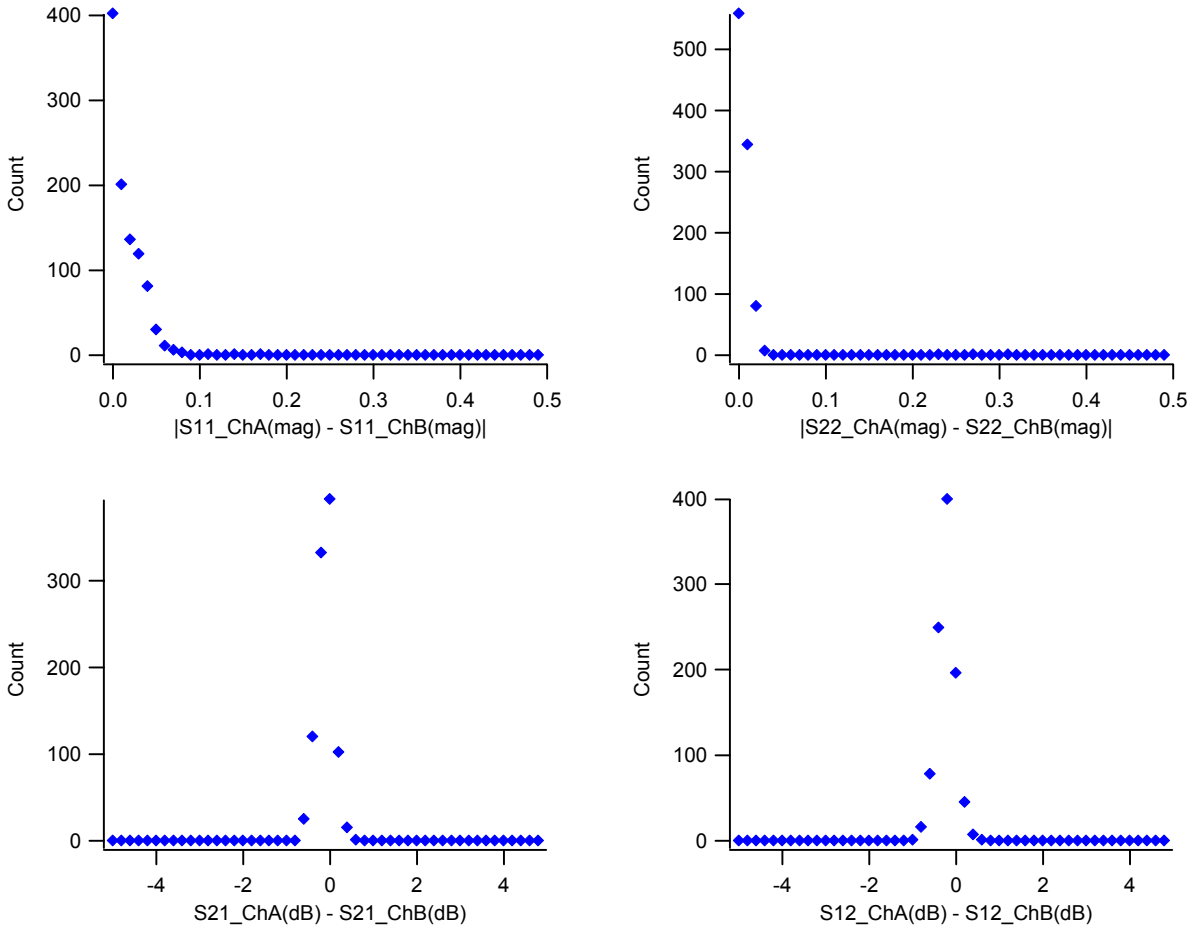
TYPICAL SMALL SIGNAL MAGNITUDE DIFFERENCE WITHIN A SINGLE PACKAGE:



The histograms above represent the distribution of the asymmetry of RF parameters for the devices within a package. ChA and ChB are the two devices within the same package. The sample size for the histograms above is 1000 parts.

PARAMETER	MEDIAN	STANDARD DEVIATION	TEST LIMIT	CPK
|S11ChA(mag) - S11ChB(mag)|	0.0001	0.027	0.1	1.3
|S22ChA(mag) – S22ChB(mag)|	0.0001	0.019	0.1	1.7
S21ChA(dB) – S21ChB(dB)	0.006	0.408	±0.75	0.68
S12ChA(dB) – S12ChB(dB)	-0.128	0.205	±0.75	1.43

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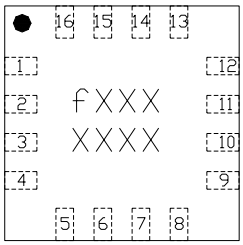
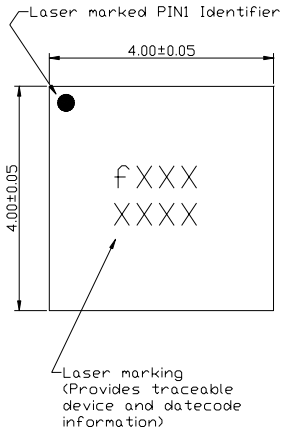
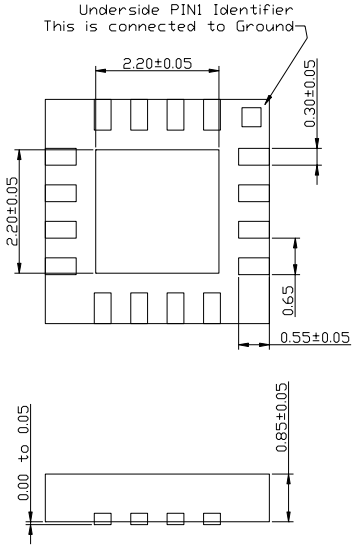
PACKAGE OUTLINE:

(dimensions in millimeters – mm, centre paddle and pin 1 identifier are grounded)

TERMINAL	FUNCTION
1-4, 6, 15	Source 1
5	RFin 1
7, 9-12, 14	Source 2
8	RFin 2
13	RFout 2
16	RFout 1







PREFERRED ASSEMBLY INSTRUCTIONS:

Please contact Filtronic Compound Semiconductors Ltd for further details.

HANDLING PRECAUTIONS:

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters are available; please contact Filtronic Compound Semiconductors Ltd.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FPM2750QFN	Packaged pHEMT
EB-FPM2750QFN-BAL	Balanced Packaged pHEMT evaluation board
EB-FPM2750QFN-SE	Single-ended Packaged pHEMT evaluation board

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