

Rail-to-rail input/output 8MHz operational amplifiers

Features

- Rail-to-rail input and output
- Wide bandwidth
- Low power consumption: 1.1mA max.
- Unity gain stability
- High output current: 35mA
- Operating from 2.5V to 5.5V
- Low input bias current
- ESD Internal protection $\geq 5kV$
- Latch-up immunity

Description

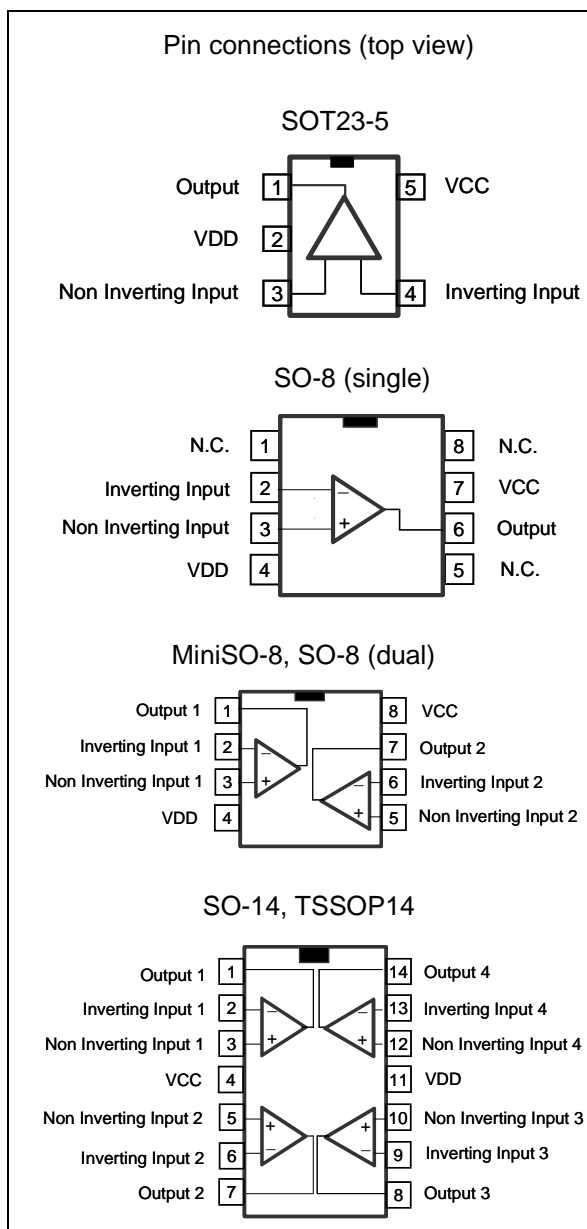
The TSV911/2/4 family of single, dual & quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering an 8MHz gain-bandwidth product while consuming only 1.1mA max at 5V supply voltage. These op-amps are unity gain stable for capacitive loads up to 200pF. They also feature an ultra-low input bias current.

These characteristics make the TSV911/2/4 family ideal for sensor interfaces, battery-supplied and portable applications, as well as active filtering.

Applications

- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation



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1 Device summary table

Part number	Temperature range	Package	Packing	Marking
TSV911ID TSV911IDT	-40 - 125°C	SO-8	Tube or tape & reel	V911I
TSV911AID TSV911AIDT				V911AI
TSV911ILT		SOT23-5	Tape & reel	K127
TSV911AILT				
TSV912IST		MiniSO-8		K125
TSV912AIST				
TSV912ID TSV912IDT		SO-8	Tube or tape & reel	V912I
TSV912AID TSV912AIDT				V912AI
TSV914IPT		TSSOP14	Tape & reel	V914I
TSV914AIPT				V914AI
TSV914ID TSV914IDT		SO-14	Tube or tape & reel	V914I
TSV914AID TSV914AIDT				V914AI
TSV911IYD TSV911IYDT		SO-8		V911IY
TSV911AIYD TSV911AIYDT				V911AY
TSV912IYD TSV912IYDT				V912IY
TSV912AIYD TSV912AIYDT				V912AY
TSV914IYD TSV914IYDT				V914IY
TSV914AIYD TSV914AIYDT				V914AY
		SO-14		

2 Absolute maximum ratings & operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	6	V
V_{id}	Differential input voltage ⁽²⁾	$\pm V_{CC}$	V
V_{in}	Input voltage ⁽³⁾	$V_{DD}-0.2$ to $V_{CC}+0.2$	V
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction to ambient ^{(4) (5)}	-	°C/W
	SOT23-5	250	
	SO-8	125	
	MiniSO-8	190	
	SO-14	103	
	TSSOP14	100	
R_{thjc}	Thermal resistance junction to case	-	°C/W
	SOT23-5	81	
	SO-8	40	
	MiniSO8	39	
	SO14	31	
	TSSOP14	32	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model ⁽⁶⁾	5	kV
	MM: machine model ⁽⁷⁾	300	V
	CDM: charged device model ⁽⁸⁾	1.5	kV
	Latch-up immunity	200	mA

1. All voltage values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. V_{CC} - V_{in} must not exceed 6V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: 100pF discharged through a 1.5kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
7. Machine model: a 200pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5Ω), done for all couples of pin combinations with other pins floating.
8. Charge device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{icm}	Common mode input voltage range	$V_{DD}-0.1$ to $V_{CC}+0.1$	V
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

Table 3. Electrical characteristics at $V_{CC} = +2.5V$

$V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x		-	0.1	4.5	mV
		$T_{min.} < T_{op} < T_{max.}$	-	-	7.5	
	TSV91xA		-	-	1.5	
		$T_{min.} < T_{op} < T_{max.}$	-	-	3	
DV_{io}/DT	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current ($V_{out} = V_{CC}/2$)		-	1	$10^{(1)}$	pA
I_{ib}	Input bias current ($V_{out} = V_{CC}/2$)		-	1	$10^{(1)}$	pA
CMR	Common Mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 2.5V, $V_{out} = 1.25V$	58	75	-	dB
A_{vd}	Large signal voltage gain	$R_L = 10k\Omega$, $V_{out} = 0.5V$ to $2V$	80	89	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$		15 45	40 150	mV
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15 45	40 150	mV
I_{out}	Isink	$V_o = 2.5V$	18	32	-	mA
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	
	Isource	$V_o = 0V$	18	35	-	
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	
I_{CC}	Supply current (per operator)	No load, $V_{out} = V_{CC}/2$	-	0.78	1.1	mA
		$T_{min.} < T_{op} < T_{max.}$	-	-	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L = 100pF$,		7.2		MHz
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L = 100pF$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L = 100pF$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $A_v = 1$	-	4.5	-	$V/\mu s$

Table 3. Electrical characteristics at $V_{CC} = +2.5V$

$V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	$f=10kHz$	-	27	-	$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G=1$, $f=1kHz$, $R_I=2k\Omega$, $BW=22kHz$, $V_{icm}=(V_{CC}+1)/2$, $V_{out}=1.1V_{pp}$	-	0.001	-	%

1. Guaranteed by design.

Table 4. Electrical characteristics at $V_{CC} = +3.3V$

$V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x	$T_{min.} < T_{op} < T_{max.}$	-	0.1	4.5	mV
		$T_{min.} < T_{op} < T_{max.}$	-	-	7.5	
	TSV91xA	$T_{min.} < T_{op} < T_{max.}$	-	-	1.5	
		$T_{min.} < T_{op} < T_{max.}$	-	-	3	
DV_{io}	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current		-	1	$10^{(1)}$	pA
I_{ib}	Input bias current		-	1	$10^{(1)}$	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	$0V$ to $3.3V$, $V_{out} = 1.65V$	60	78	-	dB
A_{vd}	Large signal voltage gain	$R_L=10k\Omega$, $V_{out}= 0.5V$ to $2.8V$	80	90	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$		15 45	40 150	mV
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15 45	40 150	mV
I_{out}	Isink	$V_o = 3.3V$	18	32	-	mA
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	
	Isource	$V_o = 0V$	18	35	-	
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	
I_{CC}	Supply current (per operator)	No load, $V_{out}=V_{CC}/2$	-	0.8	1.1	mA
		$T_{min.} < T_{op} < T_{max.}$	-	-	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L=100pF$	-	7.2	-	MHz

Table 4. Electrical characteristics at $V_{CC} = +3.3V$ $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$, $A_v=1$	-	4.5	-	V/ μs
e_n	Equivalent input noise voltage	$f=10kHz$	-	27	-	$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G=1$, $f=1kHz$, $R_I=2k\Omega$, $BW=22kHz$, $V_{icm}=(V_{CC}+1)/2$, $V_{out}=1.9V_{pp}$	-	0.00 07	-	%

1. Guaranteed by design.

Table 5. Electrical characteristics at $V_{CC} = +5V$ $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Offset voltage TSV91x		-	0.1	4.5	mV
		$T_{min.} < T_{op} < T_{max.}$	-	-	7.5	
	TSV91xA		-	-	1.5	
		$T_{min.} < T_{op} < T_{max.}$	-	-	3	
DV_{io}	Input offset voltage drift		-	2	-	$\mu V/^{\circ}C$
I_{io}	Input offset current		-	1	$10^{(1)}$	pA
I_{ib}	Input bias current		-	1	$10^{(1)}$	pA
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0V to 5V, $V_{out} = 2.5V$	62	82	-	dB
SVR	Supply voltage rejection ratio $20 \log (\Delta V_{CC}/\Delta V_{io})$	$V_{CC} = 2.5$ to 5V	70	86	-	dB
A_{vd}	Large signal voltage gain	$R_L=10k\Omega$, $V_{out}= 0.5V$ to 4.5V	80	91	-	dB
$V_{CC}-V_{OH}$	High level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$		15 45	40 150	mV
V_{OL}	Low level output voltage	$R_L = 10k\Omega$ $R_L = 600\Omega$	-	15 45	40 150	mV
I_{out}	Isink	$V_o = 5V$	18	32	-	mA
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	
	Isource	$V_o = 0V$	18	35	-	
		$T_{min.} < T_{amb} < T_{max.}$	16	-	-	

Table 5. Electrical characteristics at $V_{CC} = +5V$ $V_{DD} = 0V$, $V_{icm} = V_{CC}/2$, $T_{amb} = 25^{\circ}C$, R_L connected to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (per operator)	No load, $V_{out}=2.5V$	-	0.82	1.1	mA
		$T_{min.} < T_{op} < T_{max.}$	-	-	1.1	
AC performance						
GBP	Gain bandwidth product	$R_L = 2k\Omega$, $C_L = 100pF$, $f = 100kHz$	-	8	-	MHz
F_u	Unity gain frequency	$R_L = 2k\Omega$, $C_L=100pF$	-	7.5	-	MHz
ϕ_m	Phase margin	$R_L = 2k\Omega$, $C_L=100pF$	-	45	-	Degrees
G_m	Gain margin	$R_L = 2k\Omega$, $C_L=100pF$	-	8	-	dB
SR	Slew rate	$R_L = 2k\Omega$, $C_L = 100pF$, $A_V = 1$	-	4.5	-	V/ μs
e_n	Equivalent input noise voltage	$f=10kHz$	-	27	-	$\frac{nV}{\sqrt{Hz}}$
THD+ e_n	Total harmonic distortion	$G=1$, $f=1kHz$, $R_I=2k\Omega$, $BW=22kHz$, $V_{icm}=(V_{cc}+1)/2$, $V_{out}=3.6V_{pp}$	-	0.0004	-	%

1. Guaranteed by design.

Figure 1. Input offset voltage distribution at T=25°C

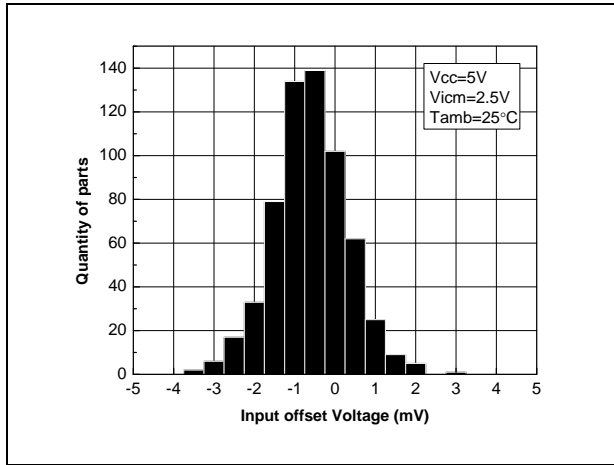


Figure 2. Input offset voltage distribution at T=125°C

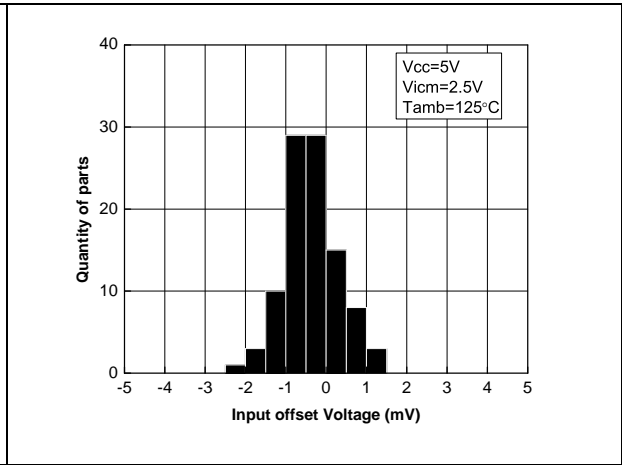


Figure 3. Supply current vs. input common mode voltage at Vcc=2.5V

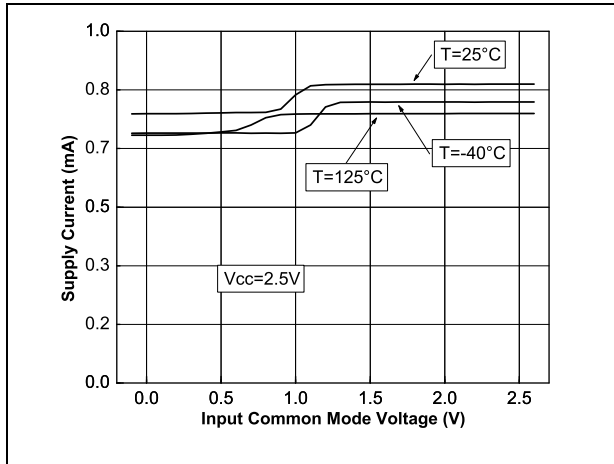


Figure 4. Supply current vs. input common mode voltage at Vcc=5V

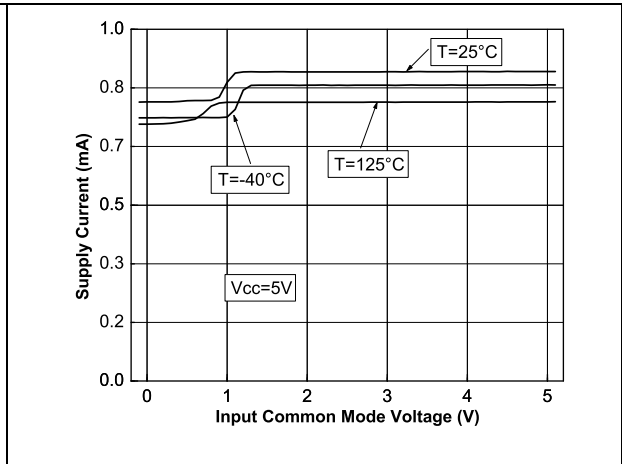


Figure 5. Output current vs. output voltage at Vcc=2.5V

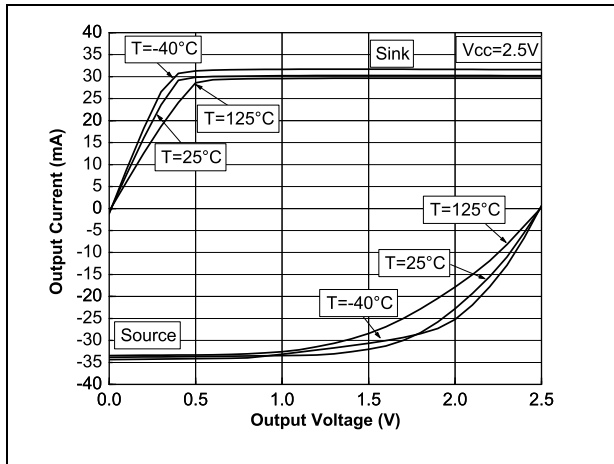


Figure 6. Output current vs. output voltage at Vcc=5V

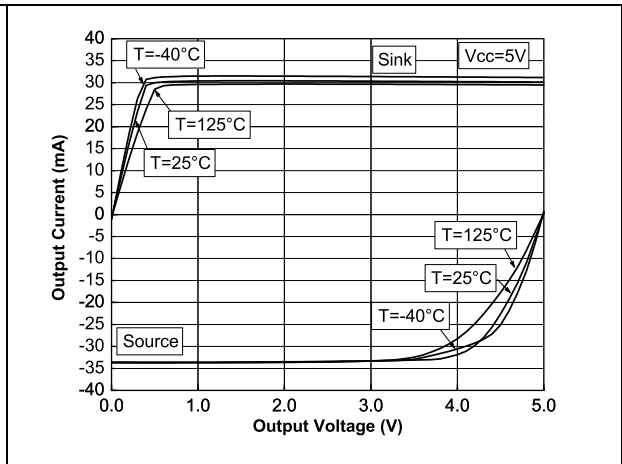


Figure 7. Voltage gain and phase vs frequency at Vcc=2.5V and Vicm=0.5V

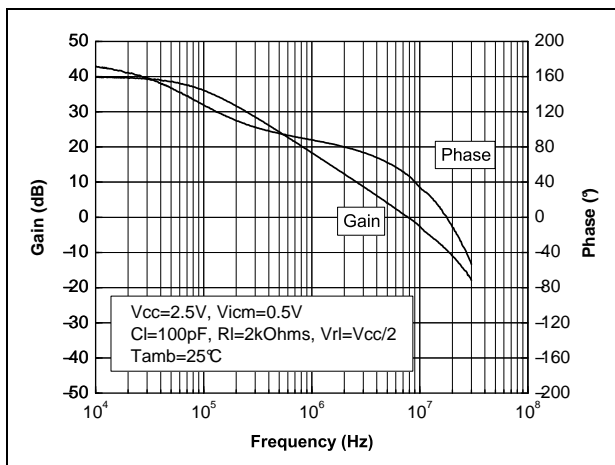


Figure 8. Voltage gain and phase vs frequency at Vcc=5.5V and Vicm=0.5V

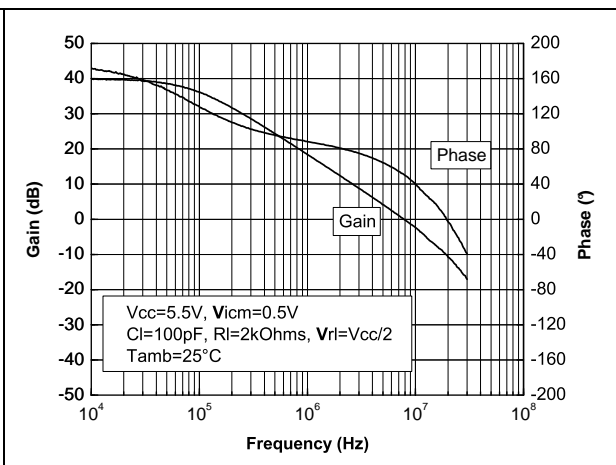


Figure 9. Phase margin vs. capacitive load

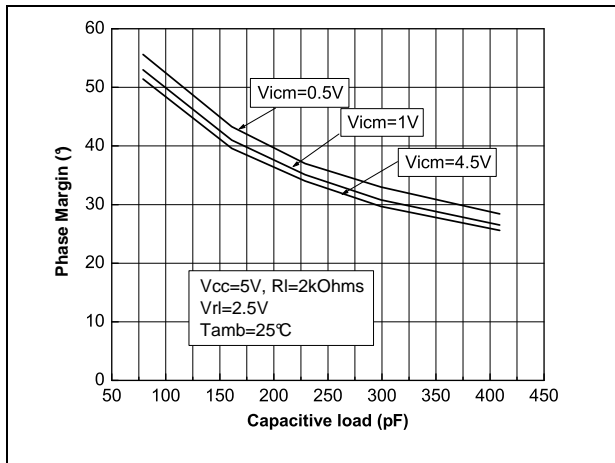


Figure 10. Phase margin vs. output current

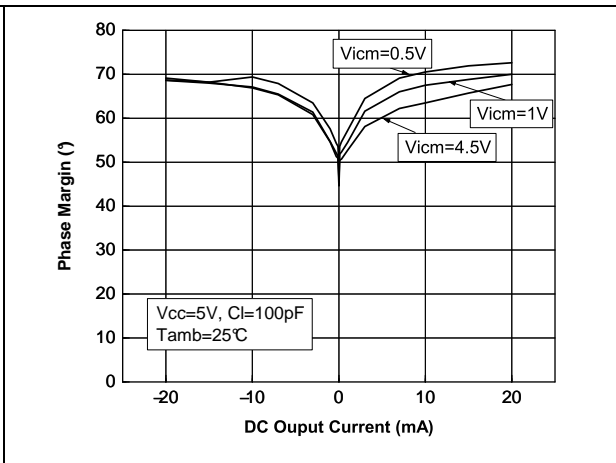


Figure 11. Positive slew rate

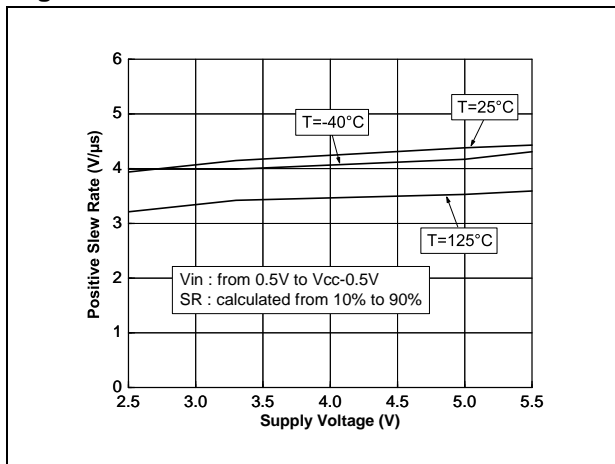


Figure 12. Negative slew rate

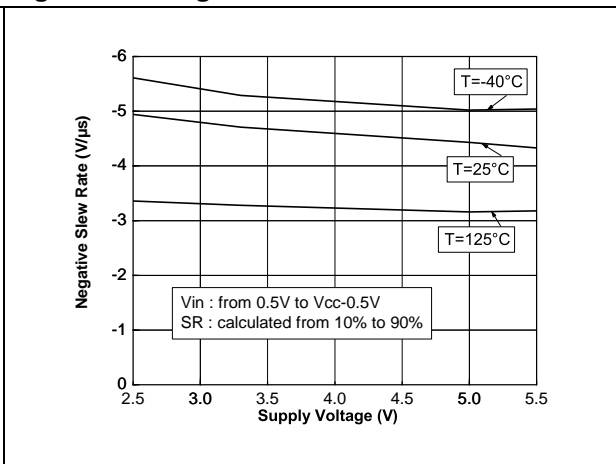


Figure 13. Distorsion + noise vs. frequency

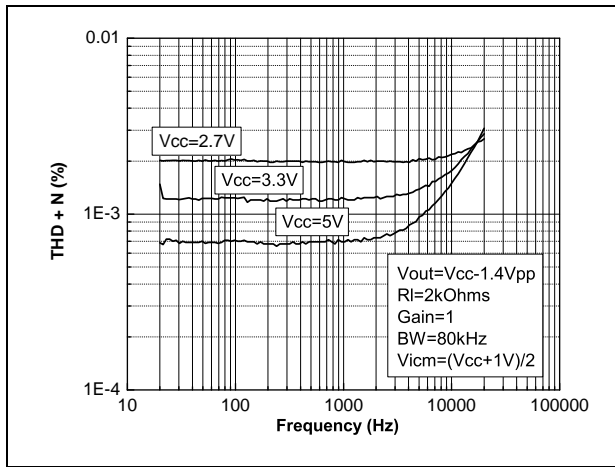


Figure 14. Distorsion + noise vs. output voltage

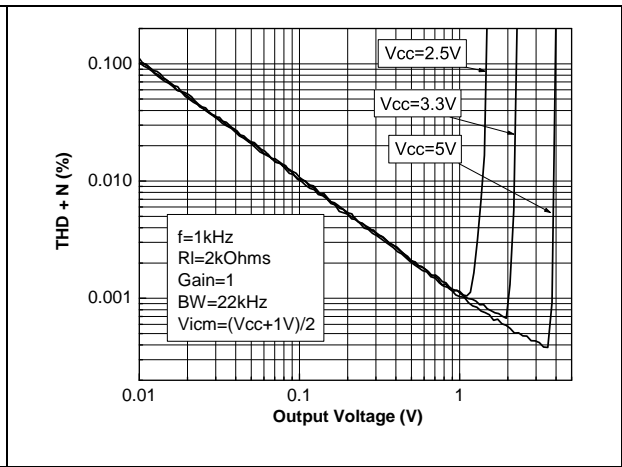
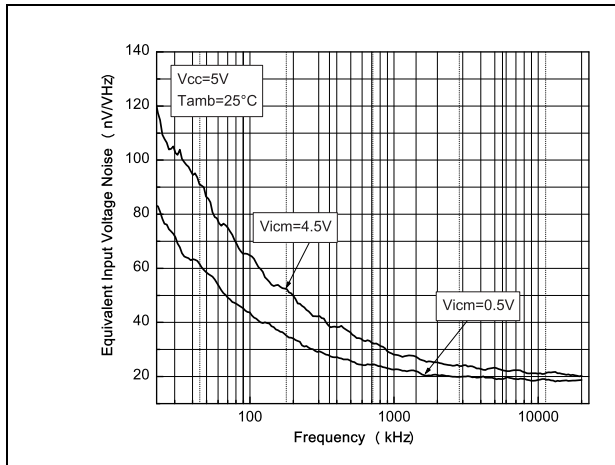


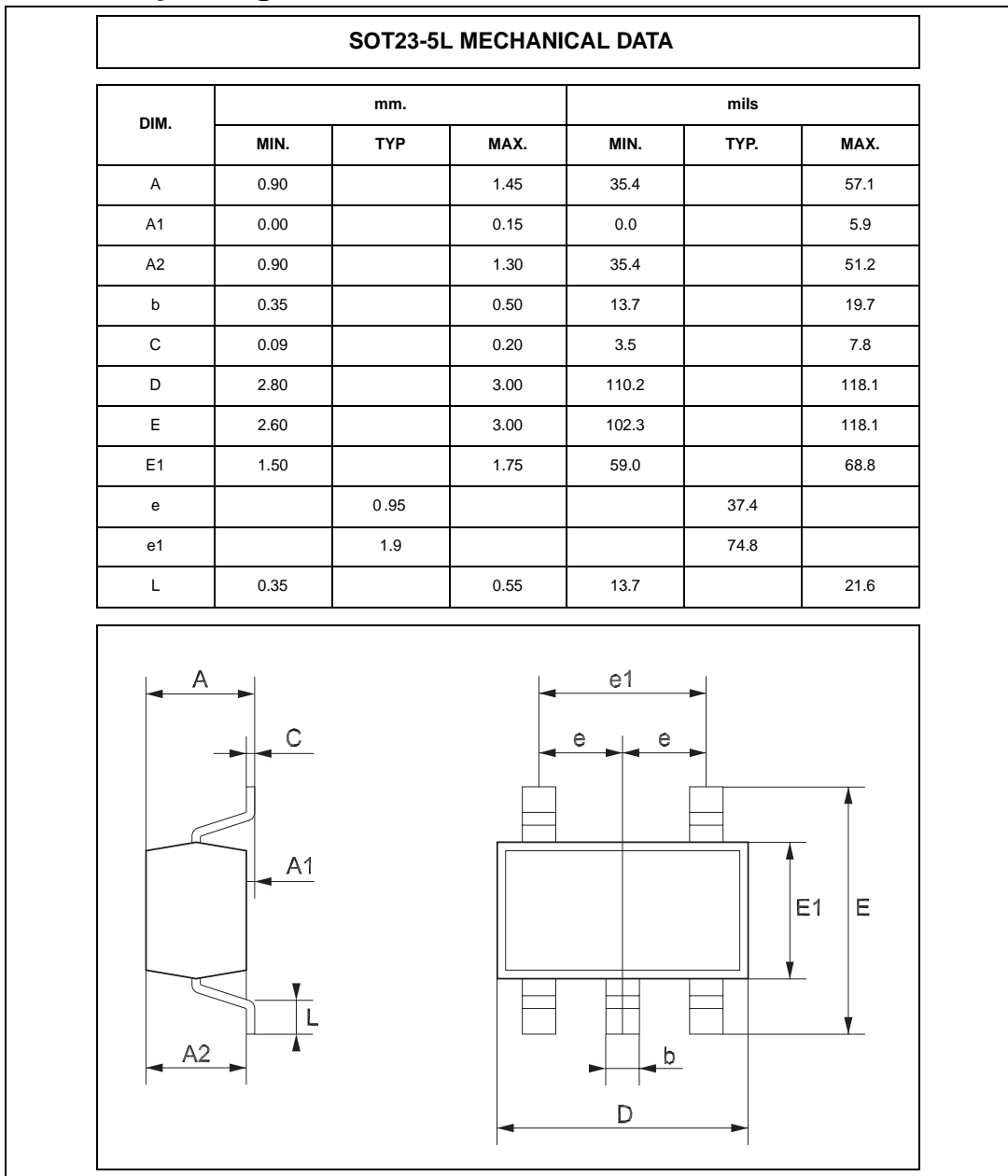
Figure 15. Noise vs. frequency



4 Package mechanical data

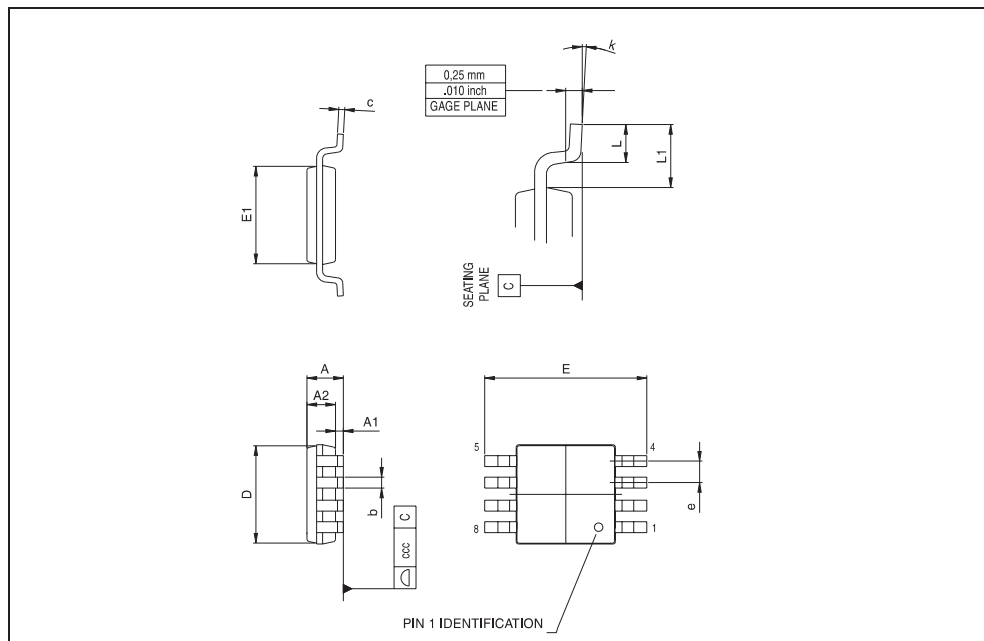
In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

4.1 SOT23-5 package

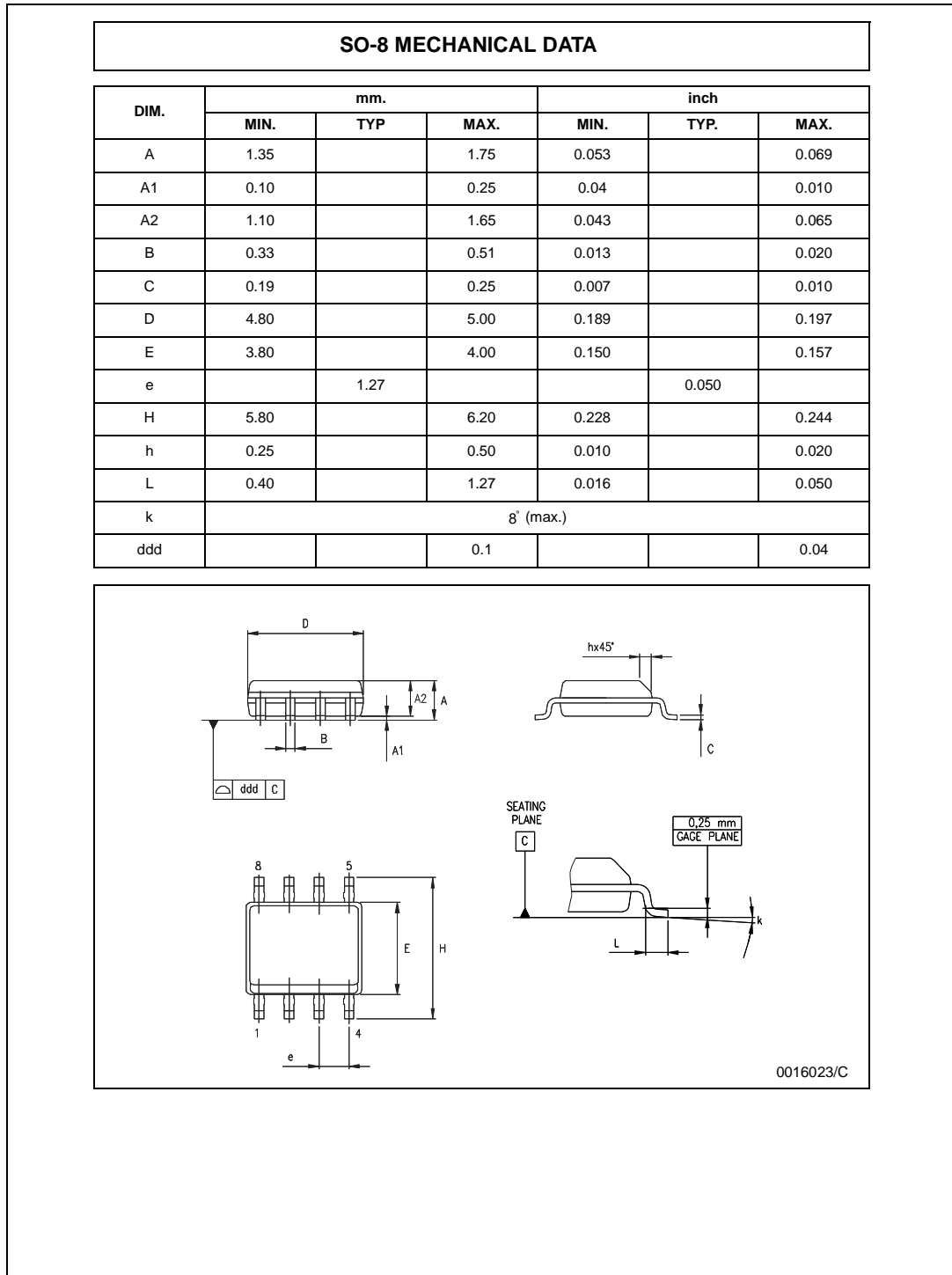


4.2 MiniSO-8 package

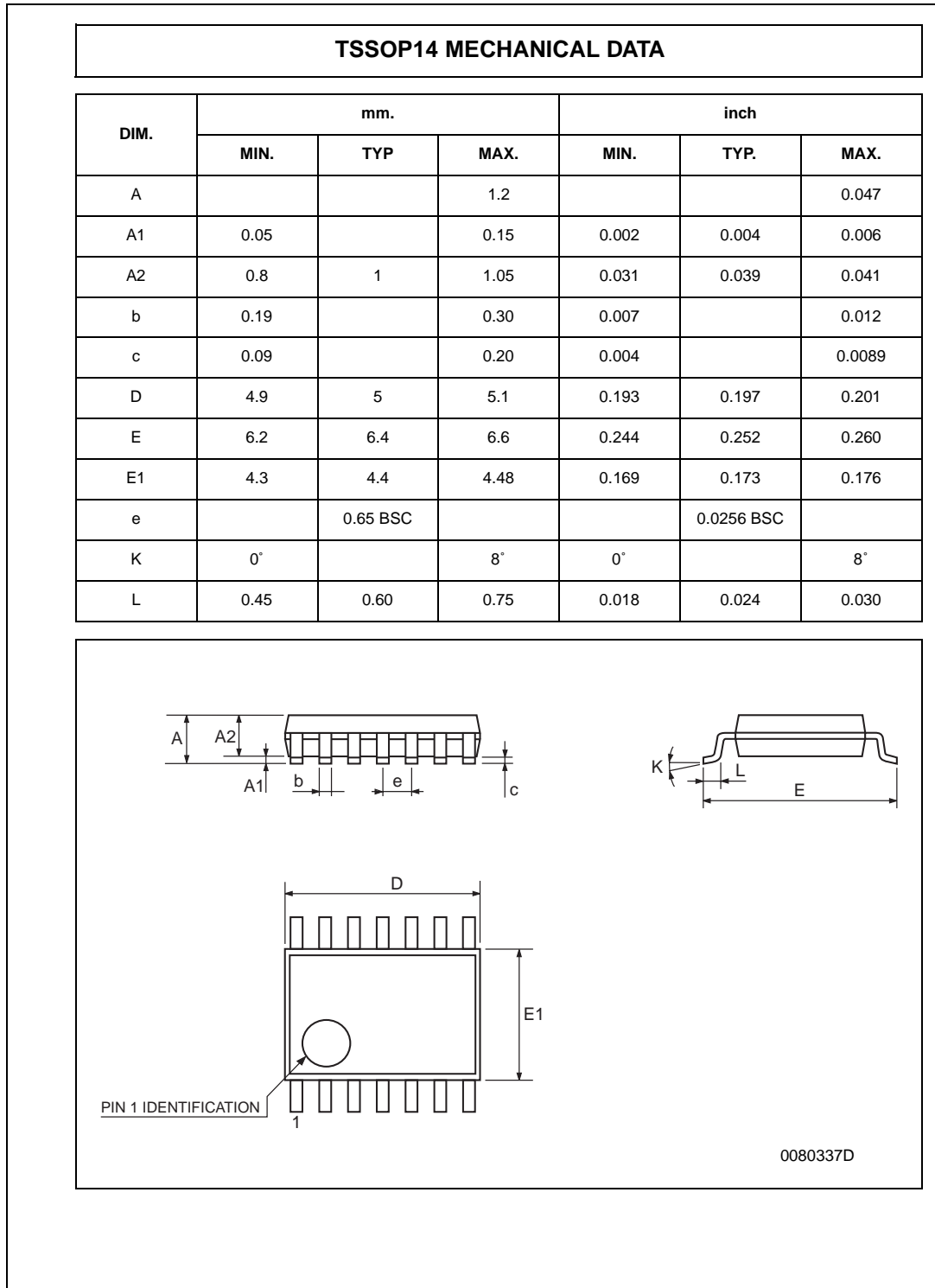
miniSO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.031	0.037
b	0.25	0.33	0.40	0.010	0.13	0.013
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	.0114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.004



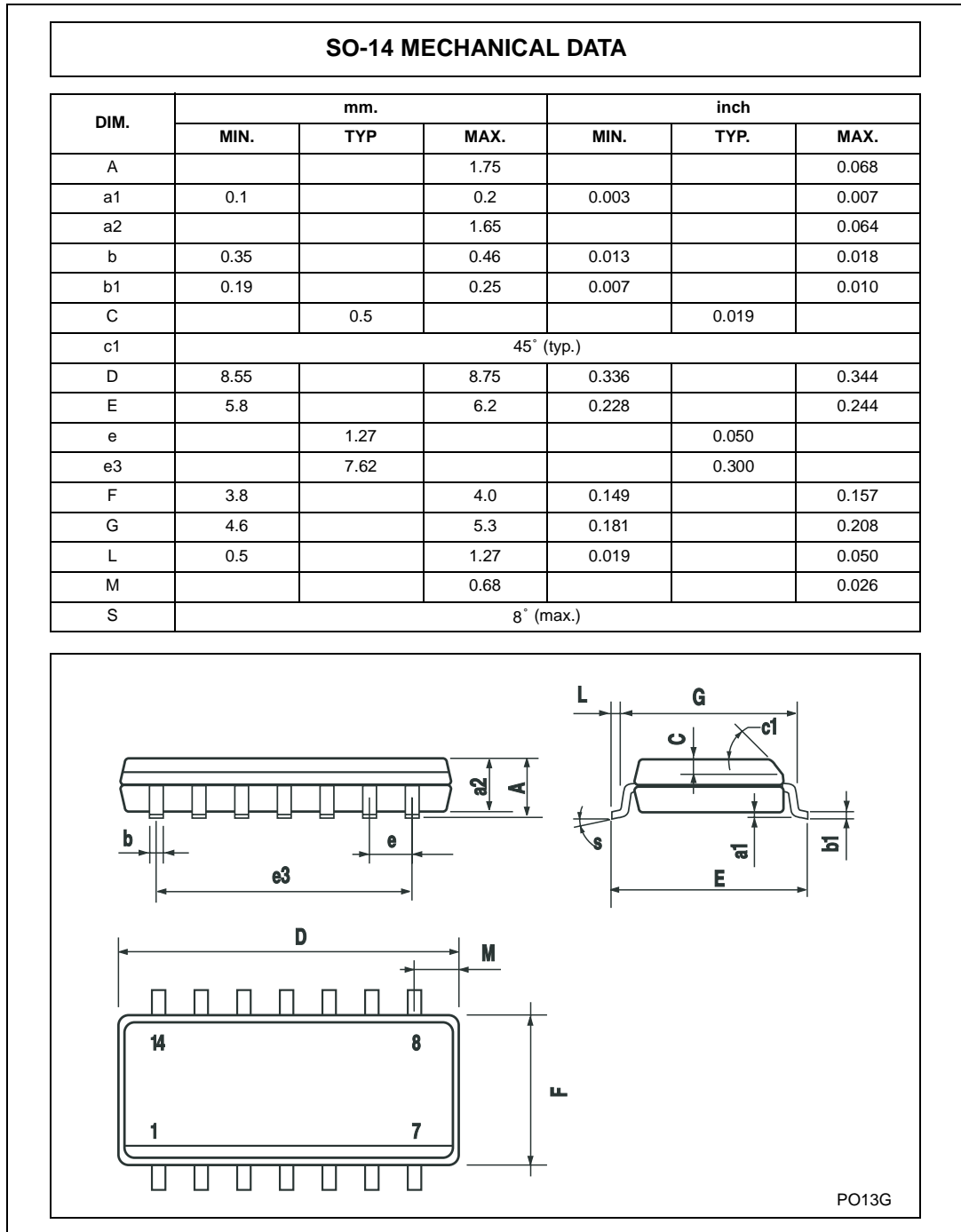
4.3 SO-8 package



4.4 TSSOP14 package



4.5 SO-14 package



5 Revision history

Table 6. Document revision history

Date	Revision	Changes
28-Aug-2006	1	First release.

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