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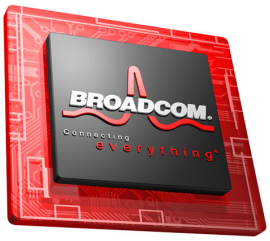
BCM1122 PRODUCT Brief



HIGH-PERFORMANCE MIPS CONTROL PROCESSOR

FEATURES

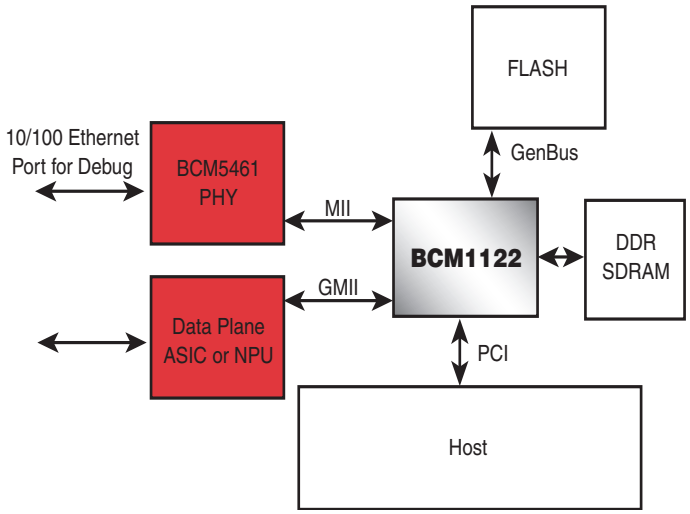
- **400 MHz MIPS64™ CPU**
  - Quad-issue in order pipeline; dual execute, dual memory pipes
  - Enhanced skew pipeline enables zero load-to-use penalty
  - 32-KB instruction cache, 32-KB data cache
  - Advanced branch predictors
- **Fast, on-chip memory-coherent bus (ZBbus)**
  - Connects the CPU, L2 cache, memory controller and I/O bridges
  - Runs at half the CPU core clock; 256 bits wide
- **On-chip L2 cache**
  - 128KB, shared by CPU and I/O bridges
  - Four-way associative, ECC protected
  - Ways can be removed to provide fast on-chip RAM
- **DDR memory controller**
  - One channel with a 64-bit data bus plus ECC
  - Runs at 100 MHz clock rate, 200 Mbps data rate
  - Support for DDR SDRAM, SGRAM, and FCRAM
- **High-speed packet interfaces**
  - One 10/100/1000 Ethernet MAC, and one 10/100 Ethernet MAC
  - 802.3 compliant with option to configure MAC into packet FIFO
- **PCI interface**
  - 32-bit, 33/66 MHz PCI 2.2
  - Host bridge or target device
- **Integrated system I/O**
  - Generic I/O for direct connect to boot ROM, FLASH, fast peripherals/ASICs
  - SMBus serial configuration interface
  - PCMCIA control interface
  - Two serial interfaces
- **Extensive, on-chip debug features**
- **4W @ 400 MHz**
- **Software-compatible with BCM1250 and BCM1125H**
- **Support for leading operating systems including VxWorks®, Linux®, NetBSD, QNX and OSE**
- **Evaluation board platform available with tools, firmware and software drivers**

SUMMARY OF BENEFITS

- **Industry-leading performance**
  - 2.2 Dhrystone MIPS/MHz
  - 51-Gbps on-chip bus bandwidth, 13-Gbps memory bandwidth
- **Low power dissipation at 4W**
- **High functional integration**
- **Programming ease and flexibility based on MIPS64 ISA**
- **Scalable system architecture**
- **Broad tools and system software support**
- **Software-compatible with BCM1250 and BCM1125H**

APPLICATIONS

- **The BCM1122's world-class performance, power efficiency and integration makes these processors ideal for a broad variety of systems including:**
  - Networking: routers, switches
  - Control plane processing
  - Line cards
  - Broadband access: DSLAM, CMTS, BRAS
  - Wireless base stations
  - Storage: RAID controllers, NAS controllers, HBAs
  - Web/networking/caching appliances
  - Imaging: printers, copiers



Example: PCI Card for TCP/IP Acceleration

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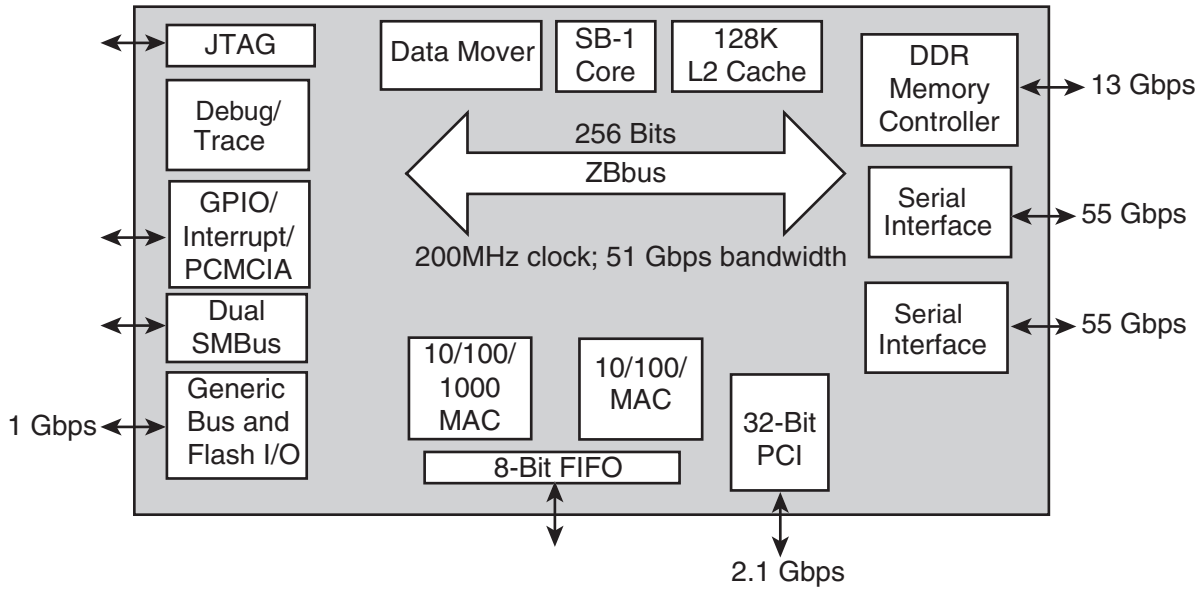
OVERVIEW



Broadcom's **BCM1122** is a state-of-the-art processor solution targeted at the fast-growing networking, wireless communications, storage, server/networking appliance and imaging markets. The **BCM1122** offers industry-leading performance, high functional integration, and low power levels in a small package required by next-generation networking applications.

The **BCM1122** is software-compatible with the BCM1125H and the dual-processor BCM1250 and share development and modeling tools, firmware, and operating systems. The **BCM1122** is an intelligent system-on-a-chip consisting of a Broadcom SB-1 high performance MIPS64 CPU, a shared 128-KB L2 cache, a DDR memory controller, and an integrated I/O. All major blocks of the processor are connected together via the ZBbus, a high-speed, low-latency, split-transaction, memory-coherent bus. The bus implements the standard MESI protocol to ensure coherency between the CPU, L2 cache, I/O agents, and memory.

One Gigabit Ethernet MAC (10/100/1000) and one Fast Ethernet MAC (10/100) enable easy interfacing to LANs as well as connecting to data plane components over the Ethernet or packet FIFO interface. In cases where Ethernet protocol processing is not required, the Gigabit Ethernet MAC can be configured as an 8-bit packet FIFO. High-speed I/O is provided using a 66-MHz (rev 2.2) PCI local bus.

Two serial ports are provided for WAN connections at up to T3/OC-1 rates (55 Mbps). To enable low-chip-count systems, the **BCM1122** processors also include a configurable generic bus that allows glueless connection of a boot ROM or FLASH memory and simple I/O peripherals. On-chip debugging, tracing, and performance monitoring functions assist both hardware and software designers in debugging and tuning the system. The system can be run in either big- or little-endian mode. The **BCM1122** is manufactured in TSMC's 0.13-µ process, and is packaged in pin-compatible 31-mm BGA package that is pin-compatible with the BCM1125H.

Implementation of MIPS64 ISA

The SB-1 CPU core is a high-performance implementation of the standard MIPS64 Instruction Set Architecture (ISA), and incorporates the MIPS-3D and MIPS-MDMX Application Specific Extensions (ASEs). The core supports a four-issue enhanced skew pipeline and can dispatch up to two memory and two ALU (Integer, Floating Point, MDMX or MIPS-3D) instructions per cycle.

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BROADCOM CORPORATION
16215 Alton Parkway, P.O. Box 57013
Irvine, California 92619-7013

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Phone: 949-450-8700
Fax: 949-450-8710
E-mail: info@broadcom.com
Web: www.broadcom.com