

# MC10H164

## 8-Line Multiplexer

### Description

The MC10H164 is a MECL 10H™ part which is a functional/pinout duplication of the standard MECL 10K™ family part, with 100% improvement in propagation delay, and no increase in power supply current.

The MC10H164 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional MC10H164's.

### Features

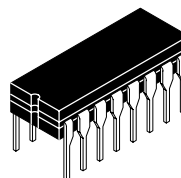
- Propagation Delay, 1.0 ns Typical
- Power Dissipation, 310 mW Typical (same as MECL 10K)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible
- Pb-Free Packages are Available\*



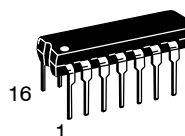
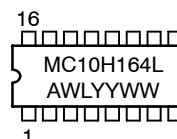
**ON Semiconductor®**

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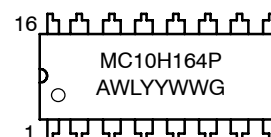
### MARKING DIAGRAMS\*



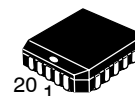
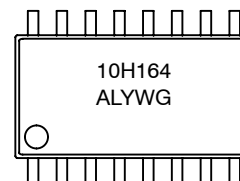
**CDIP-16  
L SUFFIX  
CASE 620A**



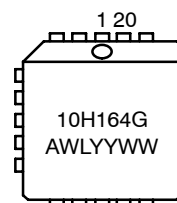
**PDIP-16  
P SUFFIX  
CASE 648**



**SOEIAJ-16  
CASE 966**



**PLLC-20  
FN SUFFIX  
CASE 775**



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

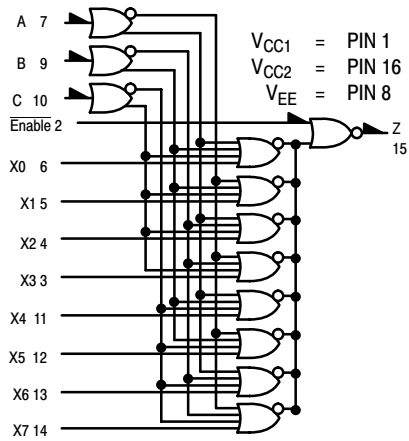
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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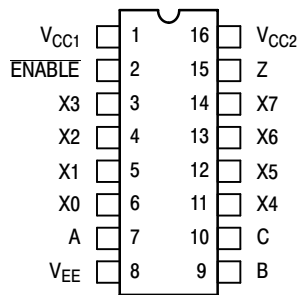
## LOGIC DIAGRAM



## TRUTH TABLE

ENABLE	ADDRESS INPUTS			Z
	C	B	A	
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	L

## DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 18  
of the ON Semiconductor MECL Data Book (DL122/D).

**Table 1. MAXIMUM RATINGS**

Symbol	Characteristic	Rating	Unit
$V_{EE}$	Power Supply ( $V_{CC} = 0$ )	-8.0 to 0	Vdc
$V_I$	Input Voltage ( $V_{CC} = 0$ )	0 to $V_{EE}$	Vdc
$I_{out}$	Output Current - Continuous - Surge	50 100	mA
$T_A$	Operating Temperature Range	0 to +75	°C
$T_{stg}$	Storage Temperature Range - Plastic - Ceramic	-55 to +150 -55 to +165	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

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**Table 2. ELECTRICAL CHARACTERISTICS** ( $V_{EE} = -5.2\text{ V} \pm 5\%$ ) (Note 1)

Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
$I_E$	Power Supply Current	-	83	-	75	-	83	mA
$I_{inH}$	Input Current High	-	512	-	320	-	320	$\mu\text{A}$
$I_{inL}$	Input Current Low	0.7	-	0.7	-	0.7	-	$\mu\text{A}$
$V_{OH}$	High Output Voltage	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
$V_{OL}$	Low Output Voltage	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
$V_{IH}$	High Input Voltage	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
$V_{IL}$	Low Input Voltage	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

1. Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50  $\Omega$  resistor to -2.0 V.

**Table 3. AC PARAMETERS**

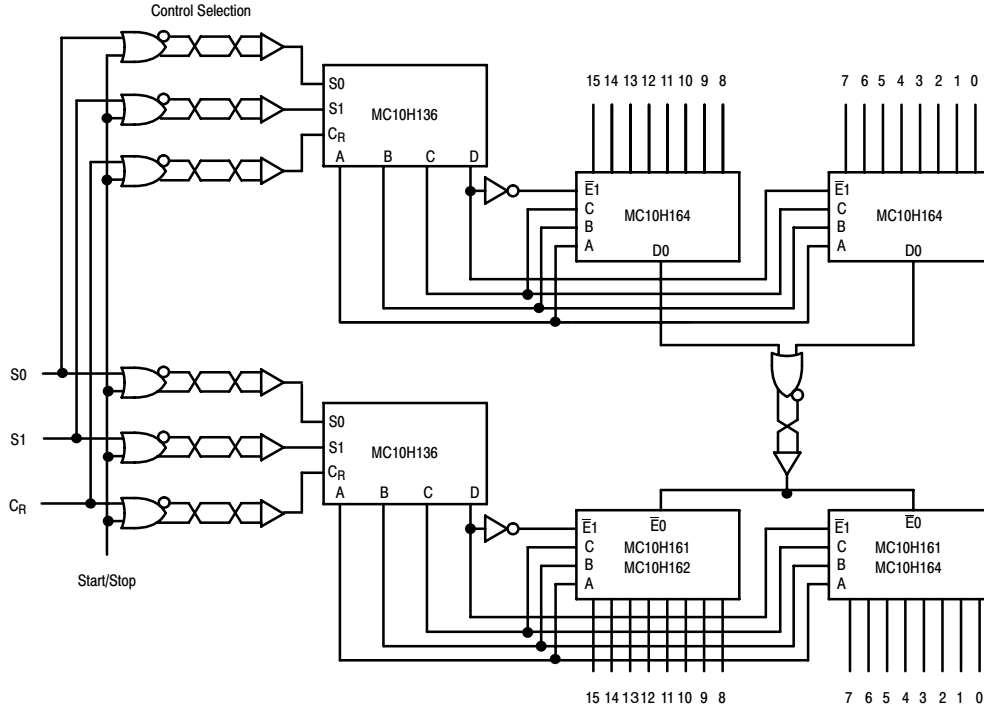
Symbol	Characteristic	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
$t_{pd}$	Propagation Delay							ns
	Enable	0.4	1.45	0.4	1.5	0.5	1.7	
	Data	0.7	2.4	0.8	2.5	0.9	2.6	
	Address	1.0	2.8	1.1	2.9	1.2	3.2	
$t_r$	Rise Time	0.5	1.5	0.5	1.6	0.5	1.7	ns
$t_f$	Fall Time	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 l/fpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

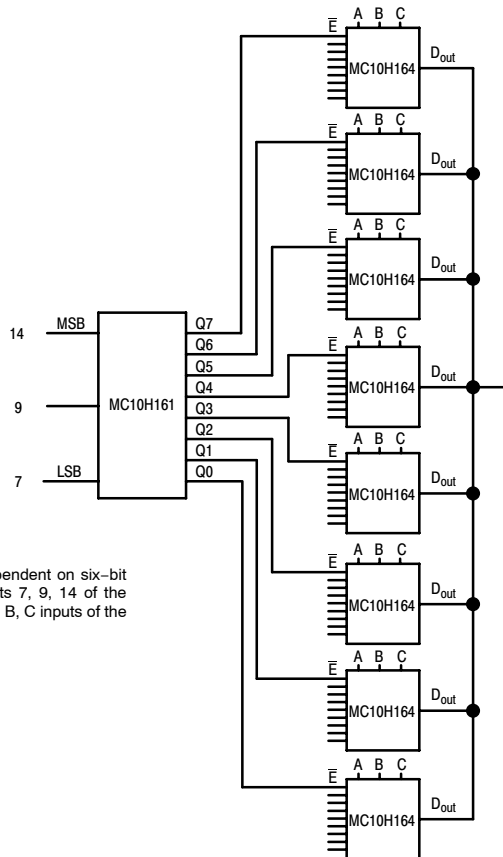
# MC10H164

## TYPICAL APPLICATIONS

**FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER**



**FIGURE 2 – 1-OF-64 LINE MULTIPLEXER**



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10H161 and the A, B, C inputs of the MC10H164.

## MC10H164

### ORDERING INFORMATION

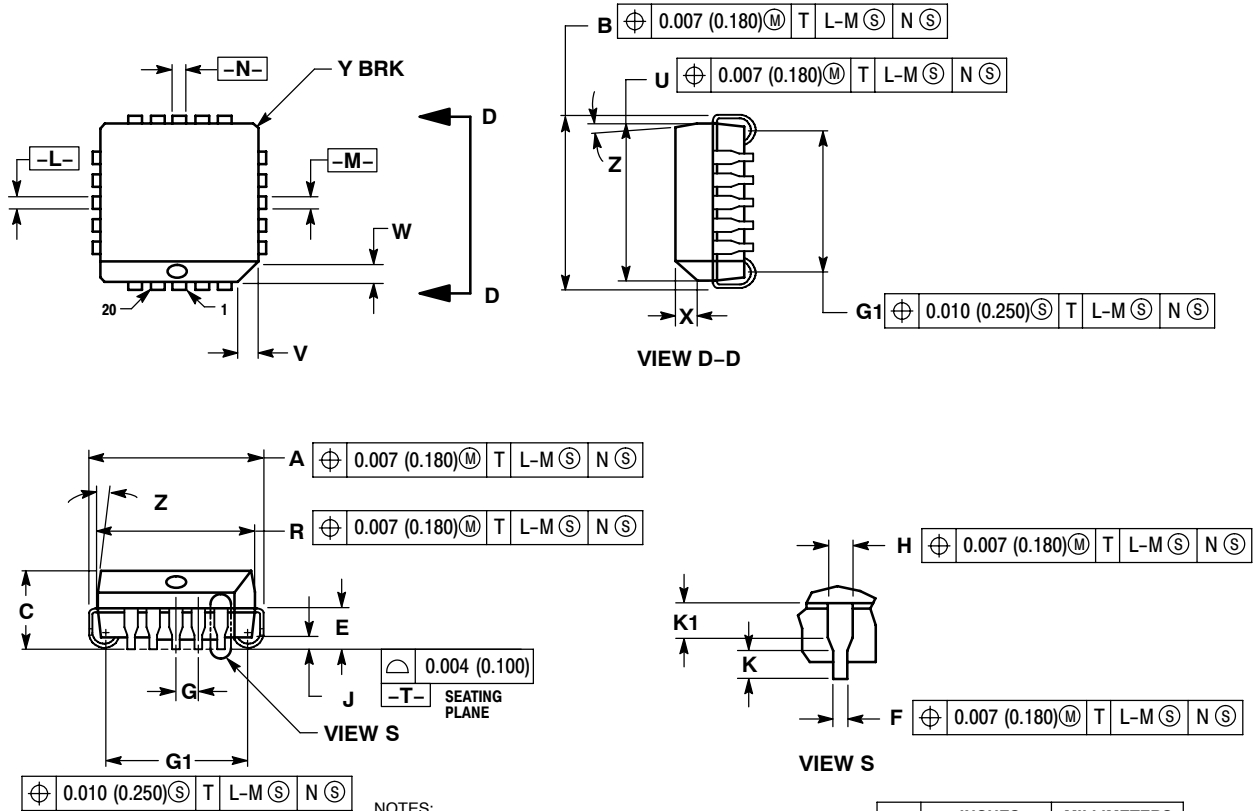
Device	Package	Shipping†
MC10H164FN	PLLC-20	46 Units / Rail
MC10H164FNG	PLLC-20 (Pb-Free)	46 Units / Rail
MC10H164FNR2	PLLC-20	500 / Tape & Reel
MC10H164FNR2G	PLLC-20 (Pb-Free)	500 / Tape & Reel
MC10H164L	CDIP-16	25 Unit / Rail
MC10H164M	SOEIAJ-16	50 Unit / Rail
MC10H164MG	SOEIAJ-16 (Pb-Free)	50 Unit / Rail
MC10H164MEL	SOEIAJ-16	2000 / Tape & Reel
MC10H164MELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel
MC10H164P	PDIP-16	25 Unit / Rail
MC10H164PG	PDIP-16 (Pb-Free)	25 Unit / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

20 LEAD PLLC  
CASE 775-02  
ISSUE E



**NOTES:**

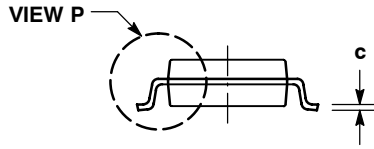
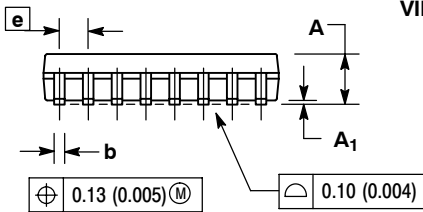
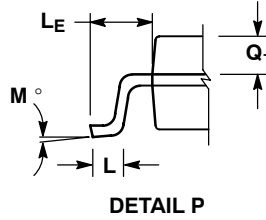
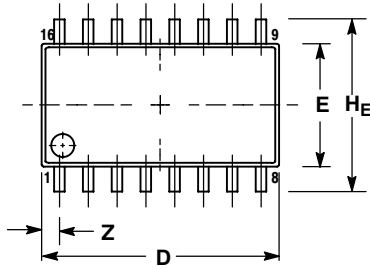
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSIONS IN INCHES.
3. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
4. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
5. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
6. DIMENSIONS IN THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.310	0.330	7.88	8.38
K1	0.040	---	1.02	---

# MC10H164

## PACKAGE DIMENSIONS

### SOEIAJ-16 CASE 966-01 ISSUE A

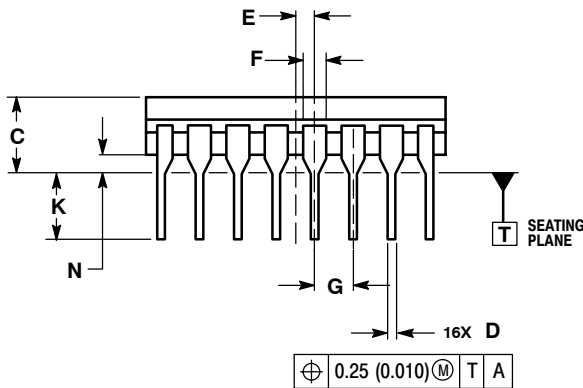
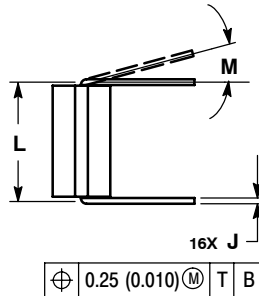
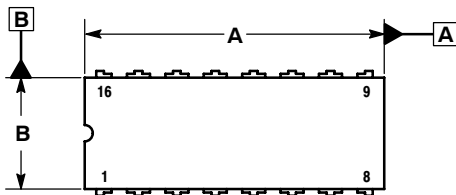


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC			
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

### CDIP-16 L SUFFIX CERAMIC DIP PACKAGE CASE 620A-01 ISSUE O



NOTES:

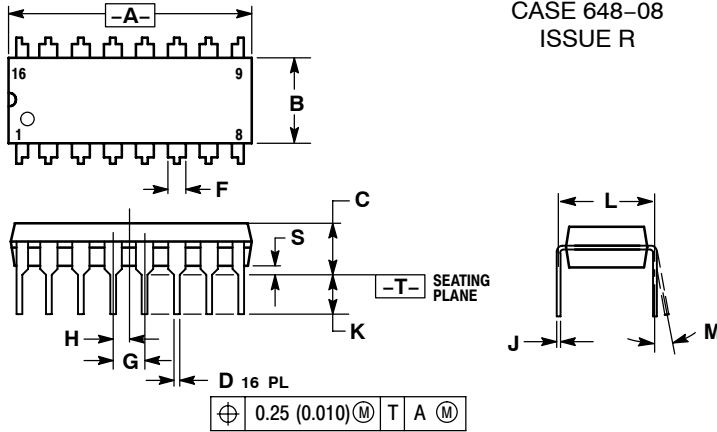
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. THIS DRAWING REPLACES OBSOLETE CASE OUTLINE 620-10.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC			
F	0.055	0.065	1.40	1.65
G	0.100 BSC			
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC			
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

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## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE R



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

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