Dual D-Type Flip-Flop with Set and Reset

The MC74VHCT74A is an advanced high speed CMOS D-type flip-flop fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The signal level applied to the D input is transferred to Q output during the positive going transition of the Clock pulse.

Reset (\overline{RD}) and Set (\overline{SD}) are independent of the Clock (CP) and are accomplished by setting the appropriate input Low.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0~V, allowing the interface of 5.0~V systems to 3.0~V systems.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The VHCT74A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{\rm CC}=0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $f_{max} = 60 \text{ MHz}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu A \text{ (Max)}$ at $T_A = 25 \text{°C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 4.5 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- Pb-Free Packages are Available

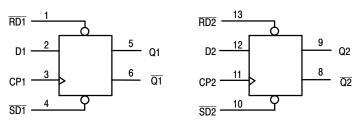


Figure 2. Logic Diagram

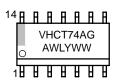


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MARKING DIAGRAMS









A = Assembly Location

WL, L = Wafer Lot Y = Year

WW, W = Work Week

G or ■ = Pb–Free Package

(Note: Microdot may be in either location)

RD1 [1 ●	14	v _{cc}
D1 [2	13	RD2
CP1 [3	12	D2
SD1 [4	11	CP2
Q1 [5	10	D SD2
Q1 [6	9	Q2
GND [7	8	Q2

Figure 1. Pin Assignment

FUNCTION TABLE

	Inputs				puts	
SD	RD	CP	D	Q	Q	
L	Н	Х	Χ	Н	L	
Н	L	X	Χ	L	Н	
L	L	X	X	H*	H*	
Н	Н		Н	Н	L	
Н	Н	\mathcal{L}	L	L	Н	
Н	Н	L	Χ	No Change		
Н	Н	Н	X	No Change		
Н	Н	~	Χ	No Cl	nange	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to + 7.0	V
V _{in}	DC Input Voltage	-0.5 to + 7.0	V
V _{out}	DC Output Voltage V _{CC} = 0 High or Low State	-0.5 to + 7.0 -0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current (V _{OUT} < GND; V _{OUT} > V _{CC})	±20	mA
l _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	-65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating – SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage V _{CC} = 0 High or Low State	0	5.5 V _{CC}	V
T _A	Operating Temperature	-40	+ 85	°C
t _r , t _f	Input Rise and Fall Time V _{CC} =5.0 V ± 0.5 V	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

			Vcc	T _A = 25°C		С	T _A = - 40 to 85°C		
Symbol	Parameter	Test Conditions	V	Min	Тур	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		4.5 to 5.5	2.0			2.0		V
V _{IL}	Maximum Low-Level Input Voltage		4.5 to 5.5			0.8		0.8	V
V _{OH}	Minimum High-Level Output	I _{OH} = -50 μA	4.5	4.4	4.5		4.4		V
	Voltage V _{in} = V _{IH} or V _{IL}	I _{OH} = -8 mA	4.5	3.94			3.80		
V _{OL}	Maximum Low–Level Output Voltage	I _{OL} = 50 μA	4.5		0.0	0.1		0.1	V
	$V_{in} = V_{IH}$ or V_{IL}	I _{OL} = 8 mA	4.5			0.36		0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μΑ
Icc	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			2.0		20.0	μΑ
Ісст	Quiescent Supply Current	Per Input: V _{IN} = 3.4 V Other Input: V _{CC} or GND	5.5			1.35		1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0			0.5		5.0	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

			T _A = 25°C		T _A = - 40 to 85°C			
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, CP to Q or Q	$V_{CC} = 5.0 \pm 0.5 V$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.8 6.3	7.8 8.8	1.0 1.0	9.0 10.0	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, SD or RD to Q or Q	$V_{CC} = 5.0 \pm 0.5 V$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	ns
f _{max}	Maximum Clock Frequency (50% Duty Cycle)	$V_{CC} = 5.0 \pm 0.5 V$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$	100 80	160 140		80 65		MHz
C _{in}	Maximum Input Capacitance			4	10		10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 1)	24	pF

^{1.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per flip–flop). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

TIMING REQUIREMENTS (Input $t_f = t_f = 3.0 \text{ ns}$)

		v _{cc}	Guara	anteed Limit	
Symbol	Parameter	v	T _A = 25°C	T _A = - 40 to 85°C	Unit
t _w	Minimum Pulse Width, CP	5.0 ± 0.5	5.0	5.0	ns
t _w	Minimum Pulse Width, RD or SD	5.0 ± 0.5	5.0	5.0	ns
t _{su}	Minimum Setup Time, D to CP	5.0 ± 0.5	5.0	5.0	ns
t _h	Minimum Hold Time, D to CP	5.0 ± 0.5	0.0	0.0	ns
t _{rec}	Minimum Recovery Time, SD or RD to CP	5.0 ± 0.5	3.5	3.5	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHCT74AD	SOIC-14	55 Units / Rail
MC74VHCT74ADR2	SOIC-14	2500 / Tape & Reel
MC74VHCT74ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74VHCT74ADT	TSSOP-14*	96 Units / Rail
MC74VHCT74ADTR2	TSSOP-14*	2500 / Tape & Reel
MC74VHCT74ADTR2G	TSSOP-14*	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *This package is inherently Pb–Free.

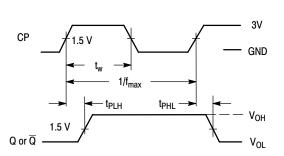


Figure 3. Switching Waveform

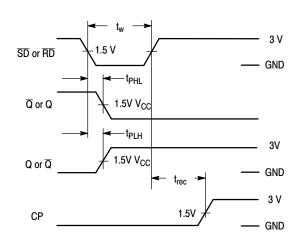


Figure 4. Switching Waveform

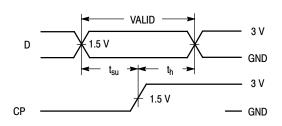
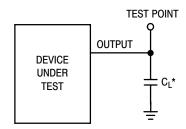


Figure 5. Switching Waveform



^{*}Includes all probe and jig capacitance

Figure 6. Switching Waveform

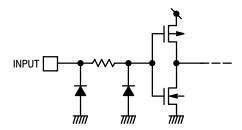
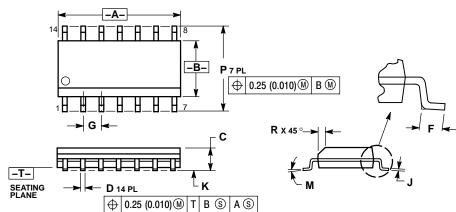


Figure 7. Input Equivalent Circuit

PACKAGE DIMENSIONS

SOIC-14 **D SUFFIX** CASE 751A-03 **ISSUE G**



- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

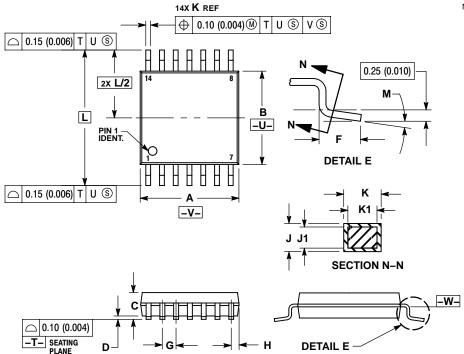
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

TSSOP-14 **DT SUFFIX** CASE 948G-01 ISSUE A



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- ANSI 114-301, 1902.

 CONTROLLING DIMENSION: MILLIMETER.

 JUMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE
- DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
 NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
U		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
7	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
Κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
М	0 °	8°	0°	8 °	

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