MGP15N40CL, MGB15N40CL

Preferred Device

Ignition IGBT 15 Amps, 410 Volts

N–Channel TO–220 and D2PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

- Ideal for Coil–On–Plug, IGBT–On–Coil, or Distributorless Ignition System Applications
- High Pulsed Current Capability up to 50 A
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- Optional Gate Resistor (R_G)

MAXIMUM RATINGS (–55°C ≤ T_J ≤ 175°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	440	V_{DC}
Collector–Gate Voltage	V_{CER}	440	V_{DC}
Gate–Emitter Voltage	V_{GE}	22	V_{DC}
Collector Current–Continuous @ T_C = 25°C – Pulsed	I_C	15 50	A_{DC} A_{AC}
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	800	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS (–55°C ≤ T_J ≤ 175°C)

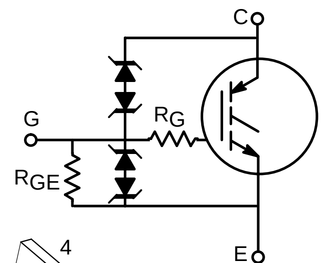
Characteristic	Symbol	Value	Unit
Single Pulse Collector–to–Emitter Avalanche Energy V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 17.4 A, L = 2.0 mH, Starting T_J = 25°C V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 14.2 A, L = 2.0 mH, Starting T_J = 150°C	E_{AS}	 300 200	mJ
Reverse Avalanche Energy V_{CC} = 100 V, V_{GE} = 20 V, L = 3.0 mH, Pk I_L = 25.8 A, Starting T_J = 25°C	$E_{AS(R)}$	1000	mJ

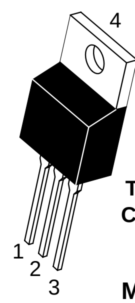
ON Semiconductor®

http://onsemi.com

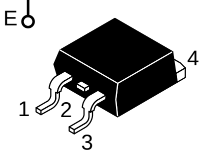
15 AMPERES
410 VOLTS (Clamped)
$V_{CE(on)}$ @ 10 A = 1.8 V Max

N–Channel



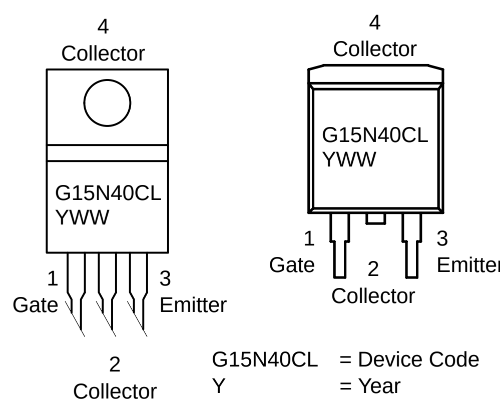


TO–220AB CASE 221A STYLE 9



D2PAK CASE 418B STYLE 4

MARKING DIAGRAMS & PIN ASSIGNMENTS



G15N40CL = Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MGP15N40CL	TO–220	50 Units/Rail
MGB15N40CLT4	D2PAK	800 Tape & Reel

Preferred devices are recommended choices for future use and best overall value.

April, 2002 – Rev. 7
Publication Order Number: MGP15N40CL/D

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	TO–220	$R_{\theta JA}$	62.5	°C/W
	D^2PAK (Note 1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Collector–Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = –40°C to 150°C	380	410	440	V_{DC}
		I_C = 10 mA	T_J = –40°C to 150°C	390	420	450	V_{DC}
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25°C	–	1.5	20	μA_{DC}
		V_{CE} = 350 V, V_{GE} = 0 V	T_J = 150°C	–	10	40*	μA_{DC}
		V_{CE} = 350 V, V_{GE} = 0 V	T_J = –40°C	–	0.7	1.5	μA_{DC}
Reverse Collector–Emitter Leakage Current	I_{ECS}	V_{CE} = –24 V	T_J = 25°C	–	0.35	1.0	mA
		V_{CE} = –24 V	T_J = 150°C	–	8.0	15*	mA
		V_{CE} = –24 V	T_J = –40°C	–	0.05	0.5	mA
Reverse Collector–Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = –75 mA	T_J = 25°C	25	33	50	V_{DC}
		I_C = –75 mA	T_J = 150°C	25	36	50	V_{DC}
		I_C = –75 mA	T_J = –40°C	25	30	50	V_{DC}
Gate–Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = –40°C to 150°C	17	20	22	V_{DC}
Gate–Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = –40°C to 150°C	384	600	1000	μA_{DC}
Gate Resistor (Optional)	R_G	–	T_J = –40°C to 150°C	–	70	–	Ω
Gate Emitter Resistor	R_{GE}	–	T_J = –40°C to 150°C	10	16	26	kΩ
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 25°C	1.4	1.7	2.0	V_{DC}
		I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = 150°C	0.75	1.1	1.4	V_{DC}
		I_C = 1.0 mA, V_{GE} = V_{CE}	T_J = –40°C	1.6	1.9	2.1*	V_{DC}
Threshold Temperature Coefficient (Negative)	–	–	–	–	4.4	–	mV/°C

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
ON CHARACTERISTICS (continued) (Note 3)							
Collector–to–Emitter On–Voltage	$V_{CE(on)}$	I_C = 6.0 A, V_{GE} = 4.0 V	T_J = 25°C	1.0	1.3	1.6	V_{DC}
			T_J = 150°C	0.9	1.2	1.5	
			T_J = –40°C	1.1	1.4	1.7*	
		I_C = 10 A, V_{GE} = 4.0 V	T_J = 25°C	1.3	1.6	1.9	
			T_J = 150°C	1.2	1.5	1.8	
			T_J = –40°C	1.3	1.6	1.9*	
		I_C = 15 A, V_{GE} = 4.0 V	T_J = 25°C	1.6	1.95	2.25	
			T_J = 150°C	1.7	2.0	2.3*	
			T_J = –40°C	1.6	1.9	2.2	
		I_C = 20 A, V_{GE} = 4.0 V	T_J = 25°C	1.9	2.2	2.5	
			T_J = 150°C	2.1	2.4	2.7*	
			T_J = –40°C	1.85	2.15	2.45	
		I_C = 25 A, V_{GE} = 4.0 V	T_J = 25°C	2.1	2.5	2.9	
			T_J = 150°C	2.5	2.9	3.3*	
			T_J = –40°C	2.0	2.4	2.8	
Collector–to–Emitter On–Voltage	$V_{CE(on)}$	I_C = 10 A, V_{GE} = 4.5 V	T_J = 150°C	–	1.5	1.8	V_{DC}
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = –40°C to 150°C	8.0	15	25	Mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	C_{ISS}	V_{CC} = 25 V, V_{GE} = 0 V f = 1.0 MHz	T_J = –40°C to 150°C	–	1000	1300	pF
Output Capacitance	C_{OSS}			–	100	130	
Transfer Capacitance	C_{RSS}			–	5.0	8.0	
SWITCHING CHARACTERISTICS (Note 3)							
Turn–Off Delay Time (Inductive)	$t_{d(off)}$	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, L = 300 μH	T_J = 25°C	–	4.0	10	μSec
			T_J = 150°C	–	4.5	10	
Fall Time (Inductive)	t_f	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, L = 300 μH	T_J = 25°C	–	7.0	10	
			T_J = 150°C	–	10	15*	
Turn–Off Delay Time (Resistive)	$t_{d(off)}$	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	4.0	10	μSec
			T_J = 150°C	–	4.5	10	
Fall Time (Resistive)	t_f	V_{CC} = 300 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	–	13	20	
			T_J = 150°C	–	16	20	
Turn–On Delay Time	$t_{d(on)}$	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω	T_J = 25°C	–	1.0	1.5	μSec
			T_J = 150°C	–	1.0	1.5	
Rise Time	t_r	V_{CC} = 10 V, I_C = 6.5 A R_G = 1.0 kΩ, R_L = 1.5 Ω	T_J = 25°C	–	4.5	6.0	
			T_J = 150°C	–	5.0	6.0	

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
*Maximum Value of Characteristic across Temperature Range.

TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

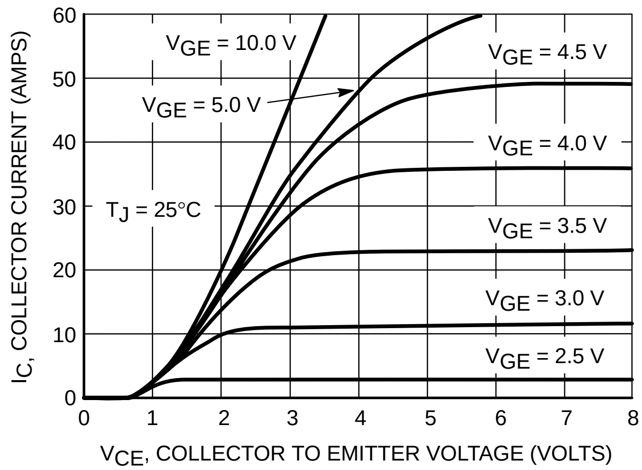


Figure 1. Output Characteristics

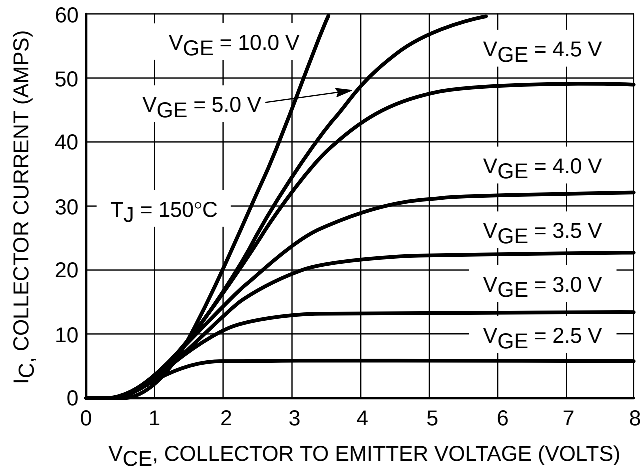


Figure 2. Output Characteristics

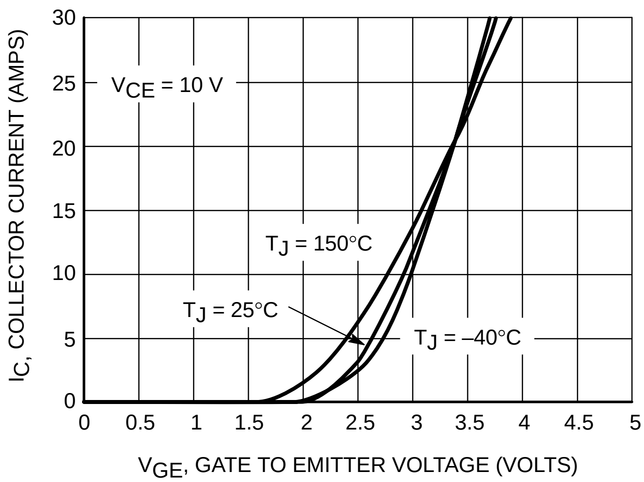


Figure 3. Transfer Characteristics

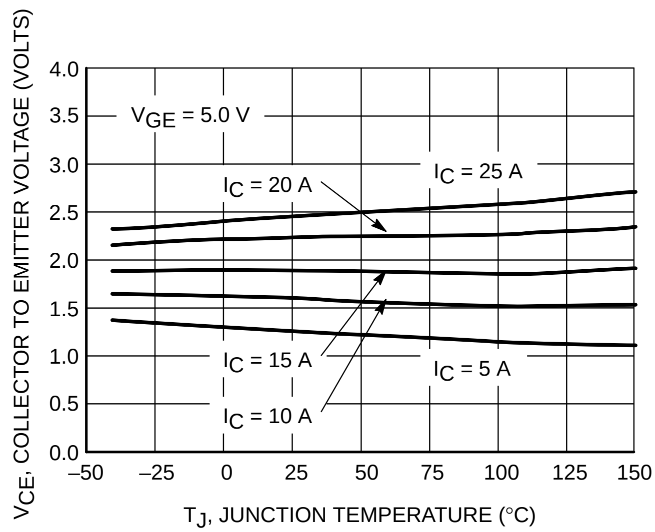


Figure 4. Collector–to–Emitter Saturation Voltage vs. Junction Temperature

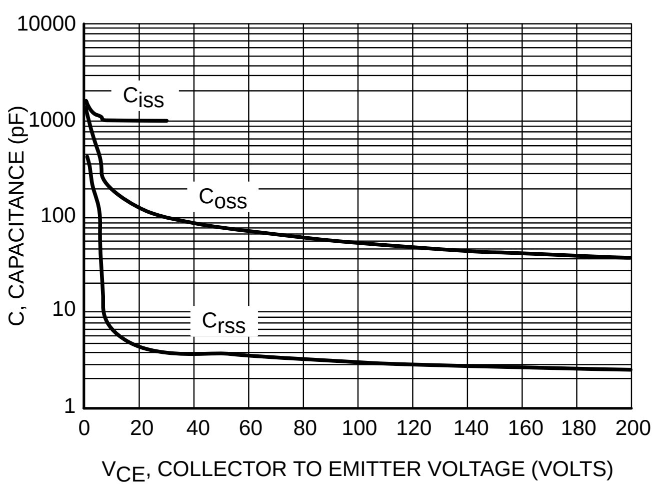


Figure 5. Capacitance Variation

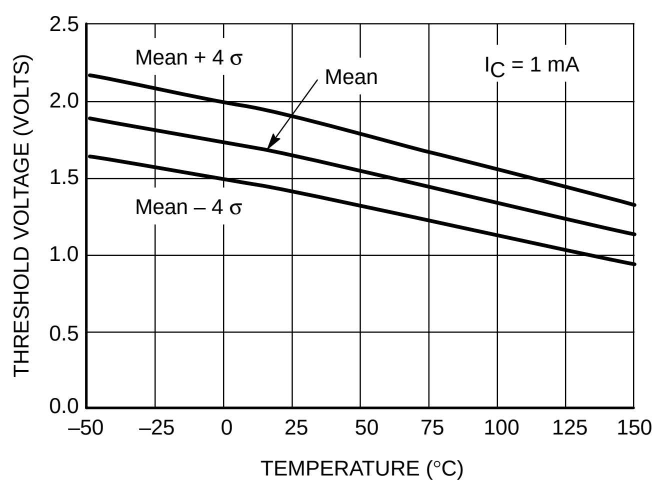


Figure 6. Threshold Voltage vs. Temperature

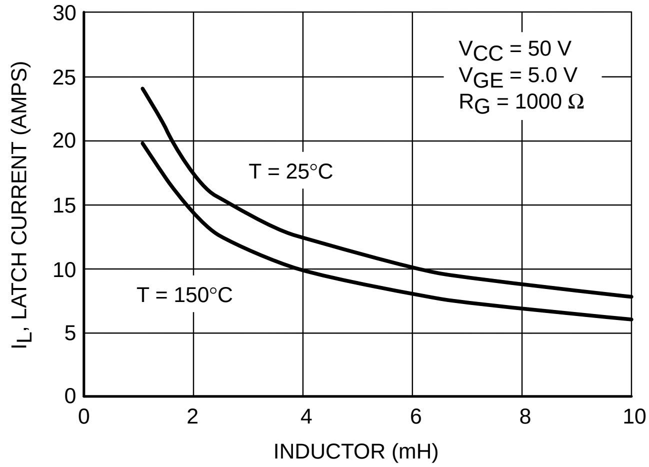


Figure 7. Minimum Open Secondary Latch Current vs. Inductor

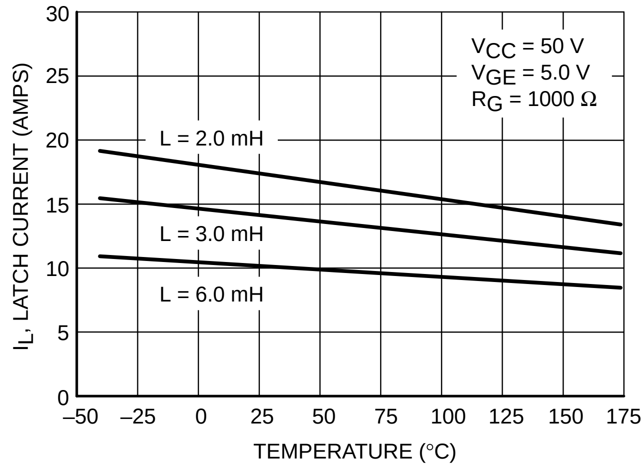


Figure 8. Minimum Open Secondary Latch Current vs. Temperature

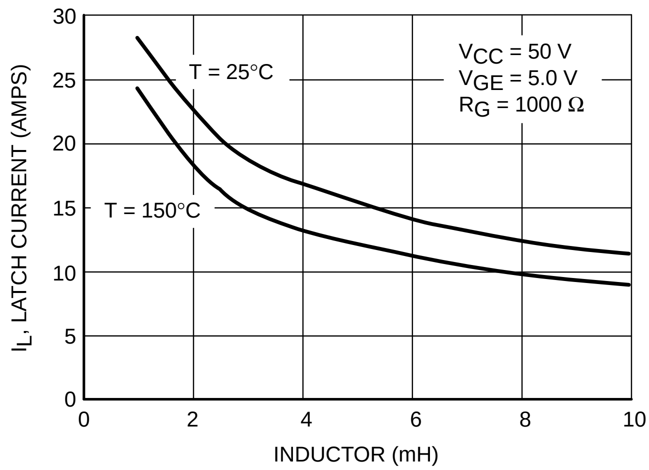


Figure 9. Typical Open Secondary Latch Current vs. Inductor

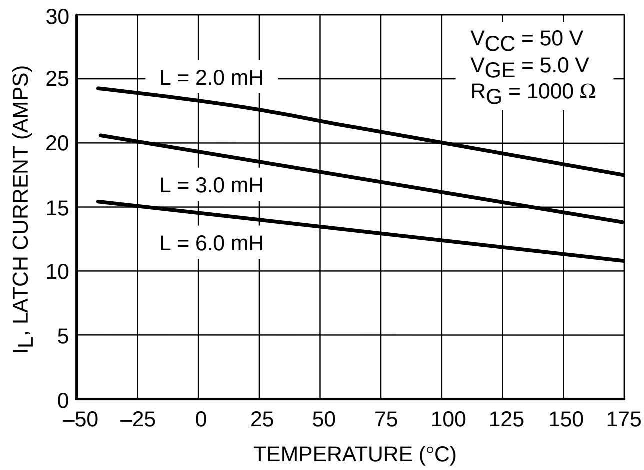


Figure 10. Typical Open Secondary Latch Current vs. Temperature

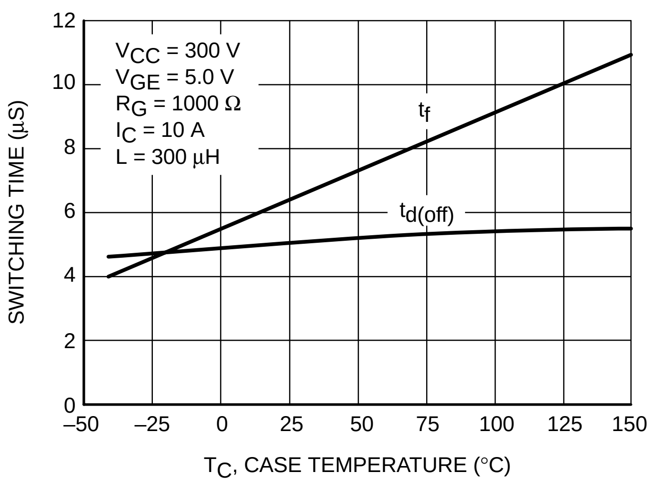


Figure 11. Switching Speed vs. Case Temperature

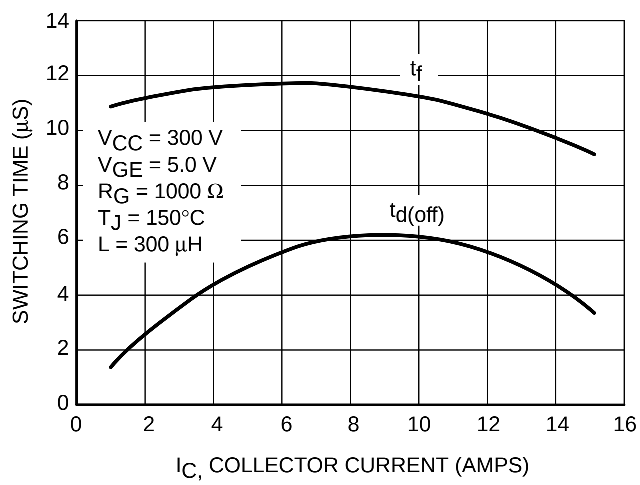


Figure 12. Switching Speed vs. Collector Current

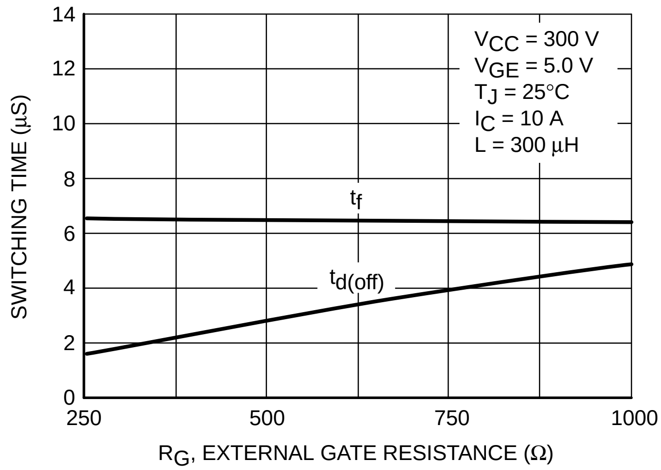


Figure 13. Switching Speed vs. External Gate Resistance

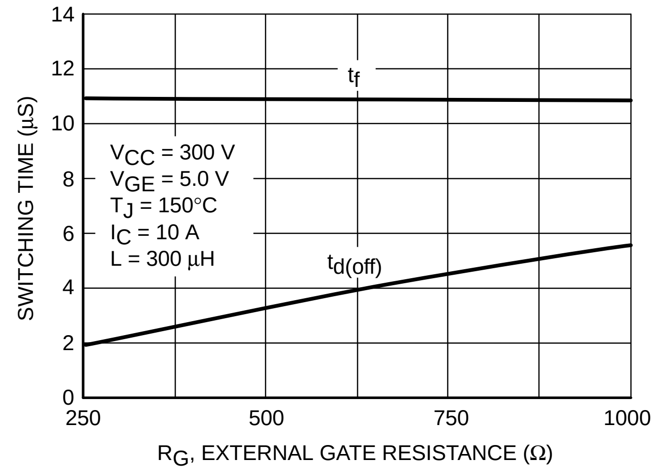


Figure 14. Switching Speed vs. External Gate Resistance

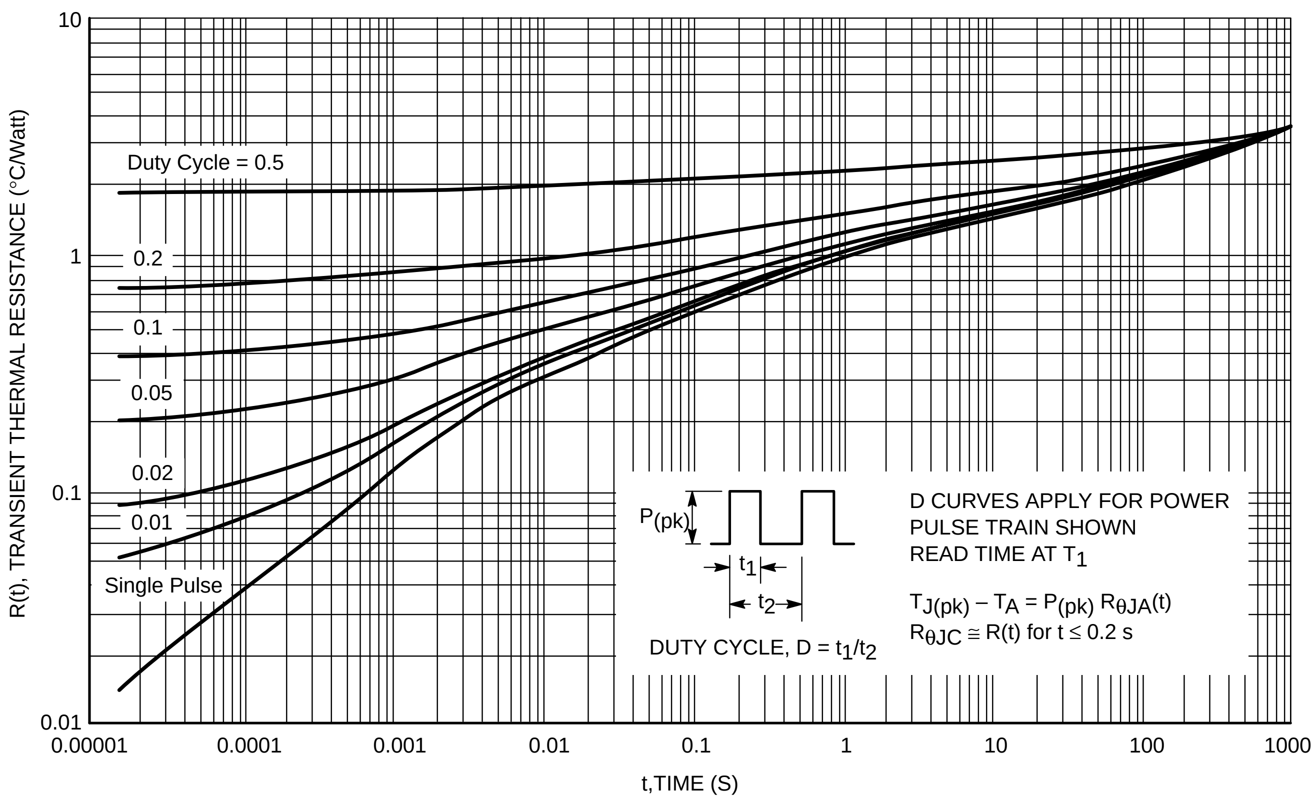


Figure 15. Transient Thermal Resistance (Non–normalized Junction–to–Ambient mounted on fixture in Figure 16)

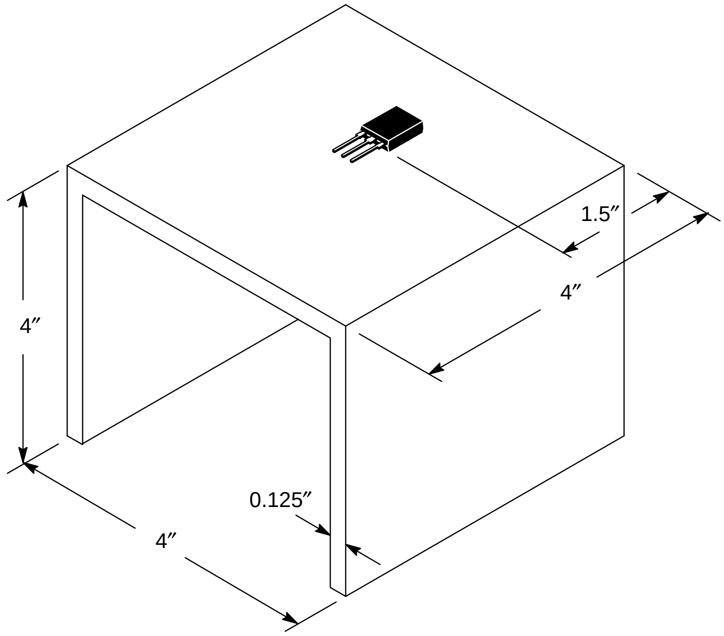


Figure 16. Test Fixture for Transient Thermal Curve (48 square inches of 1/8″ thick aluminum)

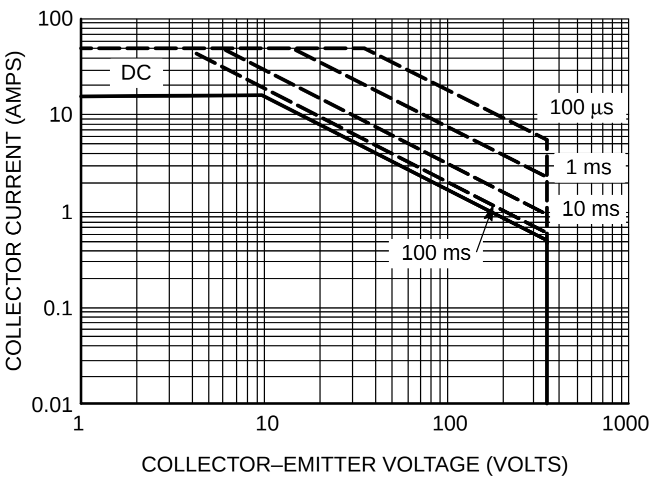


Figure 17. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 25°C)

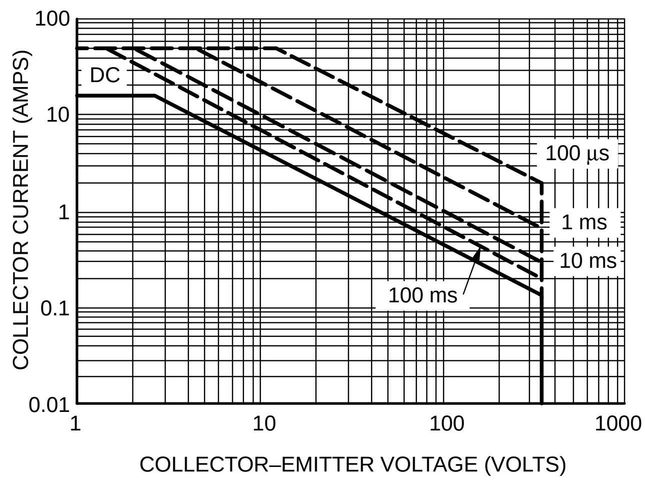


Figure 18. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 125°C)

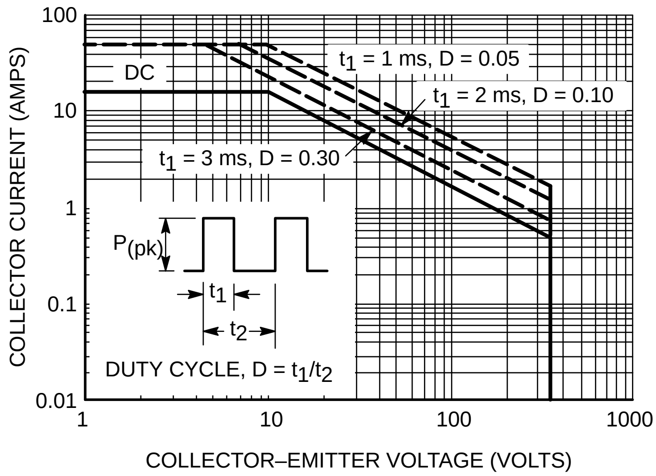


Figure 19. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 25°C)

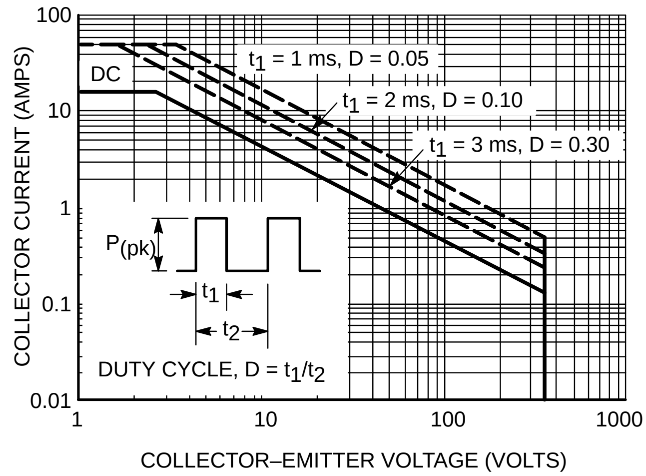
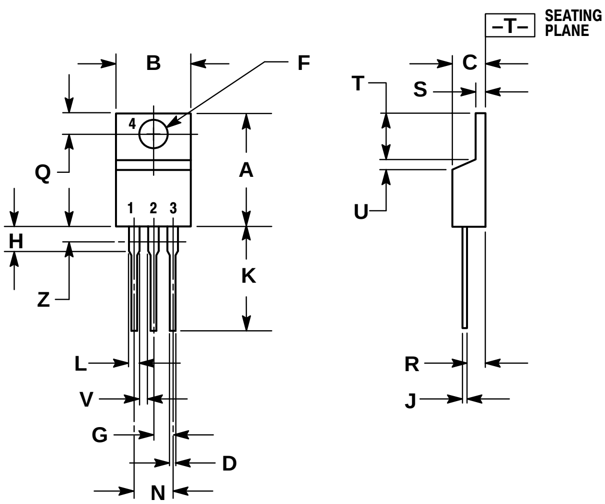


Figure 20. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 125°C)

PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA



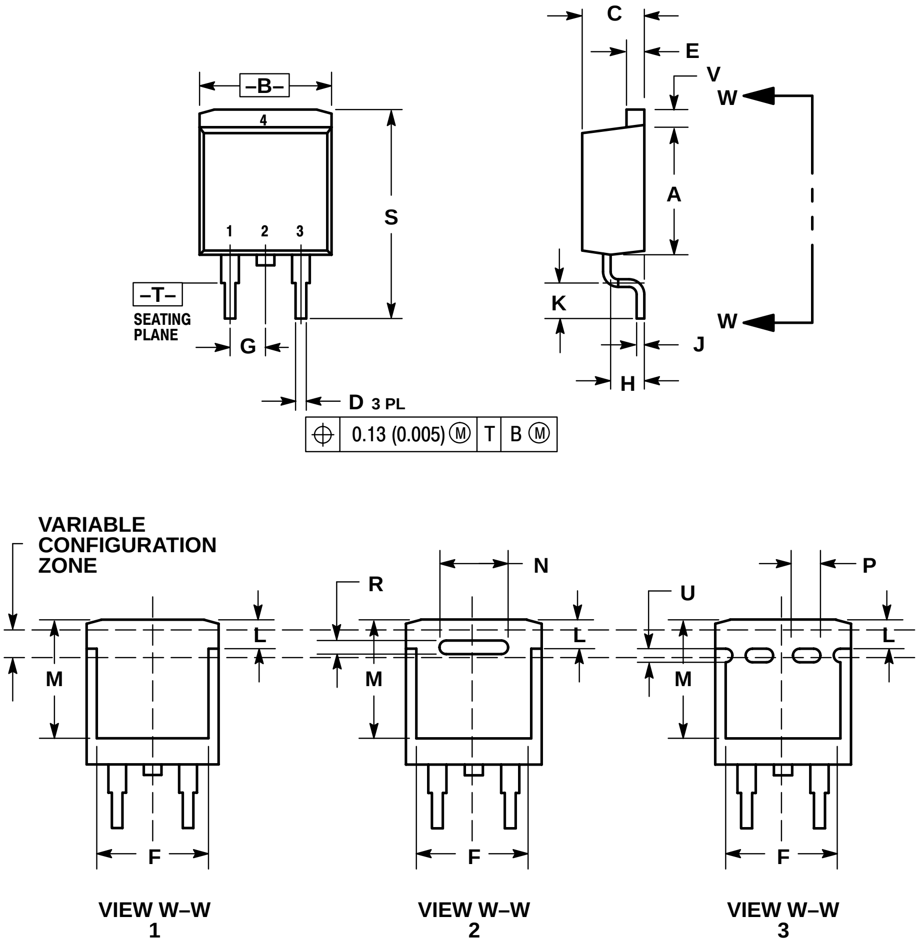
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PACKAGE DIMENSIONS

D2PAK
CASE 418B–04
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Notes

PUBLICATION ORDERING INFORMATION

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