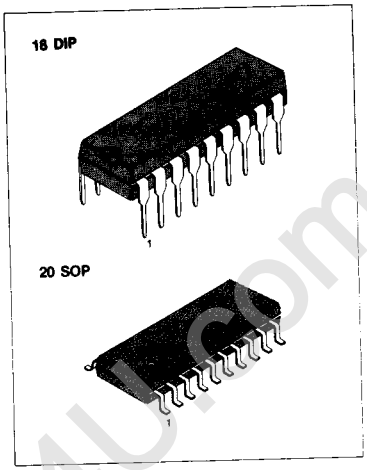
8-CHANNEL SOURCE DRIVERS

These integrated circuits, rated for operation with output voltages of up to 50V and designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic-and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

KA2580A is a high current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

KA2588A is a high-current source driver similar to KA2580A, has separated logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies.

KA2580A is furnished in 18-pin dual in-line plastic package; KA2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.



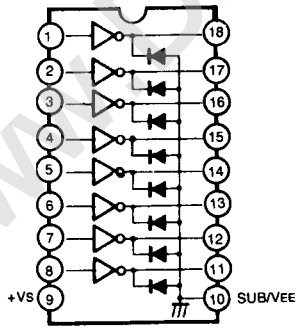
FEATURES

- **TTL, CMOS, PMOS, NMOS Compatible**
- **High Output Current Ratings**
- **Internal Transient Suppression**
- **Efficient Input/Output Pin Structure**

ORDERING INFORMATION

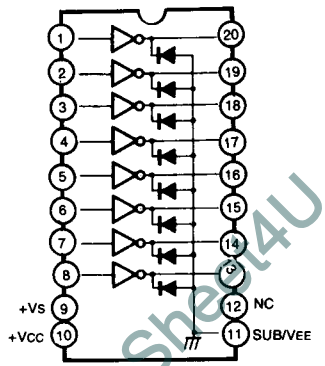
Device	Package	Operating Temperature
KA2580A	18 DIP	– 20 ~ + 85°C
KA2588A	20 DIP	

SCHEMATIC DIAGRAM



KA2580A

Fig. 1



KA2588A

Fig. 2

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Output Voltage	V_O	50	V
Supply Voltage (ref, sub)	V_{CC}	50	V
Supply Voltage (ref, sub, KA2588A)	V_{CC}	50	V
Input Voltage (ref, Vs)	V_I	−30	V
Total Current	$I_{CC}+I_S$	−500	mA
Substrate Current	I_{SUB}	3.0	A
Power Dissipation (single output)	P_D	1.0	W
(total Package)*		2.2	W
Operating Temperature	T_{OPR}	−20 ~ +85	°C
Storage Temperature	T_{STG}	−65 ~ +150	°C

* Derate at the rate of 18mW/°C above 25°C

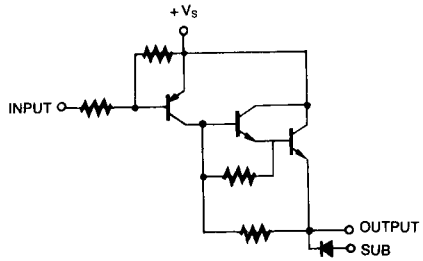
RECOMMANDED OPERATING VOLTAGE (Ta = 25°C)

V_S	V_{IN} (on)	V_{IN} (off)	V_{CC}	V_{EE}(max)	DVC Type
0V	−15V ~ −3.6V	−0.5V ~ 0V	NA	−50V	KA2580A
+5V	0V ~ +1.4V	+4.5V ~ +5V	NA	−45V	KA2580A
			≤5V	−45V	KA2588A
+12V	0V ~ +8.4V	+11.5V ~ +12V	NA	−38V	KA2580A
			≤12V	−38V	KA2588A
+15V	0V ~ +11.4V	+14.5V ~ +15V	NA	−35V	KA2580A
			≤15V	−35V	KA2588A

Notes

1) For simplication, these devices are characterized to the above with specific voltages for inputs, logic supply (V_s), load supply (V_{EE}), and collector supply (V_{CC}).
2) Typical use of the KA2580A is with negative referenced logic. The more common application of the KA2588A is with positive referenced logic supplies.
3) In application, the devices are capable of operation over a wide range of logic and supply voltage levels.
4) The substrate must be tied to the most negative point in the external circuit to maintain isolation drivers and to provide for normal circuit operation.

PARTIAL SCHEMATIC (KA2580A)



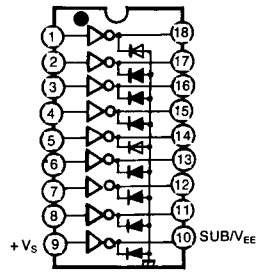


Fig. 3

ELECTRICAL CHARACTERISTICS (KA2580A)

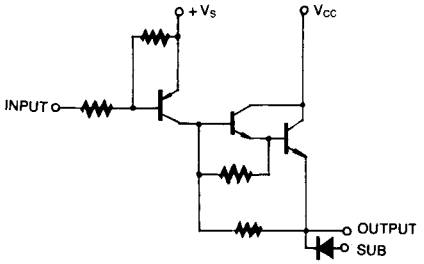
(Ta = 25°C, V_S = 0V, V_{EE} = − 45V unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Input Current	$I_{I\ (ON)}$	V_{IN} = − 3.6V, I_{OUT} = − 350mA		− 500	μA
		V_{IN} = − 15V, I_{OUT} = − 350mA		− 2.1	mA
	$I_{I\ (OFF)}$	I_{OUT} = − 500μA, Ta = 70°C (Note 3)	− 50		μA
Input Voltage (Note 4)	$V_{I\ (ON)}$	I_{OUT} = − 100mA, $V_{CE} \leq$ 1.8V		− 2.4	V
		I_{OUT} = − 225mA, $V_{CE} \leq$ 1.9V		− 3.0	V
		I_{OUT} = − 350mA, $V_{CE} \leq$ 2.0V		− 3.6	V
	$V_{I\ (OFF)}$	I_{OUT} = − 500μA, Ta = 70°C	− 0.2		V
Output Leakage Current	$I_{O\ (LKG)}$	V_{IN} = − 0.5V, V_{OUT} = V_{EE} = − 50V		50	μA
		V_{IN} = − 0.4V, V_{OUT} = V_{EE} = − 50V Ta = 70°C		100	μA
Output Saturation Voltage	$V_{O\ (SAT)}$	V_{IN} = − 2.4V, I_{OUT} = − 100mA		1.8	V
		V_{IN} = − 3.0V, I_{OUT} = − 225mA		1.9	V
		V_{IN} = − 3.6V, I_{OUT} = − 350mA		2.0	V
Output Sustaining Voltage (Note 1, 2)	$V_{O\ (SUS)}$	V_{IN} = − 0.4V, I_{OUT} = − 25mA	35		V
Input Capacitance	C_I			25	pF
Clamp Diode Leakage Current	$I_{LKG\ (CD)}$	V_R = 50V, Ta = 70°C		50	μA
Clamp Diode Forward Voltage	$V_{F\ (CD)}$	If = 350mA		2.0	V
Turn-On Delay	$t_{D\ (ON)}$	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	$t_{D\ (OFF)}$	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp ≤ 300uS, duty cycle ≤ 2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_s.

PARTIAL SCHEMATIC (KA2588A)



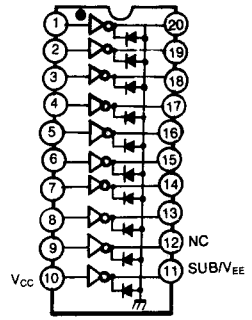


Fig. 4

ELECTRICAL CHARACTERISTICS (KA2588A)

(Ta = 25°C, $V_S = V_{CC} = 5.0V$, $V_{EE} = -40V$, unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
Input Current	$I_{I(ON)}$	$V_{IN} = -1.4V$, $I_{OUT} = -350mA$		−500	μA
		$V_S = 15V$, $V_{EE} = -30V$, $V_{IN} = 0V$, $I_{OUT} = -350mA$		−2.1	mA
	$I_{I(OFF)}$	$I_{OUT} = -500\mu A$, Ta = 70°C (Note 3)	−50		μA
Input Voltage (Note 4)	$V_{I(ON)}$	$I_{OUT} = -100mA$, $V_{CE} \leq 1.8V$		2.6	V
		$I_{OUT} = -225mA$, $V_{CE} \leq 1.9V$		2.0	V
		$I_{OUT} = -350mA$, $V_{CE} \leq 2.0V$		1.4	V
	$V_{I(OFF)}$	$I_{OUT} = -500\mu A$, Ta = 70°C	4.8		V
Output Leakage Current	$I_{O(LKG)}$	$V_{IN} \geq 4.5V$, $V_{OUT} = V_{EE} = -45V$		50	μA
		$V_{IN} \geq 4.6V$, $V_{OUT} = V_{EE} = -45V$ Ta = 70°C		100	μA
Output Saturation Voltage	$V_{O(SAT)}$	$V_{IN} = 2.6V$, $I_{OUT} = -100mA$ Ref. V_{CC}		1.8	V
		$V_{IN} = 2.0V$, $I_{OUT} = -225mA$ Ref. V_{CC}		1.9	V
		$V_{IN} = 1.4V$, $I_{OUT} = -350mA$ Ref. V_{CC}		2.0	V
Output Sustaining Voltage (Note 1, 2)	$V_{O(SUS)}$	$V_{IN} \geq 4.6V$, $I_{OUT} = -25mA$	35		V
Input Capacitance	C_I			25	pF
Clamp Diode Leakage Current	$I_{LKG(CD)}$	$V_R = 50V$, Ta = 70°C		50	μA
Clamp Diode Forward Voltage	$V_{F(CD)}$	If = 350mA		2.0	V
Turn-On Delay	$t_{D(ON)}$	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS
Turn-Off Delay	$t_{D(OFF)}$	0.5 V_{IN} to 0.5 V_{OUT}		5.0	μS

Notes

1) Pulsed test, tp ≤ 300uS, duty cycle ≤ 2%.
2) Negative current is defined as coming out of specified device pin.
3) The Iin (off) current limit guarantees against partial turn-on of the output.
4) The Vin (on) voltage limit guarantees a minimum output source per the specified conditions.
5) The substrate must always be tied to the most negative point and must be at least 4.0V below V_S.
6) V_{CC} must never be more positive than V_S.

APPLICATION CIRCUIT

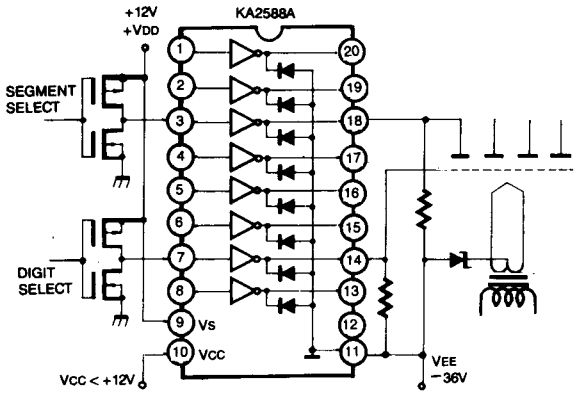


Fig. 5 Vacuum Fluorescent Display Driver (Split Supply)

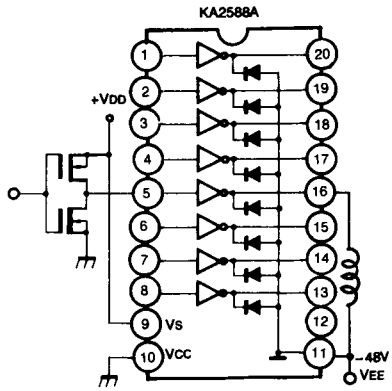


Fig. 6 Telecommunication Relay Driver (Positive Logic)

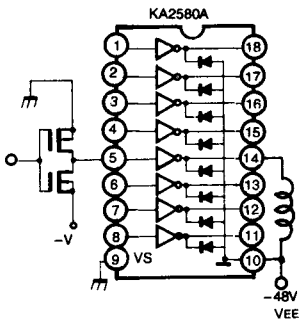


Fig. 7 Telecommunication Relay Driver (Negative Logic)

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