1 PRODUCT OVERVIEW

SAM87RI PRODUCT FAMILY

Samsung's SAM87RI family of 8-bit single-chip CMOS microcontrollers offer fast and efficient CPU, a wide range of integrated peripherals, and supports OTP device.

A dual address/data bus architecture and bit- or nibble-configurable I/O ports provide a flexible programming environment for applications with varied memory and I/O requirements. Timer/counters with selectable operating modes are included to support real-time operations.

KS86C6104/P6104 MICROCONTROLLER

The KS86C6104/P6104 microcontroller with USB function can be used in a wide range of general purpose applications. It is especially suitable for mouse or joystick controller and is available in 20-pin DIP and 24-pin SOP package.

The KS86C6104/P6104 single-chip 8-bit microcontroller is fabricated using an advanced CMOS process. It is built around the powerful SAM87RI CPU core.

Stop and Idle power-down modes were implemented to reduce power consumption. To increase on-chip register space, the size of the internal register file was logically expanded. The KS86C6104/P6104 has 4 Kbytes of program memory on-chip and 208 bytes of RAM including 16 bytes of working register.

Using the SAM87Ri design approach, the following peripherals were integrated with the SAM87Ri core:

— Two configurable I/O ports (11 pins)

— 7 bit-programmable pins for external interrupts

— 8-bit timer/counter with two operating modes

OTP

The KS86C6104 microcontroller is also available in OTP (One Time Programmable) version, KS86P6104. KS86P6104 microcontroller has an on-chip 4-Kbyte one-time-programmable EPROM instead of masked ROM. The KS86P6104 is comparable to KS86C6104, both in function and in pin configuration.

FEATURES

CPU

- SAM87RI CPU core

Memory

- 4-Kbyte internal program memory (ROM)
- 208-byte RAM
- 16 bytes of working register

Instruction Set

- 41 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 1.0 µs at 6 MHz f_{OSC}

Interrupts

- 12 interrupt sources with one vector
- One level, one vector interrupt structure

Oscillation Circuit Options

- 6 MHz crystal/ceramic oscillator
- External clock source

General I/O

- 11 bit-programmable I/O pins

Timer/Counter

- One 8-bit basic timer for watchdog function and programmable oscillation stabilization interval generation function
- One 8-bit timer/counter with Compare/Overflow counter

USB Serial Bus

- Compatible to USB low speed (1.5 Mbps) device 1.0 specification.
- Serial bus interface engine (SIE)
  — Packet decoding/generation
  — CRC generation and checking
  — NRZI encoding/decoding and bit-stuffing
- Two 8-byte receive/transmit USB buffer

Operating Temperature Range

- $-40^{\circ}C$ to $+85^{\circ}C$

Operating Voltage Range

- 4.0 V to 5.25 V

Package Types

- 20-pin DIP
- 24-pin SOP

Comparator

- 4-channel mode, 4-bit resolution
- 3-channel mode, external reference low EMI design

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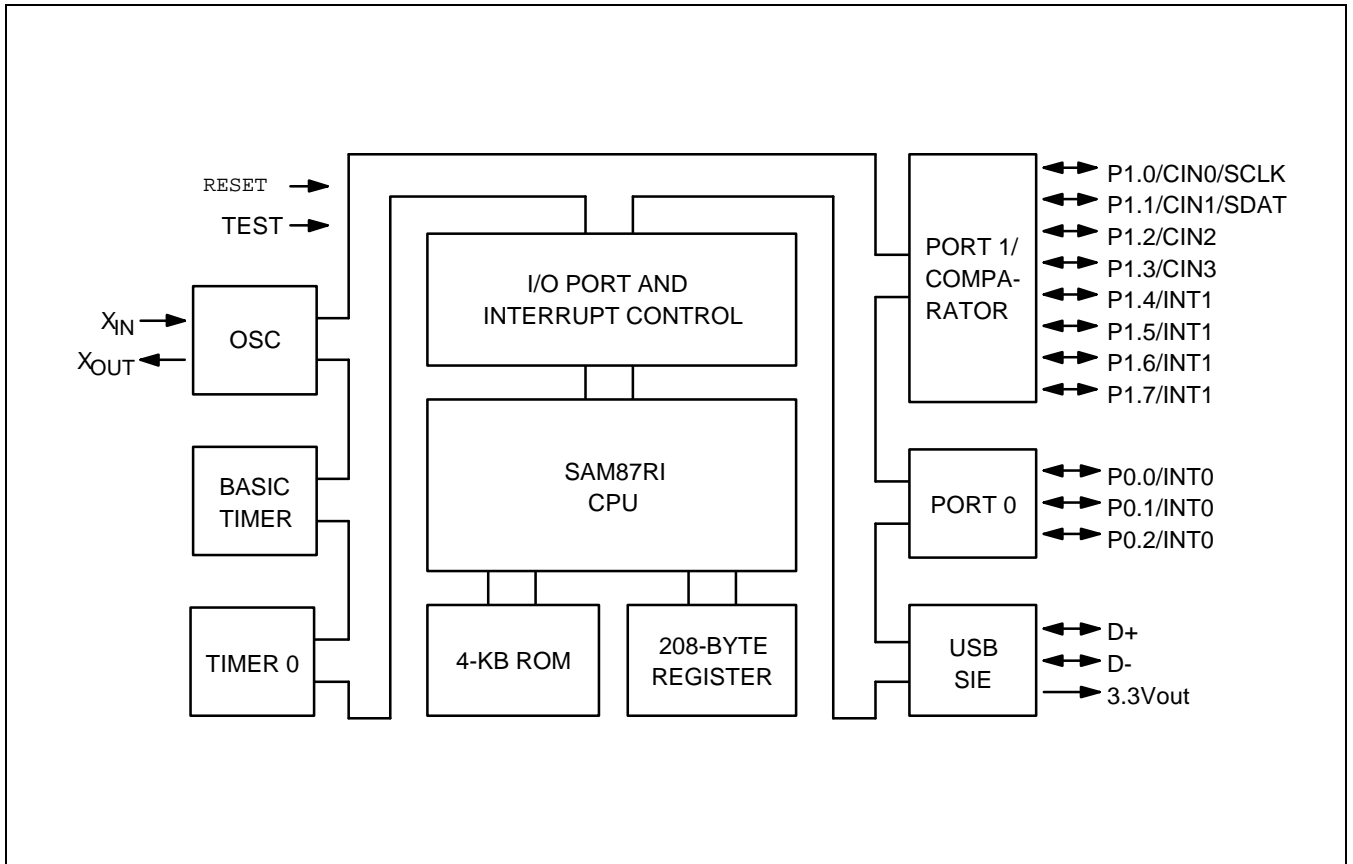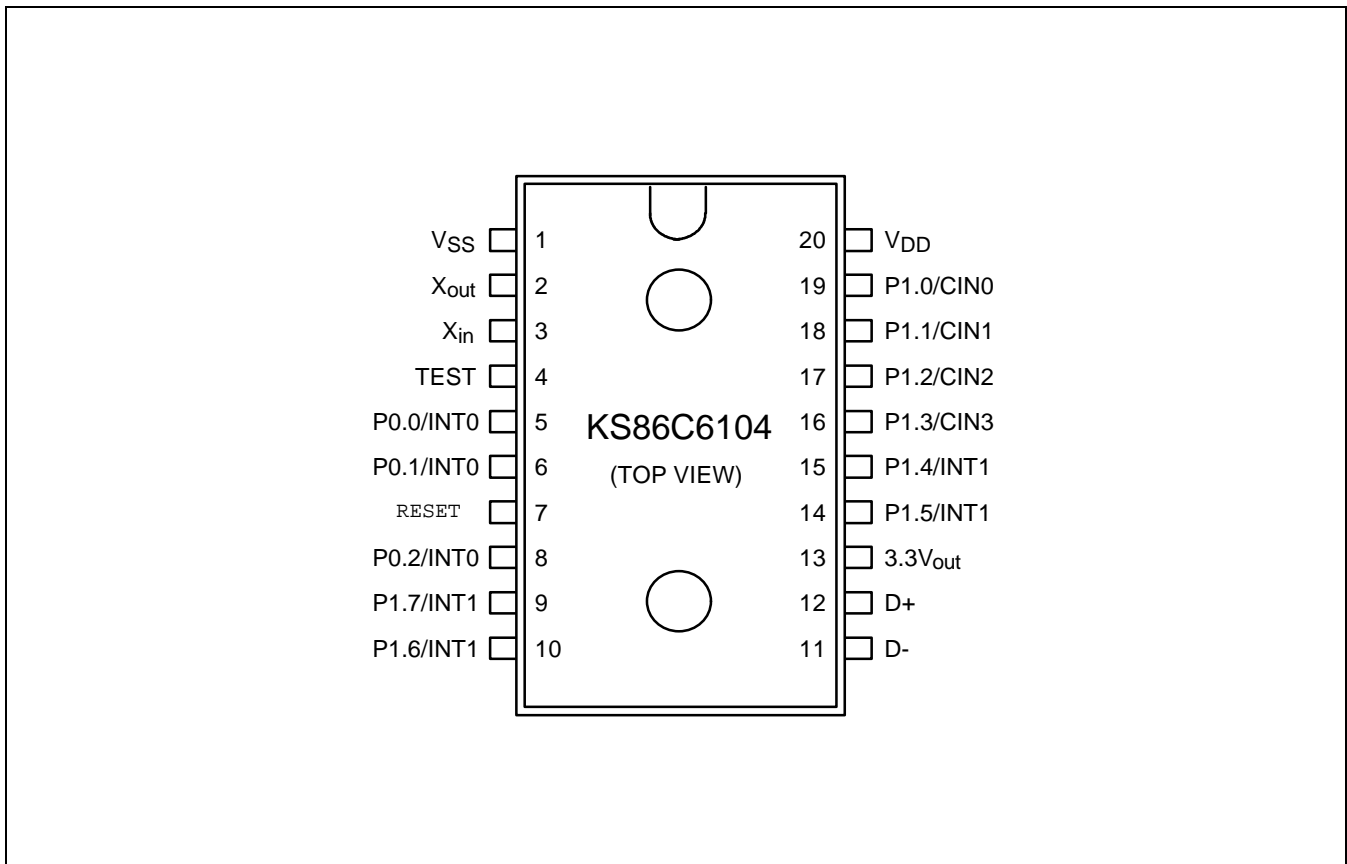**ELECTRONICS**

BLOCK DIAGRAM

Figure 1-1. Block Diagram

PIN ASSIGNMENTS

V_SS	1		20	V_DD
X_out	2		19	P1.0/CIN0
X_in	3		18	P1.1/CIN1
TEST	4		17	P1.2/CIN2
P0.0/INT0	5	KS86C6104	16	P1.3/CIN3
P0.1/INT0	6	(TOP VIEW)	15	P1.4/INT1
RESET	7		14	P1.5/INT1
P0.2/INT0	8		13	3.3V_out
P1.7/INT1	9		12	D+
P1.6/INT1	10		11	D-

Figure 1-2. Pin Assignment Diagram (20-Pin DIP Package)

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```
                  ┌─────────────────────┐
       Vss ▭  1            24  ▭  VDD
      Xout ▭  2            23  ▭  P1.0/CIN0
       Xin ▭  3            22  ▭  P1.1/CIN1
        NC ▭  4            21  ▭  NC
      TEST ▭  5            20  ▭  P1.2/CIN2
  P0.0/INT0 ▭  6    KS86C6104  19  ▭  P1.3/CIN3
  P0.1/INT0 ▭  7   (TOP VIEW)  18  ▭  P1.4/INT1
     RESET ▭  8            17  ▭  P1.5/INT1
        NC ▭  9            16  ▭  NC
  P0.2/INT0 ▭  10           15  ▭  3.3Vout
  P1.7/INT1 ▭  11           14  ▭  D+
  P1.6/INT1 ▭  12           13  ▭  D-
                  └─────────────────────┘
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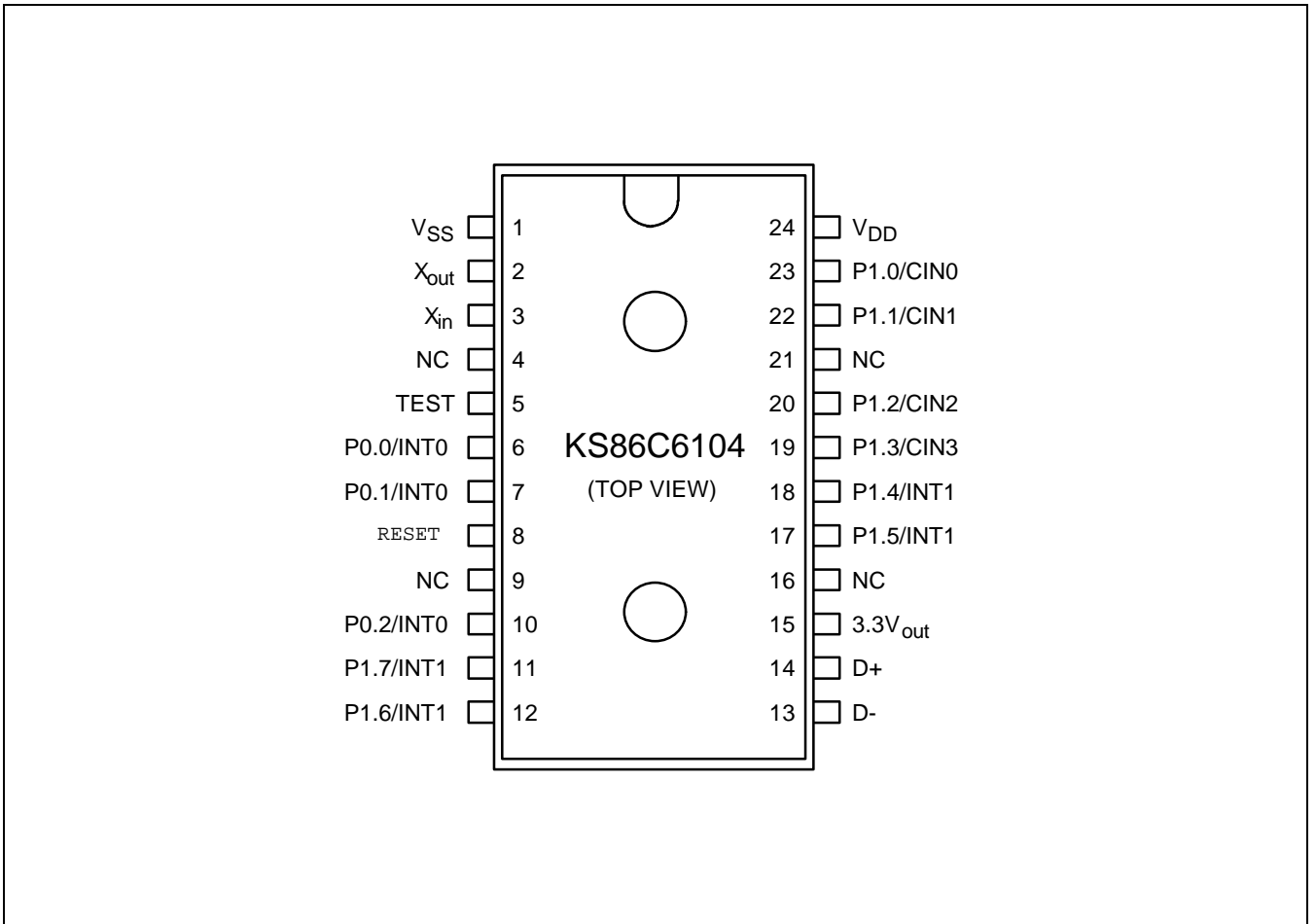
Figure 1-3. Pin Assignment Diagram (24-Pin SOP Package)

PIN DESCRIPTIONS

Table 1-1. KS86C6104/P6104 Pin Descriptions

| Pin Names	Pin Type	Pin Description	Circuit Number	Pin Numbers	Share Pins
P0.0–P0.2	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are individually assignable to input pins by software and are automatically disable for output pins. Port0 can be individually configured as external interrupt inputs.	D	5, 6, 8	INT0
P1.0–P1.3	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are individually assignable to input pins by software. Port1.0–1.3 can be configured as comparator input	F-8	19–16	CIN0–CIN3
P1.4-P1.7	I/O	Bit-programmable I/O port for Schmitt trigger input or push-pull output. Pull-up resistors are individually assignable to input pins by software and are automatically disabled for output pins. Port1.4–1.7 can be individually configured as external interrupt inputs.	D	15, 14, 10, 9	INT1
D+/D-	I/O	Only used as USB tranceive/receive port.	–	12–11	–
3.3VOUT	O	Internal regulator 3.3 V output pin for referencing the voltage	–	13	–
X_{IN}, X_{OUT}	–	System clock input and output pin (crystal/ceramic oscillator, or external clock source)	–	3–2	–
INT0	I	External interrupt for bit-programmable port0.	D	5, 6, 8	Port0
INT1	I	External interrupt for bit-programmable port1	D	9, 10, 14, 15	Port1
RESET	I	RESET signal input pin.	–	7	–
TEST	I	Test signal input pin (for factory use only; must be connected to V_{SS})	–	4	–
V_{DD}	–	Power input pin	–	20	–
V_{SS}	–	V_{SS} is a ground power for CPU core.	–	1	–

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PIN CIRCUITS

Table 1-2. Pin Circuit Assignments for the KS86C6104/P6104

Circuit Number	Circuit Type	KS86C6104/P6104 Assignments
C	O	
D	I/O	Port0, Port1.4–1.7, INT0, INT1
F-8	I/O	Port1.0–1.3

NOTE: Diagrams of circuit types C–D, and F-8 are presented below.
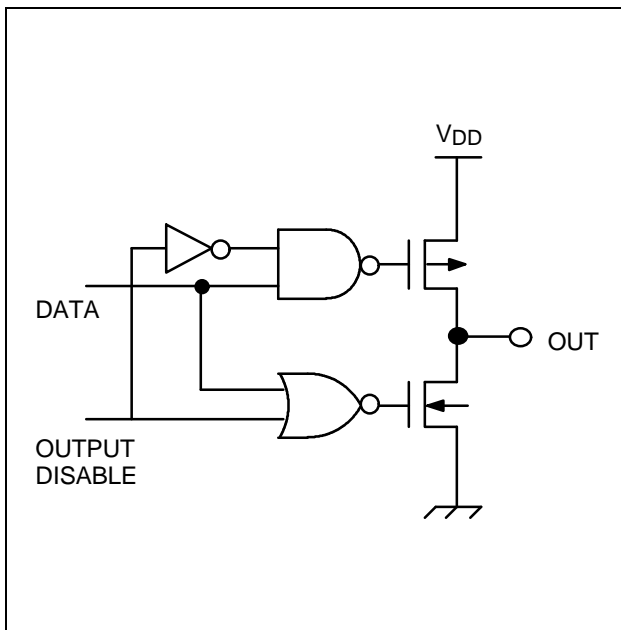
Figure 1-4. Pin Circuit Type C
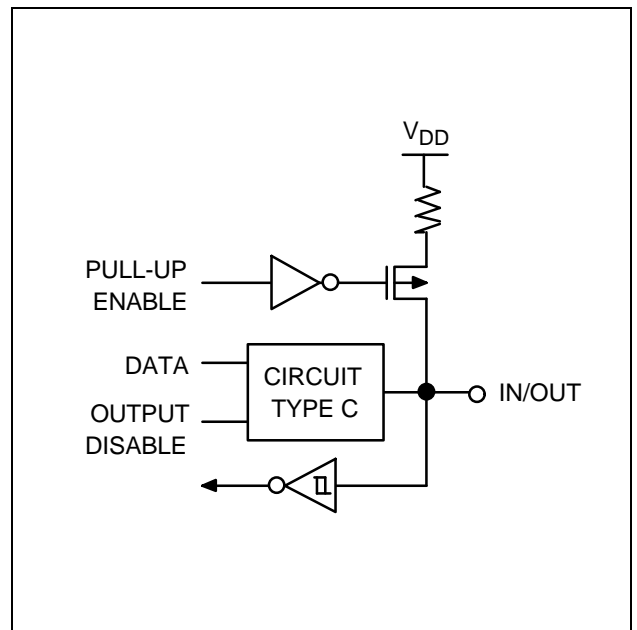
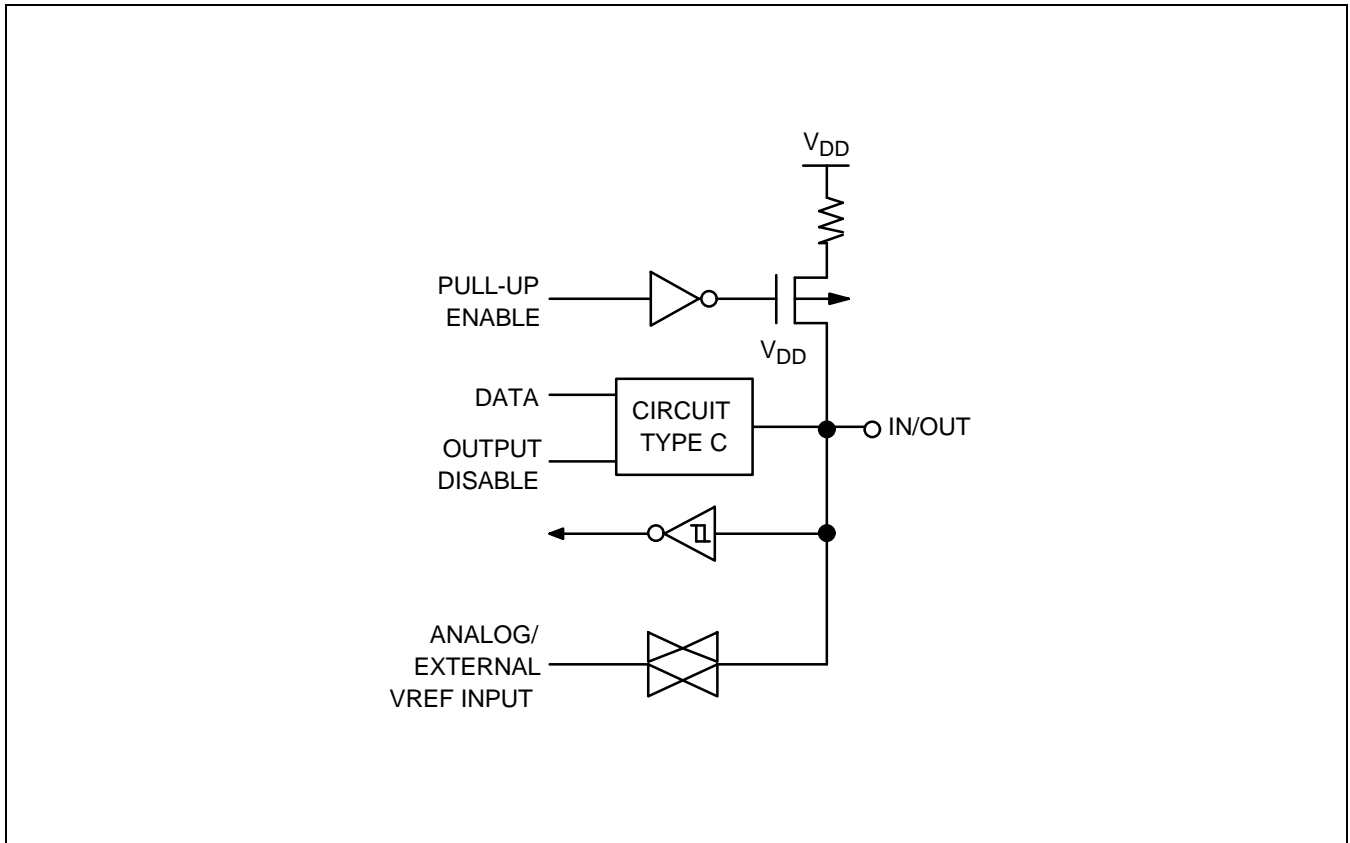

Figure 1-5. Pin Circuit Type D
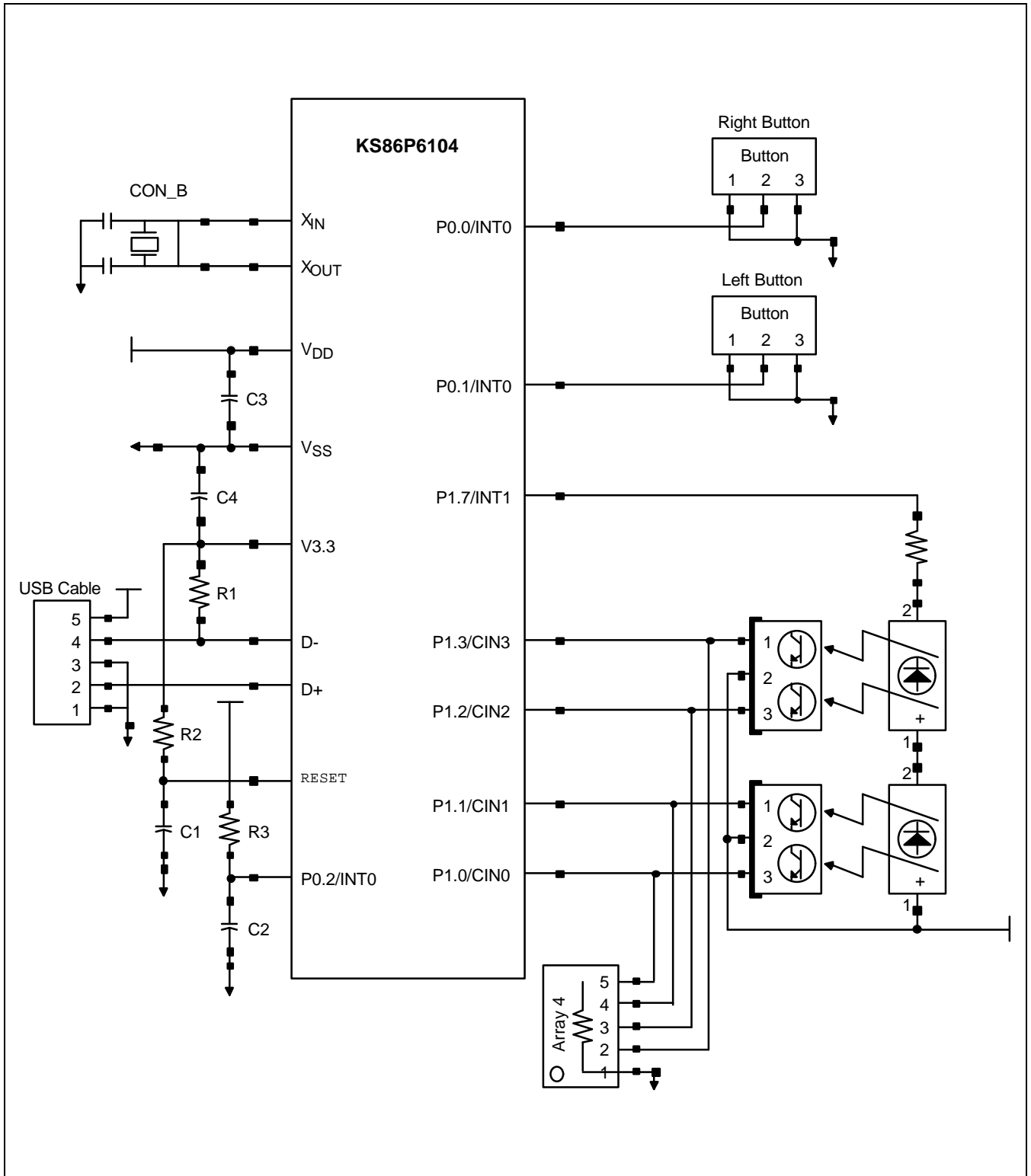
Figure 1-6. Pin Circuit Type F-8

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Figure 1-7. USB Mouse Circuit Diagram

NOTES

13 ELECTRICAL DATA

OVERVIEW

In this section, the following KS86C6104/P6104 electrical characteristics are presented in tables and graphs:

— Absolute maximum ratings
— D.C. electrical characteristics
— I/O capacitance
— A.C. electrical characteristics
— Input timing for RESET
— Oscillator characteristics
— Operating voltage range
— Oscillation stabilization time
— Clock timing measurement points at X_{IN}
— Data retention supply voltage in Stop mode
— Stop mode release timing when initiated by a RESET
— Stop mode release timing when initiated by an external interrupt
— Characteristic curves
— Comparator Electrical Characteristics

Table 13-1. Absolute Maximum Ratings

($T_A =$ 25$°$C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	$-$ 0.3 to $+$ 6.5	V
Input voltage	V_{IN}	All in ports	$-$ 0.3 to V_{DD} + 0.3	V
Output voltage	V_O	All output ports	$-$ 0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	One I/O pin active	$-$ 18	mA
		All I/O pins active	$-$ 60	
Output current low	I_{OL}	One I/O pin active	$+$ 30	mA
		Total pin current for ports 0, 1	$+$ 100	
Operating temperature	T_A	–	$-$ 40 to +85	$°$C
Storage temperature	T_{STG}	–	$-$ 65 to $+$ 150	$°$C

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Table 13-2. D.C. Electrical Characteristics

$(T_A = -40°C$ to $+85°C, V_{DD} = 4.0$ V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input highvoltage	V_{IH1}	All input pins except V_{IH2}, D+, D–	$0.8 V_{DD}$	–	V_{DD}	V
	V_{IH2}	X_{IN}	$V_{DD} - 0.5$		V_{DD}	
Input low voltage	V_{IL1}	All input pins except V_{IL2}, D+, D–	–	–	$0.2 V_{DD}$	V
	V_{IL2}	X_{IN}	–	–	0.4	
Output high voltage	V_{OH}	$V_{DD} = 4.5$ V – 5.5 V $I_{OH} = -200$ µA All output ports except D+, D–	$V_{DD} - 1.0$	–	–	V
Output low voltage	V_{OL}	$V_{DD} = 4.5$ V – 5.5 V $I_{OL} = 2$ mA All output ports except D+, D–	–	–	0.4	V
Input high leakage current	I_{LIH1}	$V_{IN} = V_{DD}$ All inputs except I_{LIH2} except D+, D–	–	–	3	µA
	I_{LIH2}	$V_{IN} = V_{DD}$ X_{IN}, X_{OUT}	–	–	20	
Input low leakage current	I_{LIL1}	$V_{IN} = 0$ V All inputs except I_{LIL2} except D+, D–	–	–	– 3	µA
	I_{LIL2}	$V_{IN} = 0$ V X_{OUT}, X_{IN}	–	–	– 20	
Output high leakage current	I_{LOH}	$V_{OUT} = V_{DD}$ All output pins except D+, D–	–	–	3	µA
Output low leakage current	I_{LOL}	$V_{OUT} = 0$ V All output pins except D+, D–	–	–	– 3	µA
Pull-up resistors	R_{L1}	$V_{IN} = 0$ V; $V_{DD} = 5.0$ V,	25	50	100	KΩ
	R_{L2}	$V_{IN} = 0$ V; $V_{DD} = 5.0$ V, RESET only	100	220	400	
Supply current (note)	I_{DD1}	Normal operation mode 6-MHz CPU clock	–	6.5	15	mA
	I_{DD2}	Idle mode; 6-MHz CPU clock	–	4	8	mA
	I_{DD3}	Stop mode; oscillator stop	–	150	300	µA

NOTES:
1. Supply current does not include current drawn through internal pull-up resistors or external output current load.
2. This parameter is guaranteed, but not tested (include D+, D–).
3. Only in 4.2 V to 5.25 V, D+ and D– satisfy the USB spec 1.0.

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Table 13-3. Input/Output Capacitance

$(T_A = -40^\circ C$ to $+85^\circ C$, $V_{DD} = 0$ V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	f = 1 MHz; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/o capacitance	C_{IO}					

Table 13-4. A.C. Electrical Characteristics

$(T_A = -40^\circ C$ to $+85^\circ C$, $V_{DD} = 4.0$ V to 5.25 V)

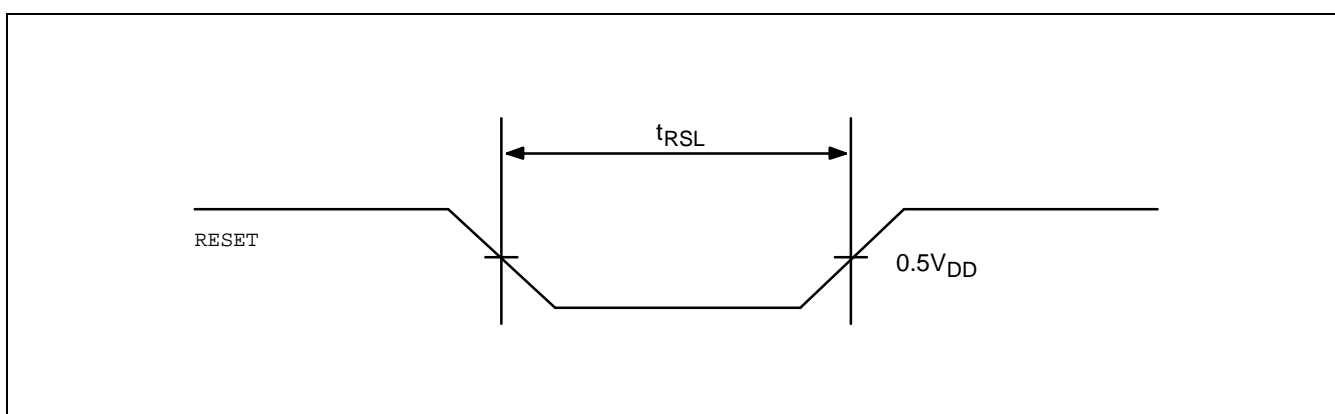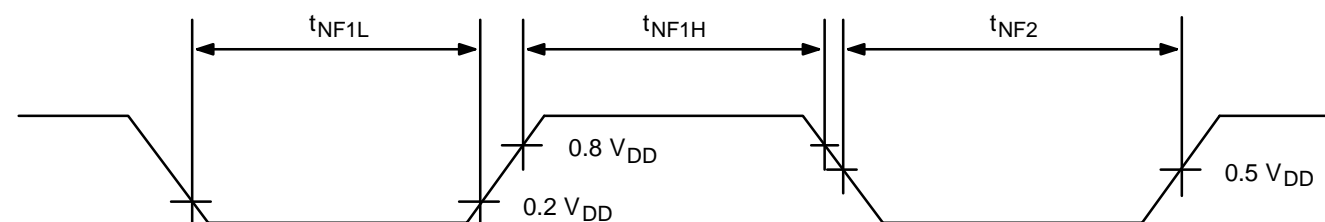| Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise filter	t_{NF1H}, t_{NF1L}	P1 (RC delay)	100	–	200	ns
	t_{NF2}	RESET only (RC delay)	–	800	–	
RESET input low width	t_{RSL}	Input	10	–	–	µs

Figure 13-1. Input Timing for RESET

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Table 13-5. Oscillator Characteristics

$(T_A = -40^{\circ}C + 85^{\circ}C)$
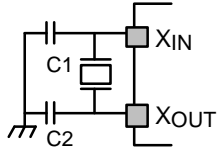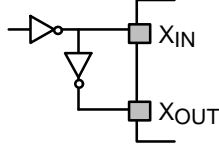
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal Main ceramic (f_{OSC})		Oscillation frequency $V_{DD} = 4.0 V - 5.25 V$	–	6.0	–	MHz
External clock		Oscillation frequency $V_{DD} = 4.0 V - 5.25 V$	–	6.0	–	

Table 13-6. Oscillation Stabilization Time

$(T_A = -40^{\circ}C + 85^{\circ}C, V_{DD} = 4.0 V \text{ to } 5.25 V)$

Oscillator	Test Condition	Min	Typ	Max	Unit
Main crystal	$V_{DD} = 4.5 V$ to $5.5 V$, $f_{OSC} > 6.0$ MHz	–	–	10	ms
Main ceramic	(Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.)				
Oscillator stabilization wait time	t_{WAIT} stop mode release time by a reset	–	$2^{16}/f_{OSC}$	–	
	t_{WAIT} stop mode release time by an interrupt	–	–	–	

NOTE: The oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt, is determined by the setting in the basic timer control register, BTCON.
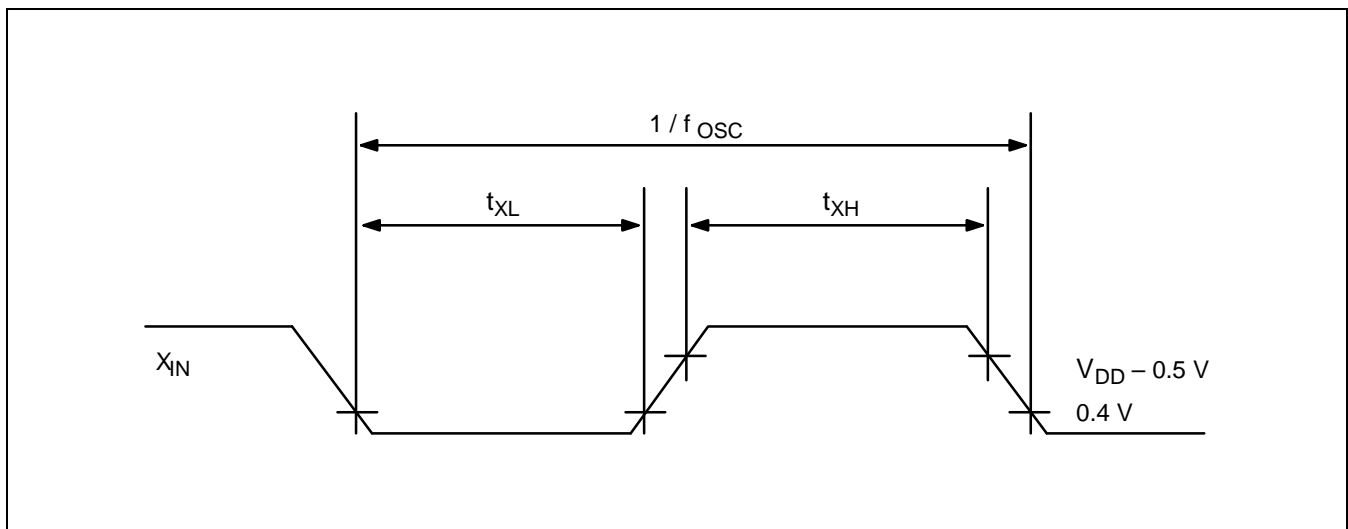
Figure 13-2. Clock Timing Measurement Points at X$_{IN}$

Table 13-7. Data Retention Supply Voltage in Stop Mode

(T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V$_{DDDR}$	Stop mode	2.0	–	6	V
Data retention supply current	I$_{DDDR}$	Stop mode; V$_{DDDR}$ = 2.0 V	–	–	5	µA

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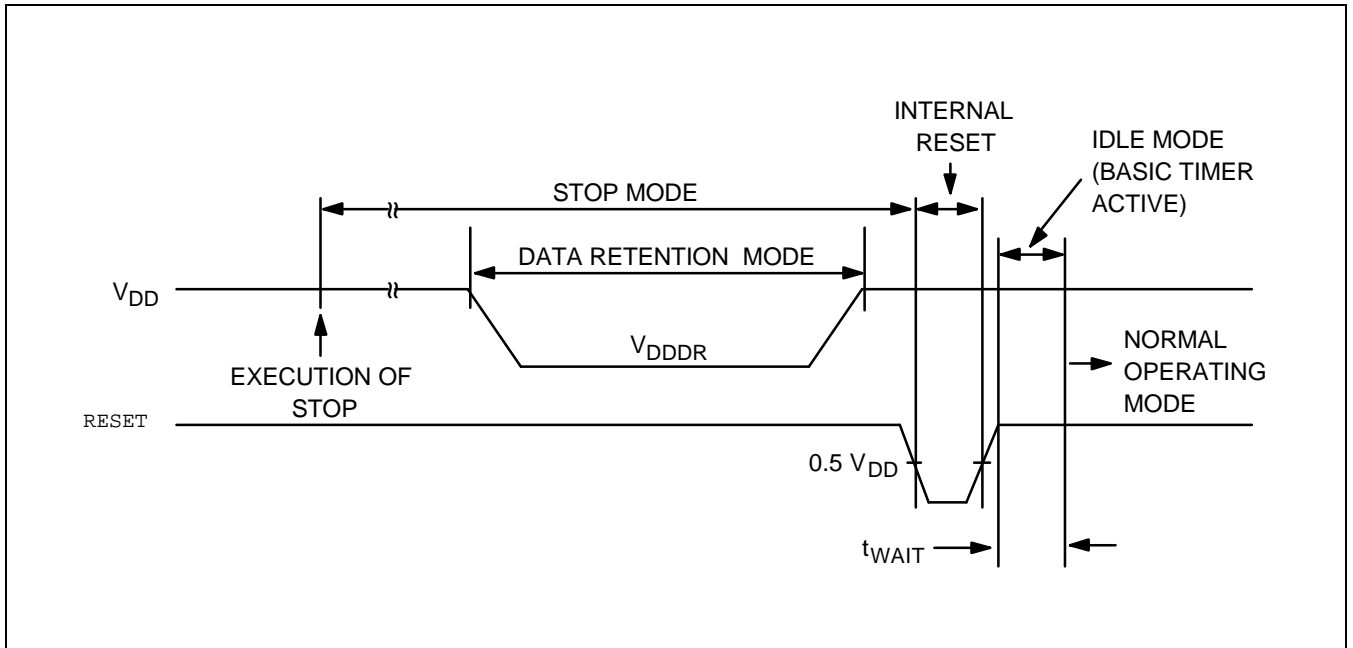
Figure 13-3. Stop Mode Release Timing When Initiated by a RESET
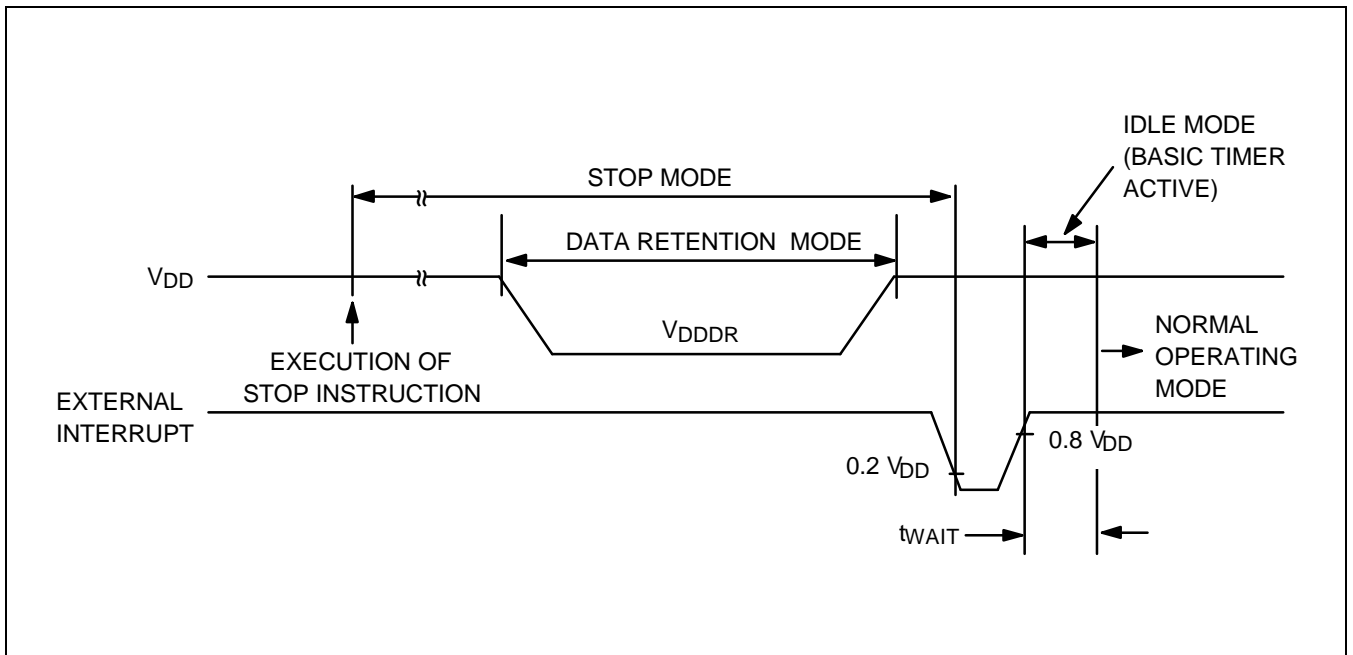
Figure 13-4. Stop Mode Release Timing When Initiated by an External Interrupt

Table 13-8. Comparator Electrical Characteristics

$(T_A = -40^{\circ}C$ to $+85^{\circ}C, V_{DD} = 4.0$ V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Conversion time [1]	tCON	–	–	4×2^4 or 4×2^7	–	F_{CPU}
Comparator input voltage	V_{ICN}	–	V_{SS}	–	V_{DD}	V
Comparator input impedance	R_{CN}	–	2	1000	–	$M\Omega$
Comparator reference voltage	V_{REF}	–	1.8	–	V_{DD}	V
Comparator input current	I_{CIN}	$V_{DD} = 5$ V	-3	–	3	μA
Reference input current	I_{REF}	$V_{DD} = 5$ V	-3	–	3	μA
Comparator block current [2]	I_{COM}	$V_{DD} = 5.5$ V	–	1	2	mA
		$V_{DD} = 4.5$ V		0.5	1	mA
		$V_{DD} = 5$ V (when power down mode)		100	500	nA

NOTES:
1. Conversion time is the time required from the moment a conversion operation starts until it ends.
2. I_{COM} is an operating current during conversion.

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Table 13-9. Low Speed Source Electrical Characteristics (USB)

(T_A = − 40°C to + 85°C, Voltage Regulator Output V_{33out} = 2.8 V to 3.5 V, typ 3,3 V)

Parameter	Symbol	Conditions	Min	Max	Unit
Transition Time: Rise Time	Tr	CL = 50 pF	75	–	ns
		CL = 350 pF	–	300	
Fall Time	Tf	CL = 50 pF	75	–	
		CL = 350 pF	–	300	
Rise/Fall Time Matching	Trfm	(Tr/Tf) CL = 50 pF	70	130	%
Output Signal Crossover Voltage	Vcrs	CL = 50 pF	1.3	2.0	V
Voltage Regulator Output Voltage	V33OUT	with V33OUT to GND 0.1 μF capacitor	2.8	3.5	V

R1 = 15 K Ω   DM: S/W ON
R2 = 1.5 K Ω   DP: S/W OFF
CL = 50pF-350pF
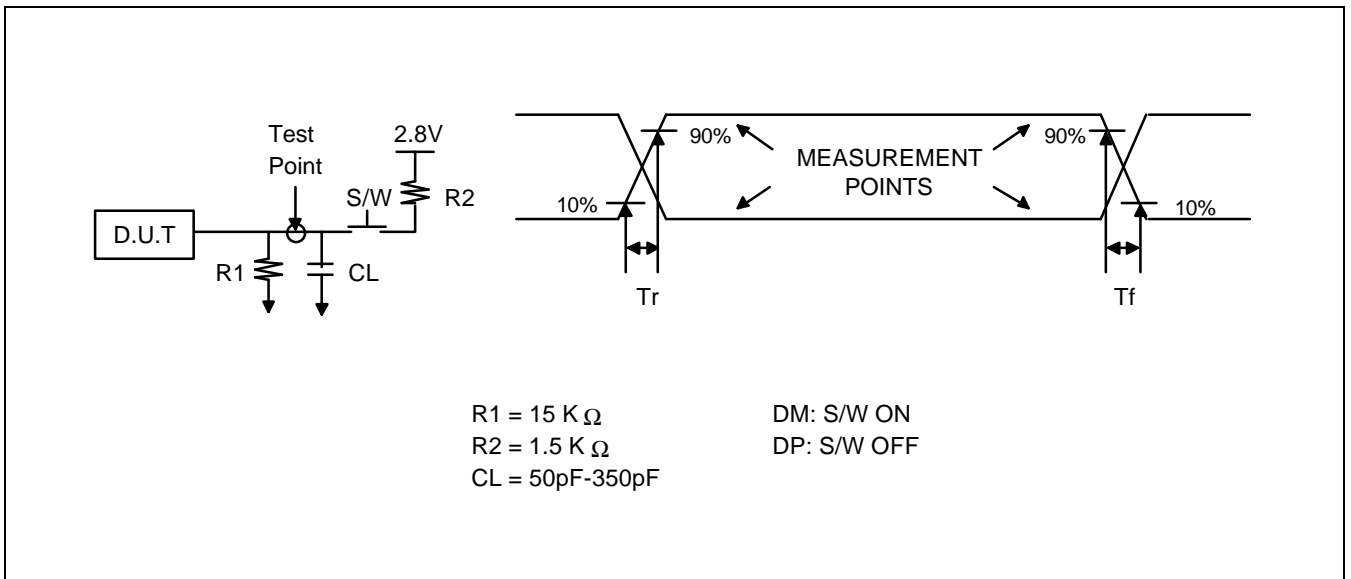
Figure 13-5. USB Data Signal Rise and Fall Time
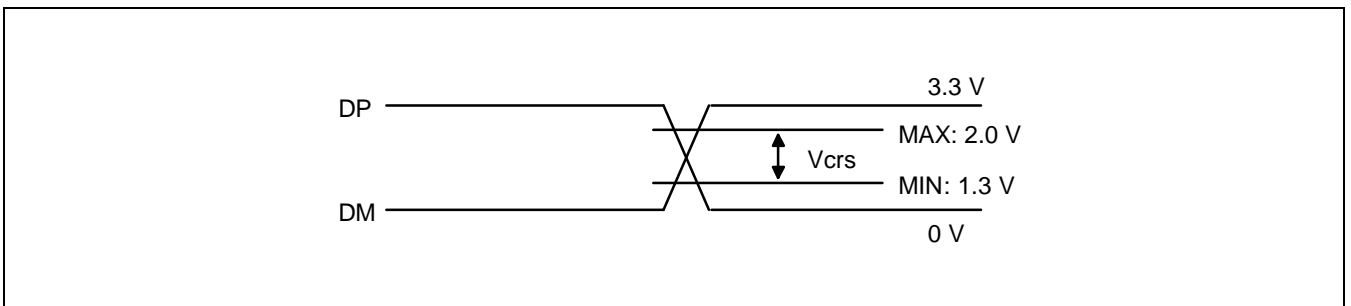
Figure 13-6. USB Output Signal Crossover Point Voltage

NOTES

14 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters

— Pad diagram
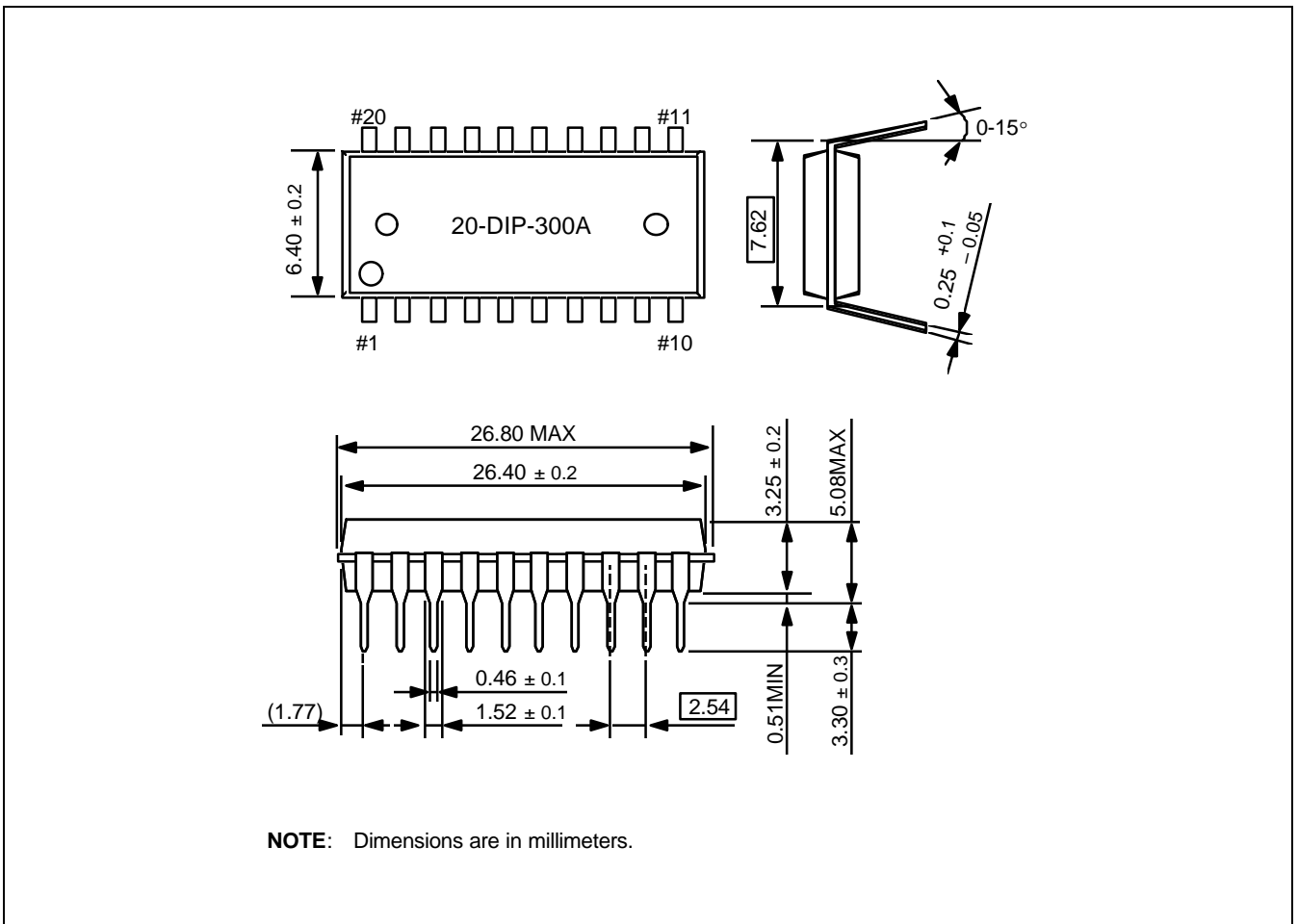
Figure 14-1. 20-DIP0300A Package Dimensions
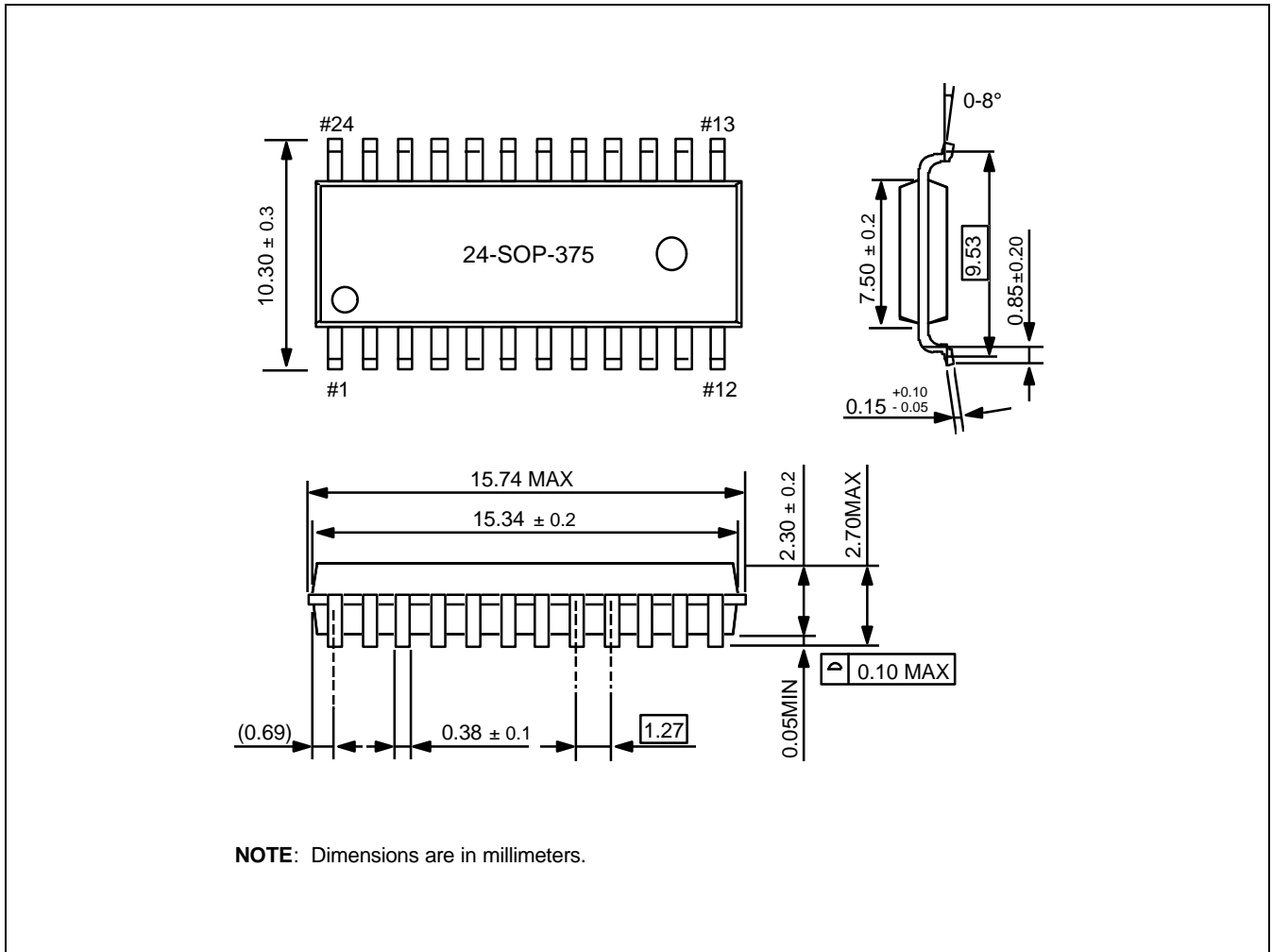
Figure 14-2. 24-SOP-375 Package Dimensions

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15

KS86P6104 OTP

OVERVIEW

The KS86P6104 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the KS86C6104 microcontroller. It has an on-chip OTP ROM instead of masked ROM. The EPROM is accessed by serial data format.

The KS86P6104 is fully compatible with the KS86C6104, both in function and in pin configuration. Because of its simple programming requirements, the KS86P6104 is ideal for use as an evaluation chip for the KS86C6104.

V_{SS}/V_{SS}	1		20	V_{DD}/V_{DD}
X_{out}	2		19	P1.0/CIN0/SCLK
X_{in}	3		18	P1.1/CIN1/SDAT
TEST/TEST	4		17	P1.2/CIN2
P0.0/INT0	5	KS86P6104	16	P1.3/CIN3
P0.1/INT0	6	(TOP VIEW)	15	P1.4/INT1
RESET /RESET	7		14	P1.5/INT1
P0.2/INT0	8		13	3.3V_{out}
P1.7/INT1	9		12	D+
P1.6/INT1	10		11	D-
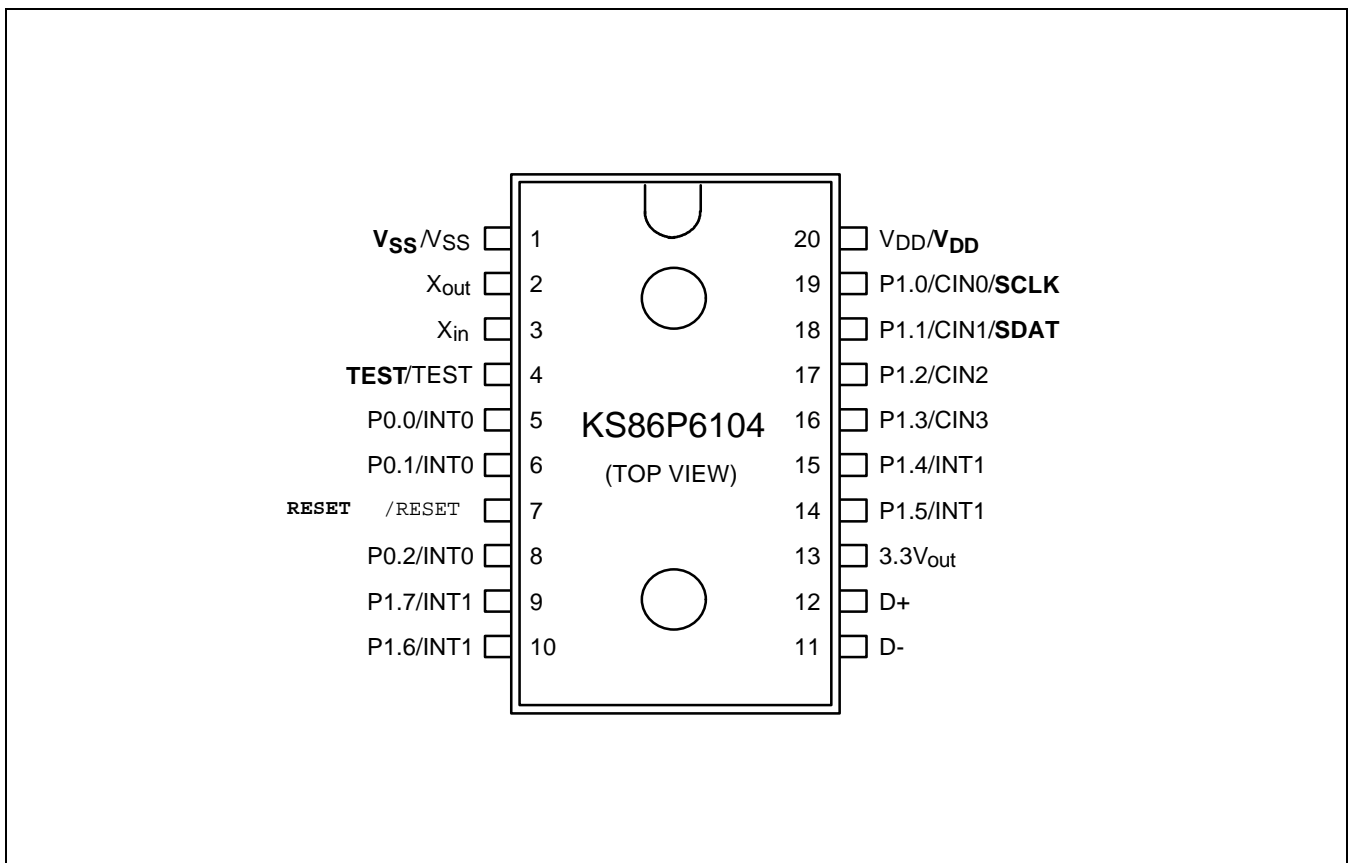
Figure 15-1. KS86P6104 Pin Assignments (20-DIP Package)
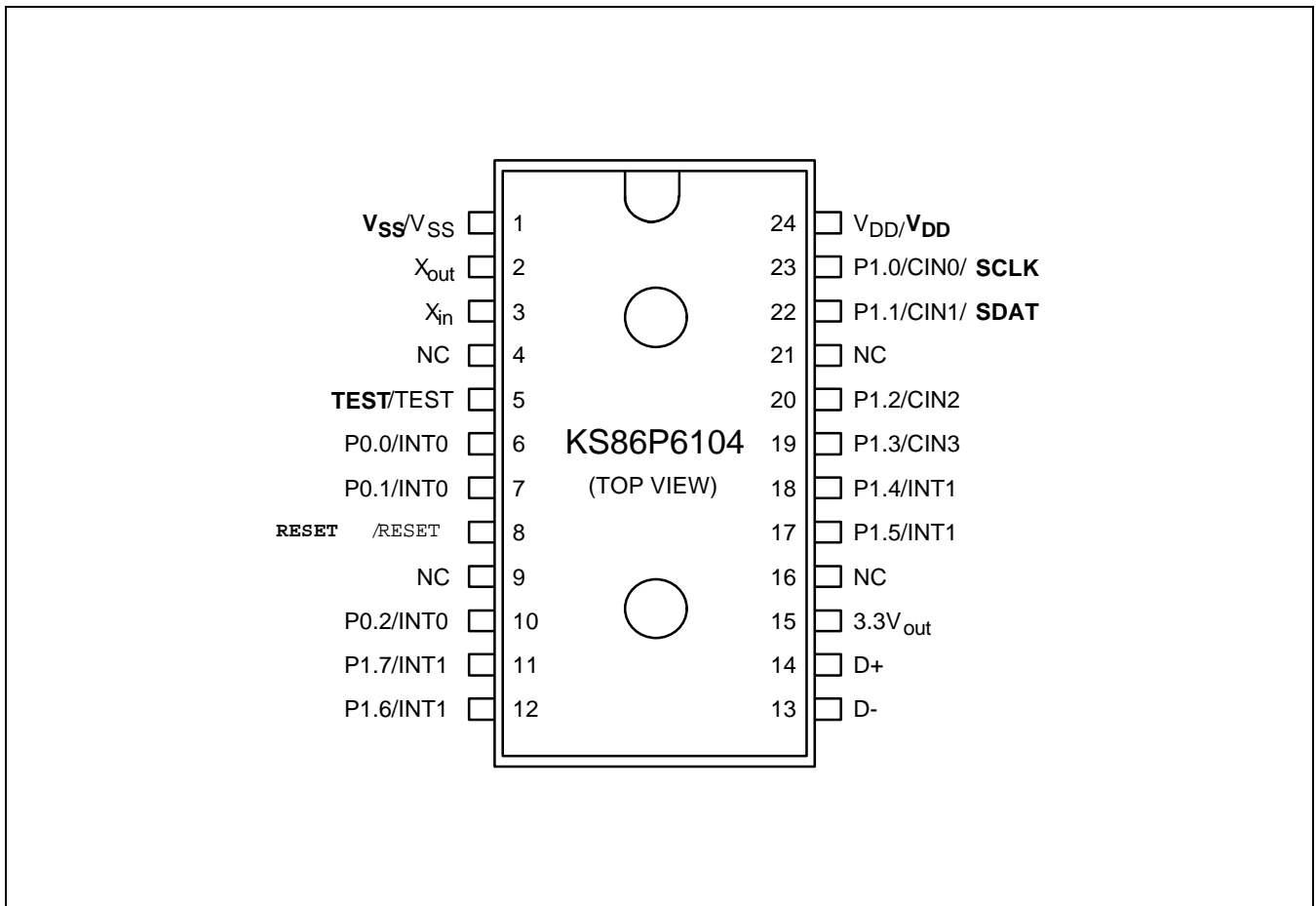
Figure 15-2. KS86P6104 Pin Assignments (24-SOP Package)

Table 15-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No. (20 DIP)	I/O	Function
P1.0 (Pin 18)	SDAT	18	I/O	Serial Data Pin (Output when reading, Input when writing) Input and Push-pull Output Port can be assigned
P1.1 (Pin 19)	SCLK	19	I/O	Serial Clock Pin (Input Only Pin)
TEST	V_{PP} (TEST)	4	I	0V : OTP write and test mode 5V : Operating mode
RESET	RESET	7	I	Chip Initialization and EPROM Cell Writing Power Supply Pin (Indicates OTP Mode Entering) When writing 12.5V is applied and when reading.
V_{DD}/V_{SS}	V_{DD}/V_{SS}	20/1	I	Logic Power Supply Pin.

Table 15-2. Comparison of KS86P6104 and KS86C6104 Features

Characteristic	KS86P6104	KS86C6104
Program Memory	4 K byte EPROM	4 K byte mask ROM
Operating Voltage (V_{DD})	4.0 V to 5.25 V	4.0 V to 5.25 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (RESET)=12.5V	
Pin Configuration	20 DIP/24 SOP	20 DIP/24 SOP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V$_{PP}$ (RESET) pin of the KS86P6104, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 14-3 below.

Table 15-3. Operating Mode Selection Criteria

V$_{DD}$	V$_{PP}$ (RESET)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

Table 15-4. D.C. Electrical Characteristics

(T_A = − 40°C to + 85°C, V$_{DD}$ = 4.0 V to 5.25 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Current (note)	I$_{DD1}$	Normal mode; 6 MHz CPU clock	–	6.5	15	mA
	I$_{DD2}$	Idle mode; 6 MHz CPU clock		4	8	
	I$_{DD3}$	Stop mode; oscillator stop		150	300	μA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.

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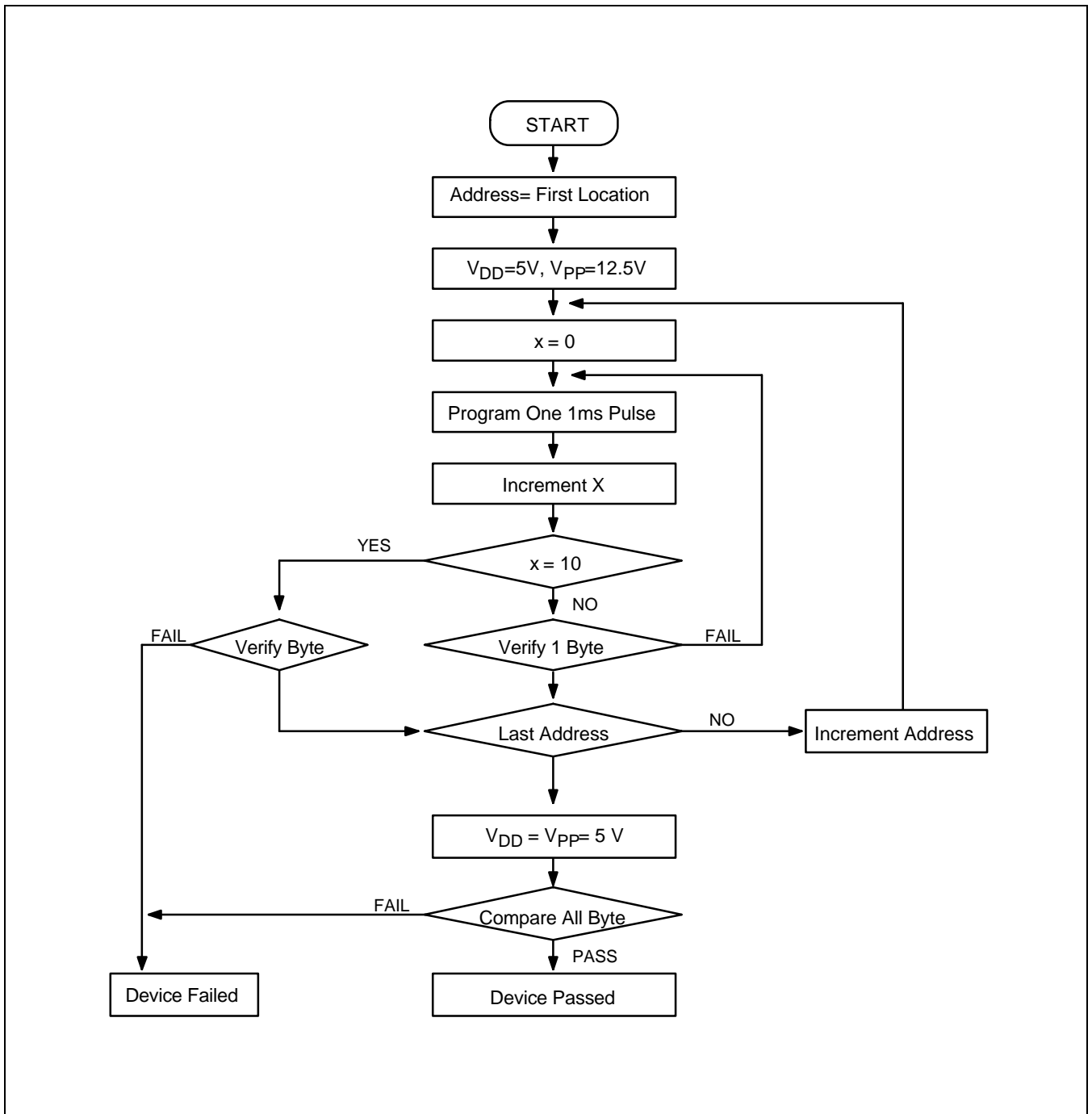ELECTRONICS

```
                              ┌─────────────┐
                              │    START    │
                              └─────────────┘
                                     │
                                     ▼
                        ┌──────────────────────────┐
                        │  Address= First Location  │
                        └──────────────────────────┘
                                     │
                                     ▼
                        ┌──────────────────────────┐
                        │  V_DD=5V, V_PP=12.5V      │
                        └──────────────────────────┘
                                     │                          ◄─────────────┐
                                     ▼                                        │
                        ┌──────────────────────────┐                         │
                        │          x = 0            │                         │
                        └──────────────────────────┘                         │
                                     │                   ◄────────────┐       │
                                     ▼                                │       │
                        ┌──────────────────────────┐                 │       │
                        │    Program One 1ms Pulse  │                 │       │
                        └──────────────────────────┘                 │       │
                                     │                                │       │
                                     ▼                                │       │
                        ┌──────────────────────────┐                 │       │
                        │        Increment X        │                 │       │
                        └──────────────────────────┘                 │       │
                   YES               │                                │       │
         ┌─────────────────◄    < x = 10 >                            │       │
         │                          │ NO                             │       │
         ▼                          ▼                                │       │
   < Verify Byte >          < Verify 1 Byte >  ── FAIL ──────────────┘       │
    FAIL   │                        │                                        │
      │    └────────────►   < Last Address >  ── NO ──►  ┌──────────────────┐│
      │                            │                     │ Increment Address ┘
      │                            ▼
      │                  ┌──────────────────────┐
      │                  │   V_DD = V_PP= 5 V    │
      │                  └──────────────────────┘
      │                            │
      │          FAIL              ▼
      │    ◄──────────── < Compare All Byte >
      │                            │ PASS
      ▼                            ▼
 ┌───────────────┐        ┌──────────────────┐
 │ Device Failed │        │  Device Passed   │
 └───────────────┘        └──────────────────┘
```

Figure 15-3. OTP Programming Algorithm

NOTES