MOTOROLA

# MC13280AY
# MC13281A/B

*Advance Information*

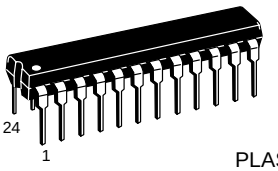
# 80/100 MHz Video Processor

**80/100 MHz VIDEO PROCESSOR**

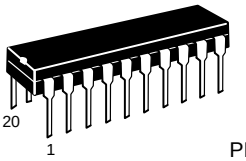
The MC13280AY and MC13281A/B are three channel wideband amplifiers designed for use as a video pre–amplifier in high resolution RGB color monitors.

**Features:**

- 4.0 Vpp Output Swing
- 3.5 ns Rise/Fall Time, 100 MHz Bandwidth (MC13281A/B)
- 4.3 ns Rise/Fall Time, 80 MHz Bandwidth (MC13280AY)
- Subcontrast Controls for Each Channel
- Main Contrast Control
- Blanking and Clamping Inputs
- Packages: NDIP–24 and NDIP–20
- A Single PC Board Pattern Can Accept the MC13281A and the MC13282A (Video Amplifier with OSD)




**P SUFFIX**
PLASTIC PACKAGE
CASE 724




**P SUFFIX**
PLASTIC PACKAGE
CASE 738

**ORDERING INFORMATION**

| Device | Operating Temperature Range | Package |
|---|---|---|
| MC13280AYP | $T_A$ = 0° to +70°C | Plastic DIP |
| MC13281AP | | Plastic DIP |
| MC13281BP | | Plastic DIP |

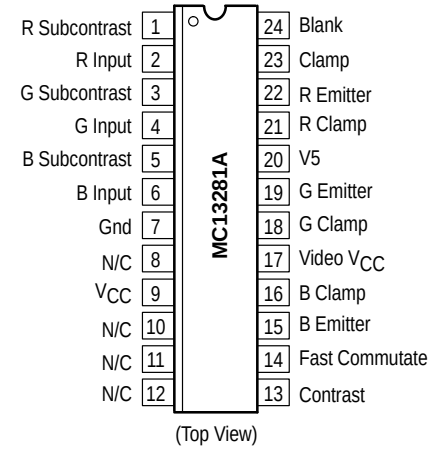
**ABSOLUTE MAXIMUM RATINGS**

| Rating | Pin | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$<br>Video $V_{CC}$ | –0.5, 10<br>–0.5, 10 | Vdc |
| Voltage at Video Amplifier Inputs | 2, 4, 6 | –0.5, +5.0 | Vdc |
| Collector–Emitter Current (Three Channels) | Video $V_{CC}$ | 120 | mA |
| Storage Temperature | – | –65 to +150 | °C |
| Junction Temperature | – | 150 | °C |

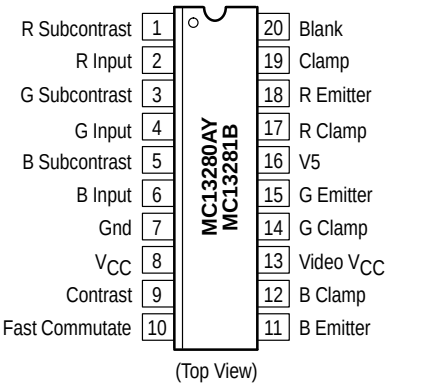
**NOTES:** 1. Devices should not be operated at these limits. Refer to "Recommended Operating Conditions" section for actual device operation.

2. ESD data available upon request.

**PIN CONNECTIONS**




(Top View)




(Top View)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**RECOMMENDED OPERATING CONDITIONS**

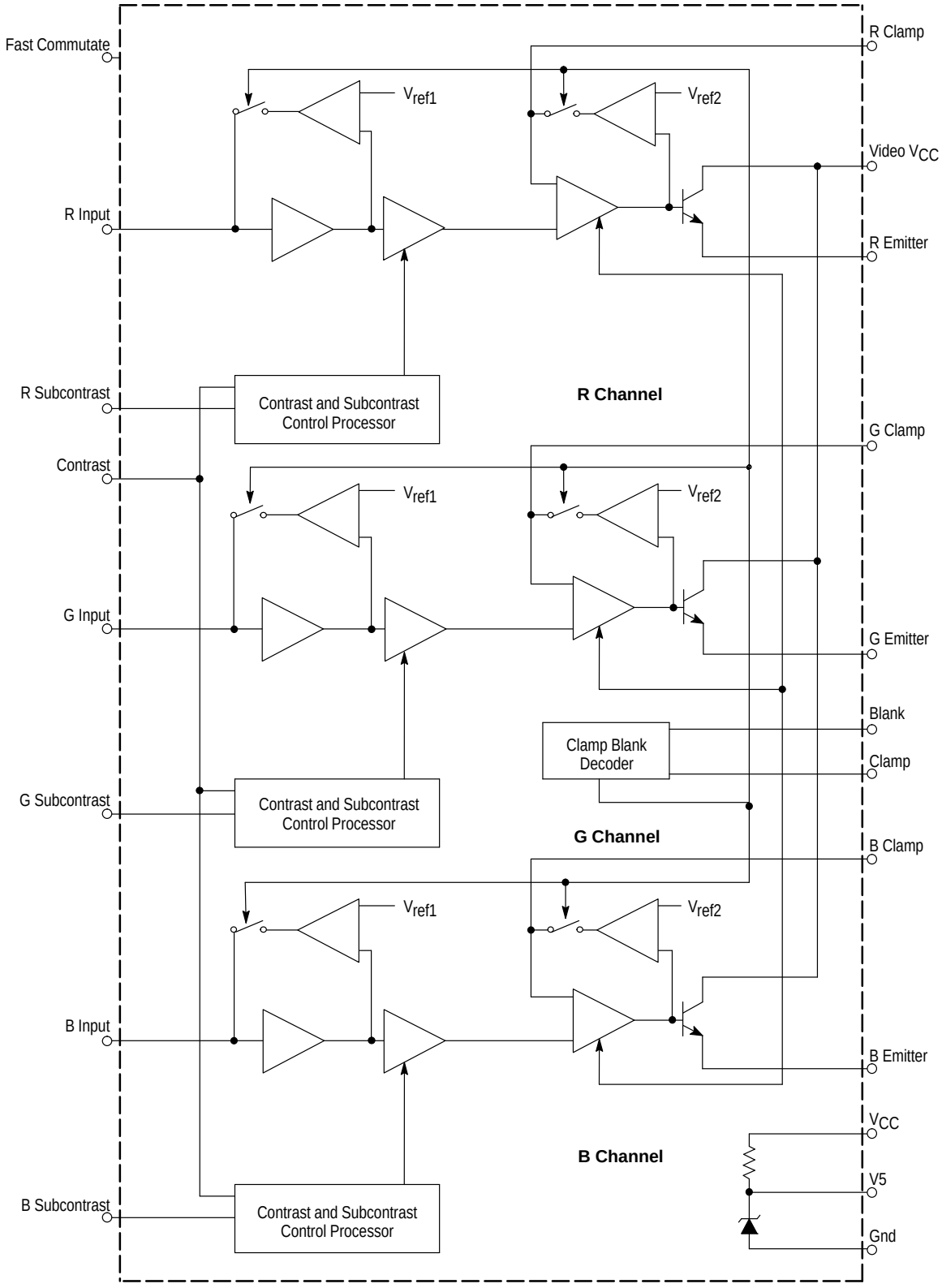
| Characteristic | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$, Video $V_{CC}$ | 7.6 | 8.0 | 8.4 | Vdc |
| Contrast Control | Contrast | 0 | – | 5.0 | Vdc |
| Subcontrast Control | 1, 3, 5 | 0 | – | 5.0 | Vdc |
| Blanking Input Signal Amplitude | Blank | 0 | – | 5.0 | V |
| Clamping Input Signal Amplitude | Clamp | 0 | – | 5.0 | V |
| Video Signal Amplitude (with 75 Ω Termination) | 2, 4, 6 | – | 0.7 | 1.0 | Vpp |
| Collector–Emitter Current (Total for Three Channels) | Video $V_{CC}$ | 0 | – | 50 | mA |
| Clamp Pulse Width | Clamp | 500 | – | – | ns |
| Operating Ambient Temperature | – | 0 | – | 70 | °C |

**ELECTRICAL CHARACTERISTICS** (Refer to Test Circuit Figure 1, $T_A$ = 25°C, $V_{CC}$ = 8.0 Vdc.)

| Characteristic | Condition | Pin | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Impedance | – | 2, 4, 6 | 100 | – | – | kΩ |
| Internal DC Bias Voltage | | | – | 2.4 | – | Vdc |
| Output Signal Amplitude | V2, V4, V6 = 0.7 Vpp<br>V1, V3, V5 = 5.0 V<br>Contrast = 5.0 V | R, G, B Emitters | 3.6 | 4.0 | – | Vpp |
| Voltage Gain | | | – | 5.6 | – | V/V |
| Contrast Control | Contrast = 5.0 to 0 V<br>V1, V3, V5 = 5.0 V | Contrast | – | –26 | – | dB |
| Subcontrast Control | V1, V3, V5 = 5.0 to 0 V<br>Contrast = 5.0 V | 1, 3, 5 | – | –26 | – | dB |
| Emitter DC Level | – | – | 1.0 | 1.2 | 1.4 | Vdc |
| Blanking Input Threshold | – | Blank | – | 1.25 | – | V |
| Clamping Input Threshold | – | Clamp | – | 3.75 | – | V |
| Video Rise Time<br>MC13280AY<br>MC13281A/B | V2, V4, V6 = 0.7 Vpp<br>$V_{out}$ = 4.0 Vpp<br>$R_L$ > 300 Ω, $C_L$ < 5.0 pF | R, G, B Emitters | <br>–<br>– | <br>4.3<br>3.5 | <br>–<br>– | ns |
| Video Fall Time<br>MC13280AY<br>MC13281A/B | V2, V4, V6 = 0.7 Vpp<br>$V_{out}$ = 4.0 Vpp<br>$R_L$ > 300 Ω, $C_L$ < 5.0 pF | R, G, B Emitters | <br>–<br>– | <br>4.3<br>3.5 | <br>–<br>– | ns |
| Video Bandwidth<br>MC13280AY<br>MC13281A/B | V2, V4, V6 = 0.7 Vpp<br>V1, V3, V5, Contrast = 5.0 V<br>$R_L$ > 300 Ω, $C_L$ < 5.0 pF | R, G, B Emitters | <br>–<br>– | <br>80<br>100 | <br>–<br>– | MHz |
| Power Supply Current | $V_{CC}$, Video $V_{CC}$ = 8.0 V | – | – | 70 | – | mA |

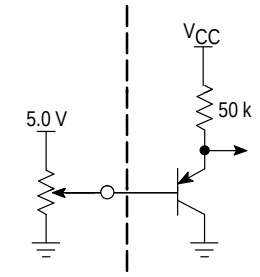
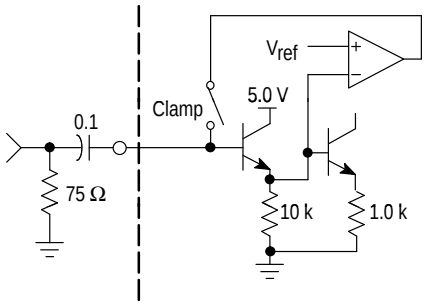
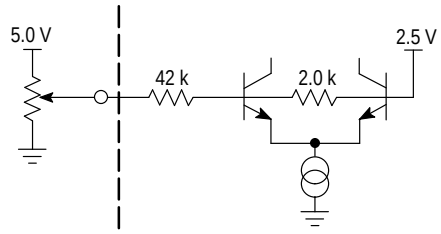
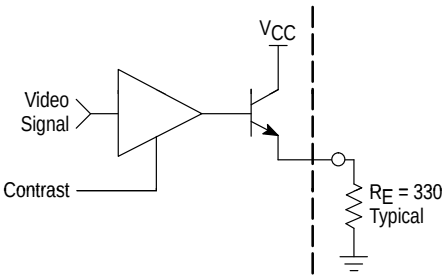
**NOTE:** It is recommended to use a double sided PCB layout for high frequency measurement (e.g., rise/fall time, bandwidth).

**Figure 1. Internal Block Diagram**

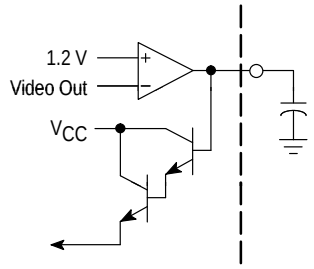
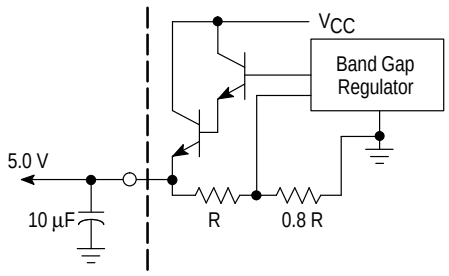
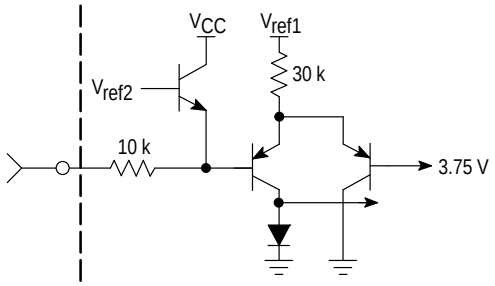
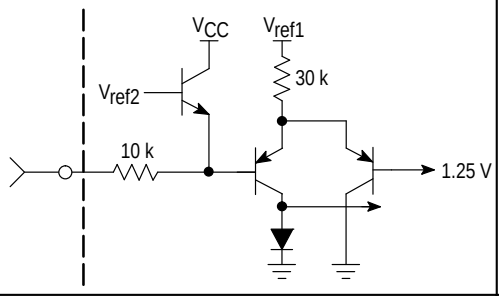



This device contains 272 active transistors.

## PIN FUNCTION DESCRIPTION

| MC13280AY MC13281B Pin | MC13281A Pin | Name | Equivalent Internal Circuit | Description |
|---|---|---|---|---|
| 1<br>3<br>5 | 1<br>3<br>5 | R Subcontrast Control<br>G Subcontrast Control<br>B Subcontrast Control |  | These pins provides a maximum of 26 dB attenuation to vary the gain of each video amplifier separately.<br>Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast level. |
| 2<br>4<br>6 | 2<br>4<br>6 | R Input<br>G Input<br>B Input |  | The input coupling capacitor is used for input clamping storage. The maximum source impedance is 100 Ω.<br>Input polarity of the video signal is positive.<br>Nominal 0.7 Vpp input signal is recommended (maximum 1.0 Vpp). |
| 7 | 7 | Ground | | Ground pin. Connect to a clean, solid ground. |
| N/A | 8<br>10<br>11<br>12 | N/C<br>N/C<br>N/C<br>N/C | | Connected to ground. |
| 8 | 9 | $V_{CC}$ | | Connect to 8.0 Vdc supply, ±5%. Decoupling is required at this pin. |
| 9 | 13 | Contrast |  | Overall Contrast Control for the three channels.<br>The input range is 0 V to 5.0 V. An increase of voltage increases the contrast. |
| 10 | 14 | Fast Commutate | | Must be connected to ground. |
| 11<br>15<br>18 | 15<br>19<br>22 | B Emitter Output<br>G Emitter Output<br>R Emitter Output |  | The video outputs are configured as emitter–followers with a driving capability of about 15 mA each.<br>The dc voltage at these three emitters is set to 1.2 V (black level).<br>The dc current through the output stage is determined by the emitter resistors (typically 330 Ω). |

**PIN FUNCTION DESCRIPTION (continued)**

| MC13280AY MC13281B Pin | MC13281A Pin | Name | Equivalent Internal Circuit | Description |
|---|---|---|---|---|
| 12<br><br>14<br><br>17 | 16<br><br>18<br><br>21 | B Clamp Capacitor<br><br>G Clamp Capacitor<br><br>R Clamp Capacitor |  | A 100 nF capacitor is connected to each of these pins.<br><br>The capacitor is used for video output dc restoration. |
| 13 | 17 | Video $V_{CC}$ | | Connect to 8.0 V dc supply, ±5%. The $V_{CC}$ is for the video output stage. It is internally connected to the collectors of the output transistors. |
| 16 | 20 | 5.0 $V_{ref}$ (V5) |  | 5.0 V regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. It can source up to 20 mA but not sink current. Output impedance is ≈ 10 Ω. Recommended for use as a voltage reference only. |
| 19 | 23 | Clamp |  | This pin is used for video clamping.<br><br>The threshold clamping level is 3.75 V. |
| 20 | 24 | Blank |  | This pin is used for video blanking.<br><br>The threshold blanking level is 1.25 V. |

## FUNCTIONAL DESCRIPTION

The MC13280AY and MC13281A/B are composed of three video amplifiers, clamping and blanking circuitry with contrast and subcontrast controls. Each video amplifier is designed to have a –3.0 dB bandwidth of 100 MHz (MC13281, 80 MHz for the MC13280) with a gain of up to about 5.6 V/V, or 15 dB.

### Video Input

The video input stages are high impedance and designed to accept a maximum signal of 1.0 Vpp with 75 Ω termination (typically) provided externally. During the clamping period, a current is provided to the input capacitor by the clamping circuit which brings the input to a proper dc level (nominal 2.0 V). The blanking and clamping signals are to be provided externally, with their thresholds at 1.25 V and 3.75 V, respectively.

### Video Output

The video output stages are configured as emitter–followers, with a driving capability of about 15 mA for each channel. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through each output stage is determined by the emitter resistor (typically 330 Ω).

### Contrast Control

The contrast control varies the gain of three video amplifiers from a minimum of 0.3 V/V to a maximum of 5.6 V/V when all subcontrast levels are set to 5.0 V.

### Subcontrast Control

Each subcontrast control provides a maximum of 26 dB attenuation on each video amplifier separately.

### Clamp Pulse Input

The clamping pulse is provided externally, and the pulse width must be no less than 500 ns.

### Blank Pulse Input

The blanking pulse is used to blank the video signal during the horizontal sync period, or used as a control pin for video mute function.

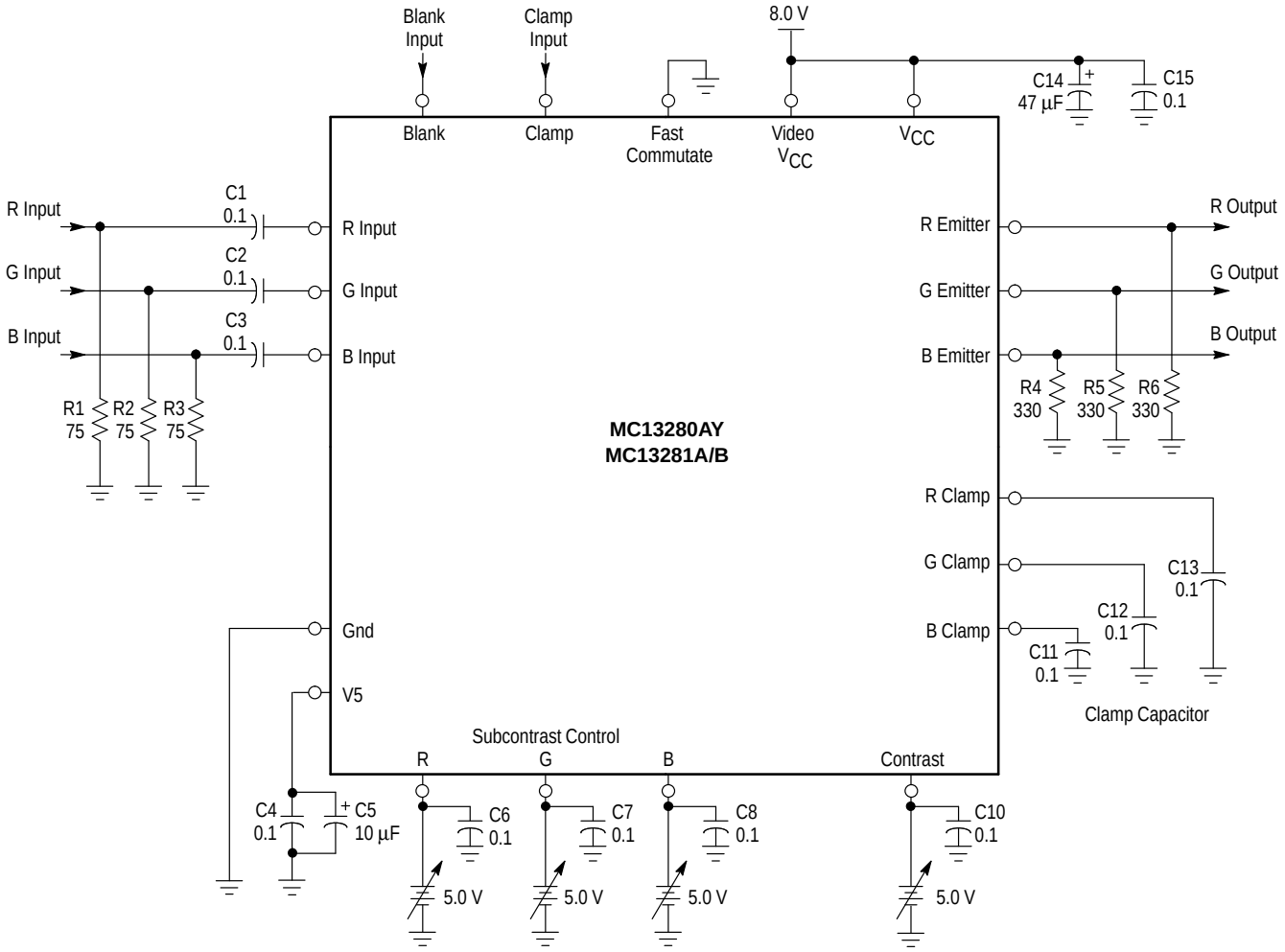
### Fast Commutate

This pin should be connected to ground.

### Power Supplies

$V_{CC}$ and Video $V_{CC}$ supplies are to be 8.0 V ±5%.

**Figure 2. Test Circuit**



## APPLICATION INFORMATION

### PCB Layout

Care should be taken in the PCB layout to minimize the noise effects. The most sensitive pins are $V_{CC}$, Video $V_{CC}$, V5 and Clamp. It is strongly recommended to make a ground plane and connect $V_{CC}$/Video $V_{CC}$ and ground traces, to the power supply directly. Separate power supply traces should be used for $V_{CC}$ and Video $V_{CC}$ and decoupling capacitors should be connected as close as possible to the device. Multi–layer ceramic and tantalum capacitors are recommended. V5 is designed as a 5.0 V voltage reference for contrast, and RGB subcontrast controls, so the same precautions for $V_{CC}$ should also be applied at this pin. The Clamp capacitors should be connected to ground close to IC's ground pin, or power supply ground. The copper trace of video signal inputs and outputs should be as short as possible and separated by ground traces to avoid any RGB cross–interference. A double sided PCB should be used to optimize the device's performance.

### RGB Input and Output

The RGB output stages are designed as emitter–followers to drive the CRT driver circuitry directly. The emitter resistors used are 330 Ω (typically) and the driving current is 15 mA maximum for each channel. The loading impedance connected to the output stages should be greater than 330 Ω and less than 5.0 pF for optimum performance (e.g., rise/fall time, bandwidth, etc.). Decreasing the resistive load will reduce the rise/fall time by increasing the driving current, but the output stage may be damaged due to increasing power dissipation at the same time. The frequency response is affected by the loading capacitance. The typical value is 3.0 to 5.0 pF. Figure 3 shows a typical interface with a video output driver. For high resolution color monitor application, it is recommended to use coaxial cable or shielded cable for input signal connections.

### Clamp and Blank Input

The clamp input is normally (except for Sync–on–Green) connected to a positive horizontal sync pulse and has a threshold level of 3.75 V. It is used as a timing reference for the dc restoration process, so it cannot be an open circuit. If Sync–on–Green timing mode is used, the clamping pulse should be located at the horizontal back porch period instead of horizontal sync. Otherwise, the black level will be clamped at the wrong dc level.

The blank input is used as a video mute, or horizontal blanking control pin, and is normally connected to a blanking pulse generated from the flyback or MCU. The threshold level is 1.25 V. The blanking pulse width should be equal to the flyback retrace period to make sure that the video signal is blanked properly during retrace. It is necessary to limit the amplitude and avoid any negative undershoot if the flyback pulse is used. The blanking input pin cannot accept a negative voltage. This pin should be grounded if it is not used.

**Figure 3. Interfacing with Video Output Drivers**

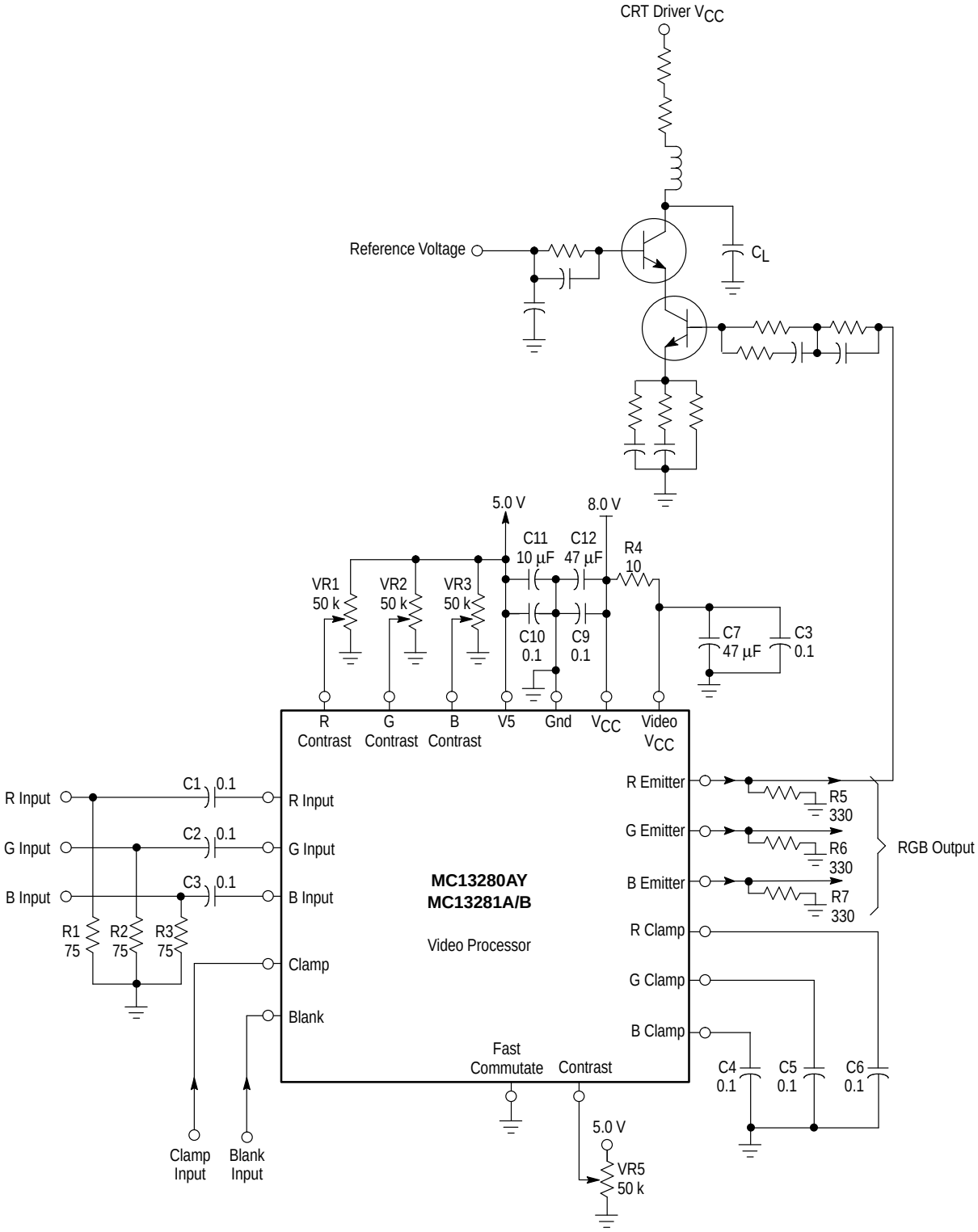


**Figure 4. RGB In/Out Linearity**

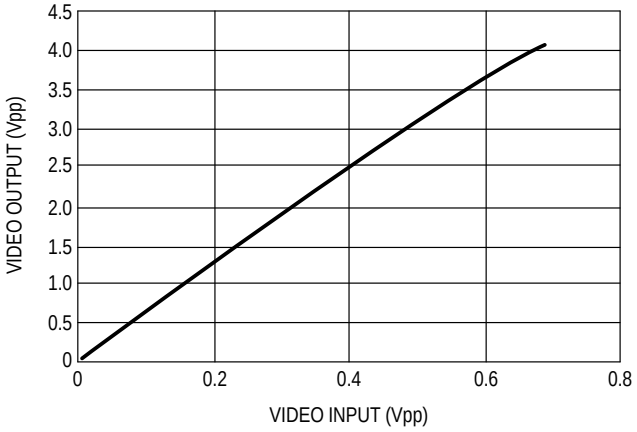



**Figure 5. Contrast Control**

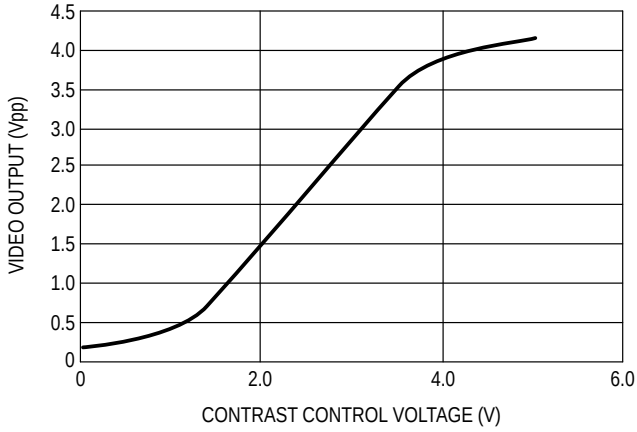



**Figure 6. Subcontrast Control**

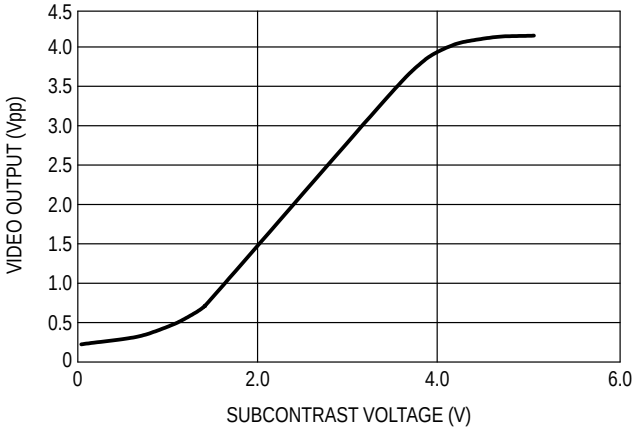



**Figure 7. Crosstalk From Green to Red and Blue Channels**

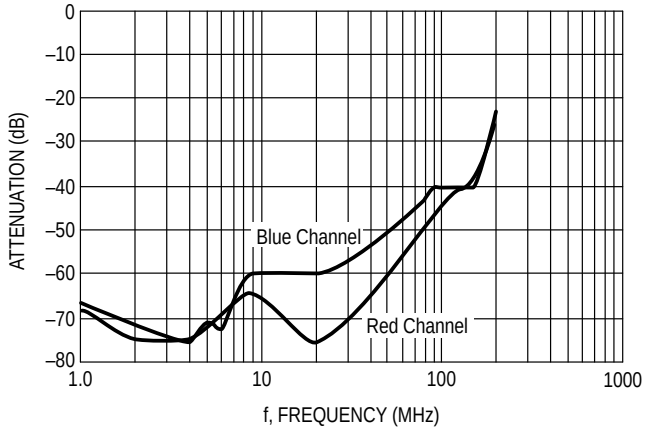
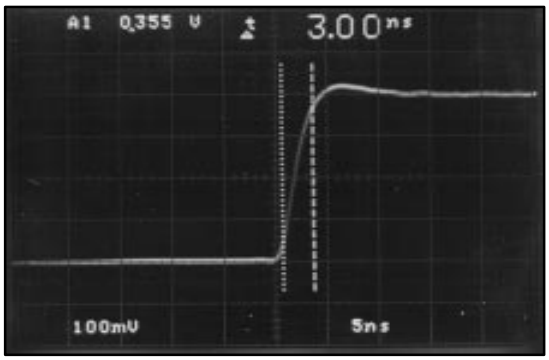
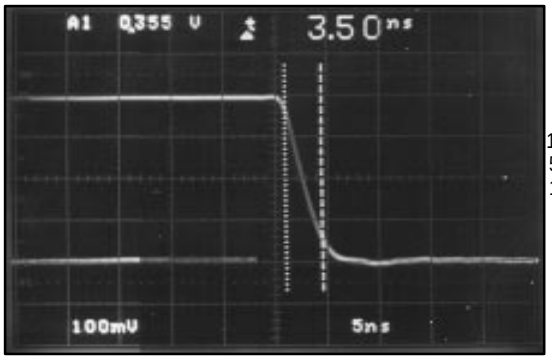


**Figure 8. Rise Time for MC13281B**




100 mV/DIV
5.0 ns/DIV
10x PROBE

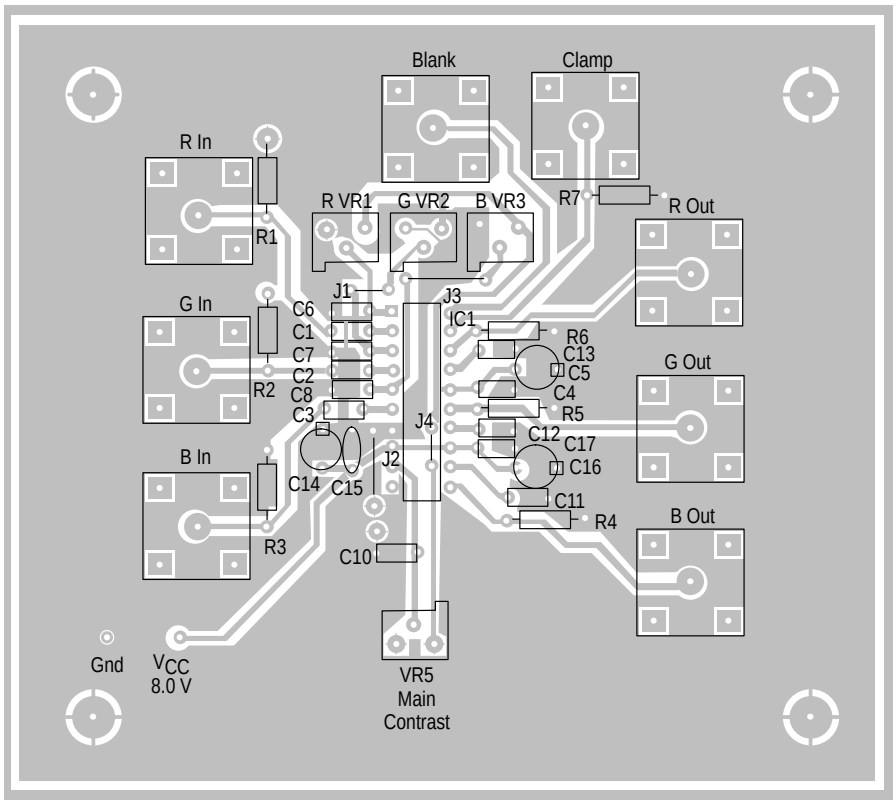
**Figure 9. Fall Time for MC13281B**




100 mV/DIV
5.0 ns/DIV
10x PROBE

**NOTE:** Recommend to use a double sided PCB without any socket for rise/fall time measurements, using an input pulse with 1.5 ns rise/fall time and an active probe with 1.7 pF capacitance loading.

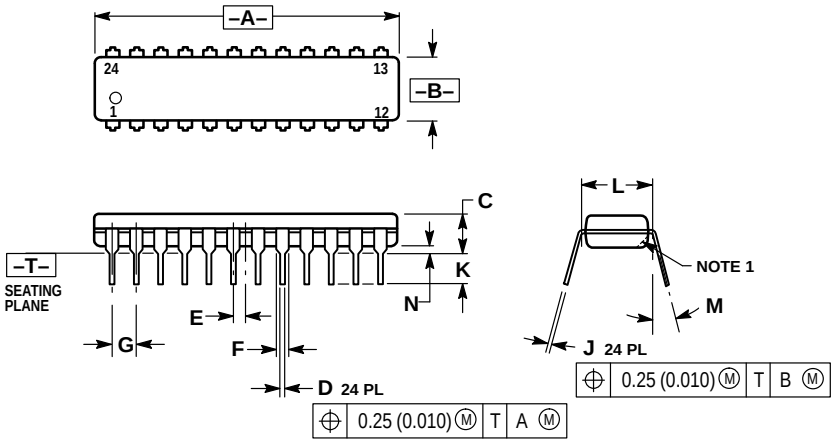
**Figure 10. Single Sided PCB Layout (Component Side) for MC13280AY, MC13281B**




**NOTE:** J = Jumper

## OUTLINE DIMENSIONS

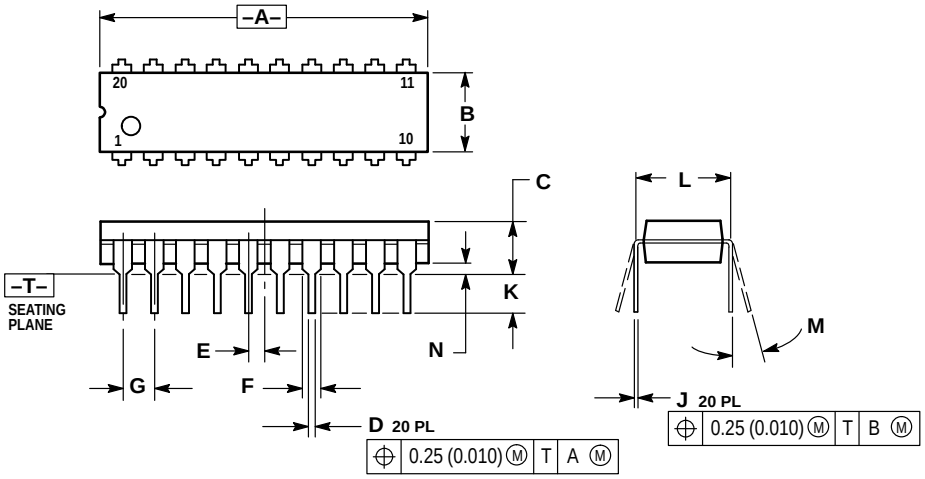
**P SUFFIX**
PLASTIC PACKAGE
CASE 724–03
ISSUE D




NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.230 | 1.265 | 31.25 | 32.13 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.020 | 0.38 | 0.51 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.040 | 0.060 | 1.02 | 1.52 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.007 | 0.012 | 0.18 | 0.30 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**P SUFFIX**
PLASTIC PACKAGE
CASE 738–03
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**How to reach us:**

**USA / EUROPE / Locations Not Listed**: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

**MFAX**: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609

**INTERNET**: http://Design–NET.com

**JAPAN**: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

**ASIA / PACIFIC**: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298