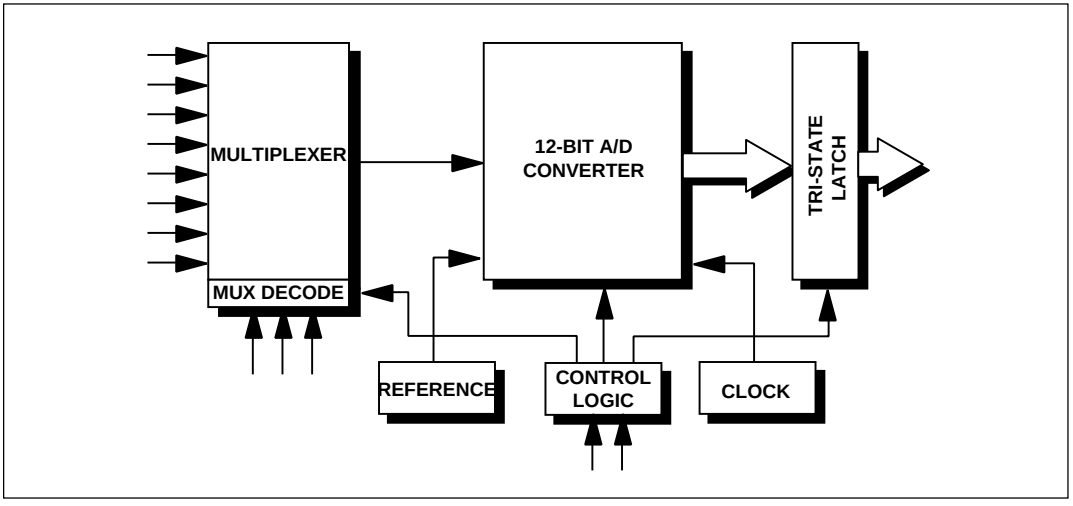
Monolithic, 12–Bit Data Acquisition System

- Complete Monolithic 8-Channel, 12-Bit DAS
- 100kHz Throughput
- 16-Bit Microprocessor Bus Interface
- Parallel 12-Bit Output
- Latched MUX Address
- Tri-State Latched Output
- No Missing Codes to 12-Bits
- 32-pin SOIC and PDIP Available
- 200mW Power Dissipation Maximum

* Formerly part of the **SP410 Series**.

DESCRIPTION

The **SP8121** is a complete data acquisition systems, featuring 8-channel multiplexer, internal reference and 12-bit sampling A/D converter implemented as a single monolithic IC. The analog multiplexer accepts 0V to +5V unipolar full scale inputs. Output data is formatted in 12-bit parallel. The **SP8121** is available in 32-pin plastic DIP or SOIC packages, operating over the commercial temperature range.



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Common Ground ..... 0V to +16.5V
V_{LOGIC} to Common Ground ..... 0V to +7V
Analog Common to Digital Common Ground ..... -0.5V to +1V
Digital Inputs to Common Ground ..... -0.5V to V_{LOGIC}+0.5V
Digital Outputs to Common Ground ..... -0.5V to V_{LOGIC}+0.5V
Multiplexer Analog Inputs ..... -16.5V to +31.5V
Gain and Offset Adjustment ..... -0.5V to V_{CC}+0.5V
Analog Input Maximum Current 100mA
Temperature with Bias Applied ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature, Soldering ..... 300°C, 10sec

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(T_A= 25°C and nominal supply voltages unless otherwise noted)

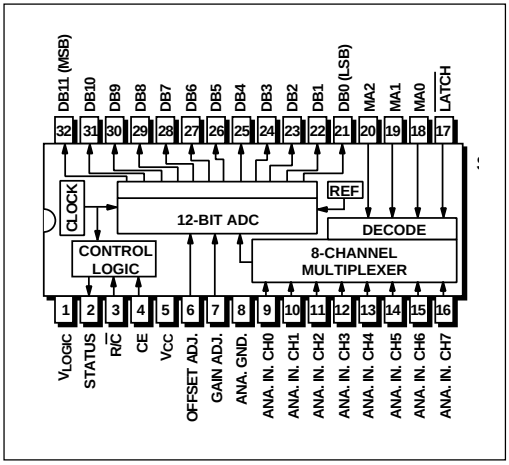
	MIN.	TYP.	MAX.	UNIT	CONDITIONS
ANALOG INPUTS					
Input Voltage Range		0 to +5		V	
Multiplexer Inputs			8		
Configuration		Single-ended			
Input Impedance					
ON Channel		10^9		Ω	Parallel with 30pF
OFF Channel		10^{10}		Ω	Parallel with 5pF
Input Bias Current/Channel		±10		nA	25°C
		±250		nA	-55°C to +125°C
Crosstalk					
OFF to ON Channel			-90	dB	10kHz, 0V to +5$V_{Pk\text{-}to\text{-}pk}$
			-80	dB	50kHz, 0V to +5$V_{Pk\text{-}to\text{-}pk}$
			-70	dB	100kHz, 0V to +5$V_{Pk\text{-}to\text{-}pk}$
ACCURACY					
Resolution	12			Bits	
Linearity Error					
–K			±0.5	LSB	
–J			±1	LSB	
Differential Non-Linearity					
–K			±1	LSB	
–J			±2	LSB	
Offset Error		±0.5	±4	LSB	Adjustable to zero
Gain Error		±0.3	±1	%FSR	Adjustable to zero
No Missing Codes					
–K		Guaranteed			
TRANSFER CHARACTERISTICS					
Throughput Rate	100			kHz	
MUX Settling/Acquisition			1.9	µs	
A/D Conversion			8.1	µs	
STABILITY					
Linearity		±0.5	±2.5	ppm/°C	
Offset		±5	±25	ppm/°C	
Gain		±10	±50	ppm/°C	
DIGITAL INPUTS					
Capacitance		5		pF	
Logic Levels					
V_{IH}	+2.4		+5.5	V	
V_{IL}	-0.5		+0.8	V	
I_{IH}			±5	µA	
I_{IL}			±5	µA	

SPECIFICATIONS (continued)

(T_A = 25°C and nominal supply voltages unless otherwise noted)

	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DIGITAL OUTPUTS					
Capacitance		5		pF	
Logic Levels					
V_{OH}	+2.4			V	$I_{OH} \leq$ 500µA
V_{OL}			+0.4	V	$I_{OL} \leq$ 1.6mA
Leakage Current		±40		µA	High impedance, data bits only
Data Output		Positive true binary			
POWER REQUIREMENTS					
V_{LOGIC}	+4.5		+5.5	V	
I_{LOGIC}		0.8	4	mA	
V_{CC}	+11.4		+16.5	V	
I_{CC}		9	12	mA	
Power Dissipation		140	200	mW	
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature					
Commercial (–J, –K)	0		+70	°C	
Storage Temperature	-65		+150	°C	
Packages					
–_P		32–pin Plastic DIP			
–_S		32–pin SOIC			

SP8121 PINOUT



SP8121 PINOUT

STATUS — Identifies valid data output; goes to logic high during conversion; goes to logic low when conversion is completed and data is valid

R/$\overline{C}$ — Read/$\overline{Convert}$ — Initiates conversion on the high-to-low transition; logic low disconnects data bus; logic high initiates read

CE — Chip Enable — Logic low disables read or convert; logic high enables read or convert

$\overline{LATCH}$ — MUX Address Latch — Logic high to low transition captures MUX address on MUX address lines

MA_0, MA_1, MA_2 — MUX Address 0, 1 & 2 — Selects analog input channels CH_0 through CH_7

DB_0 through DB_{11} — Data Outputs — Logic high is binary true; logic low binary false

SP8121 CONTROL TRUTH TABLE

CE	R/$\overline{C}$	OPERATION
L->H	0	Start Conversion
1	0	Start Conversion
1	H ->L	Start Conversion
1	1	Enable 12-bit Output (when STATUS=0)

SP8121 MULTIPLEXER TRUTH TABLE

LATCH	MA_2	MA_1	MA_0	OPERATION
H -> L	0	0	0	CH_0 Selected
H -> L	0	0	1	CH_1 Selected
H -> L	0	1	0	CH_2 Selected
H -> L	0	1	1	CH_3 Selected
H -> L	1	0	0	CH_4 Selected
H -> L	1	0	1	CH_5 Selected
H -> L	1	1	0	CH_6 Selected
H -> L	1	1	1	CH_7 Selected
0	X	X	X	Prev. CH “n” Held
1	X	X	X	Prev. CH “n” Held

FEATURES

The **SP8121** is a complete data acquisition systems, featuring 8-channel multiplexer, internal reference and 12-bit sampling A/D converter implemented as a single monolithic IC. The analog multiplexer accepts 0V to +5V unipolar full scale inputs. Output data is formatted in 12-bit parallel.

Linearity errors of ±0.5 and ±1.0 LSB, and Differential Non-linearity to 12-bits is guaranteed, with no missing codes over temperature. Channel-to-channel crosstalk is typically -85dB. Multiplexer settling plus acquisition time is 1.9µs maximum; A/D conversion time is 8.1µs maximum.

The **SP8121** is available in a 32-pin plastic DIP or SOIC packages. Operating temperature range is 0°C to +70°C commercial.

CIRCUIT OPERATION

The **SP8121** is a complete 8-channel data acquisition systems (DAS), with on-board multiplexer, voltage reference, sample-and-hold, clock and tri-state outputs. The digital control architecture is very similar to the industry-standard 574-type A/D, and uses identical control lines and digital states.

The multiplexer for the **SP8121** is identical in operation to many discrete devices available today, except that it has been integrated into the single-chip DAS. The appropriate channel is selected using the MUX address lines MA_0, MA_1, and MA_2 per the truth table. The selected analog input is fed through to the ADC. The input impedance into any MUX channel will be on the order to 10^9 ohms, since it is connected to the integral sampling structure of the capacitor DAC. Crosstalk is kept to -85dB at 0V to $5V_{p-p}$ over an input frequency range of 10kHz to 50kHz.

When the control section of the **SP8121** initiates a conversion command the internal clock is enabled, and the successive approximation register (SAR) is reset to all zeros. Once the conversion has been started it cannot be stopped or restarted. Data is not available at the output buffers until the conversion has been completed.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end–of–convert flag to the control section of the ADC. The clock is then disabled by the control section, which puts the STATUS output line low. The control section is enabled to allow the data to be read by external command (R/$\overline{C}$).

MULTIPLEXER CONTROL

On the **SP8121** the address lines MA0, MA1, and MA2 are latched into the internal address decode circuitry with the falling edge of $\overline{LATCH}$. Data set-up time for these inputs is >=50nS. The MUX address data must remain valid for the current conversion for a minimum of 3.0 µS after the conversion is initiated. This is the time required for the MUX and Sample and Hold to settle. However it is advisable that the MUX not be changed at all during the full 10µS conversion time due to capacitive coupling effects of digital edges through the silicon.

The **SP8121** multiplexer inputs have been designed to allow substantial overvoltage conditions to occur without any damage. The inputs are diode-clamped and further protected with a 200Ω series resistor. As a result, momentary (10 seconds) input voltages can be as low as -16.5V or as high as +31.5V with no change or degradation in multiplexer performance or crosstalk. This feature allows the output voltage of an externally connected op amp to swing to ±15V supply levels with no multiplexer damage. Complicated power-up sequencing is not required to protect the **SP8121**. The multiplexer inputs may be damaged, however, if the inputs are allowed to either source or sink greater than 100mA.

INITIATING A CONVERSION

The **SP8121** was designed to require a minimum of control to perform a 12-bit conversion. The control input used are R/$\overline{C}$ which tri-states the outputs when high and starts the conversion when low, in combination with CE. The last of the control inputs to reach the correct state starts the conversion, therefore either may be dynamically controlled. The nominal delay from each is the same and they may change state simultaneously. In order to ensure that a particular input controls the conversion, the other should be set up at least 50ns earlier. The STATUS line indicates when a conversion is in process and when it is complete.

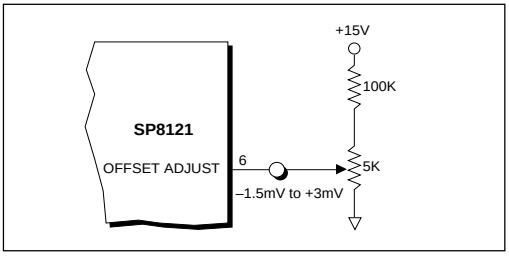


Figure 1. Offset Adjust

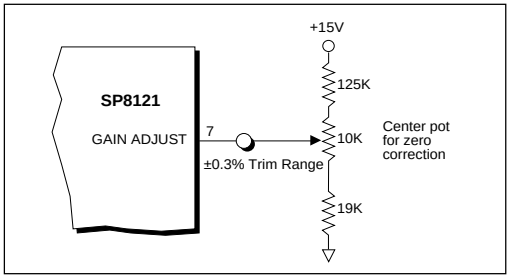


Figure 2. Gain Adjust

The conversion cycle is started when R/$\overline{C}$ is brought low and must be held low for a minimum of 50ns. The R/$\overline{C}$ signal will also put the output latches in a tri-state mode when low. Approximately 200ns after R/$\overline{C}$ is low, STATUS will change from low to high. This output signal will stay high while the **SP8121** is performing a conversion. Valid data will be latched to the output bus, through internal control, 500ns prior to the STATUS line transitioning from a high to low.

READING THE DATA

Please refer to *Figure 4*. To read data from the **SP8121**, the R/$\overline{C}$ and CE control lines are used. R/$\overline{C}$ must be high a minimum of 50ns prior to reading the data to allow time for the output latches to come out of the high impedance tri-state mode. CE is used to access the data. The first 8 MSBs will be on pins 32 through 25, with pin 32 being the MSB. The remaining 4 LSBs will be on pins 21 through 24 with pin 21 being the LSB. When CE is switched from one state to the next, there is a 50ns output latch propagation delay between the MSBs and LSBs being present on the output pins.

CALIBRATION

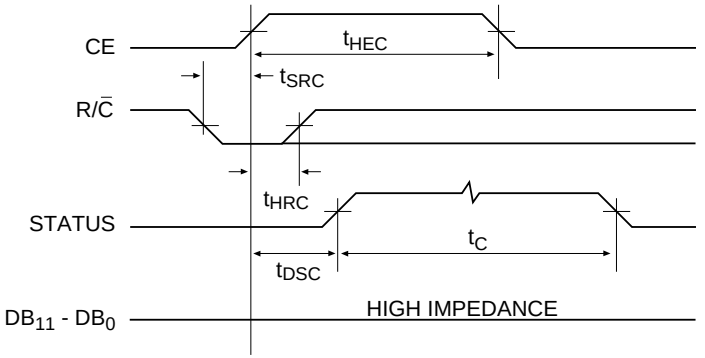
The calibration procedure for the **SP8121** consists of adjusting the most negative input voltage (0V) to the ideal output code for offset adjustment, and then adjusting the most positive input voltage (5.0V) to its ideal output code for gain adjustment.

Offset Adjustment

The offset adjustment must be completed first. Please refer to *Figure 1*. Apply an input voltage of 0.5LSB or 610µV to any multiplexer input. Adjust the offset potentiometer so that the output code fluctuates evenly between 000…000 and 000…001. It is only necessary to observe the lower eight LSB's during this procedure.

Gain Adjustment

With the offset adjusted, the gain error can now be trimmed to zero. (Please refer to *Figure 2*.) The ideal input voltage corresponding to 1.5 LSB's below the nominal full scale input value, or +4.988V, is applied to any multiplexer input. The gain potentiometer is adjusted so that the output code alternates evenly between 111…111 and 111…110. Again, only the lower eight LSB's need be observed during this procedure. With the above adjustment made, the converter is now calibrated.

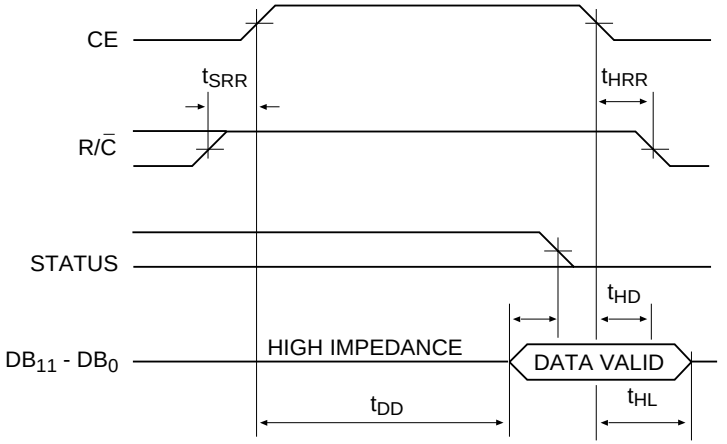


CONVERT MODE DYNAMIC CHARACTERISTICS

V_{CC} = +15V; V_{LOGIC} = +5V; T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{HEC} CE Pulse Width	50			ns	
t_{SRC} R/$\overline{C}$ to CE Setup	50			ns	
t_{HRC} R/$\overline{C}$ Low during CE High	50			ns	
t_{DSC} Status Delay from CE			200	ns	

Figure 3. Convert Mode Timing

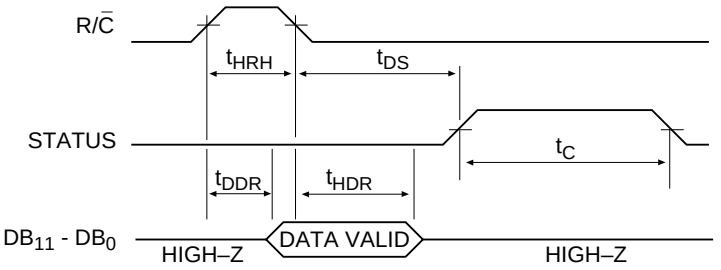


READ MODE DYNAMIC CHARACTERISTICS

V_{CC} = +15V; V_{LOGIC} = +5V; T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{SRR} R/$\overline{C}$ to CE Setup	0	0		ns	
t_{HRR} R/$\overline{C}$ High after CE Low	0	50		ns	
t_{HD} Data Valid after CE Low	25			ns	
t_{DD} Access Time from CE			150	ns	
t_{HL} Output Float Delay			150	ns	

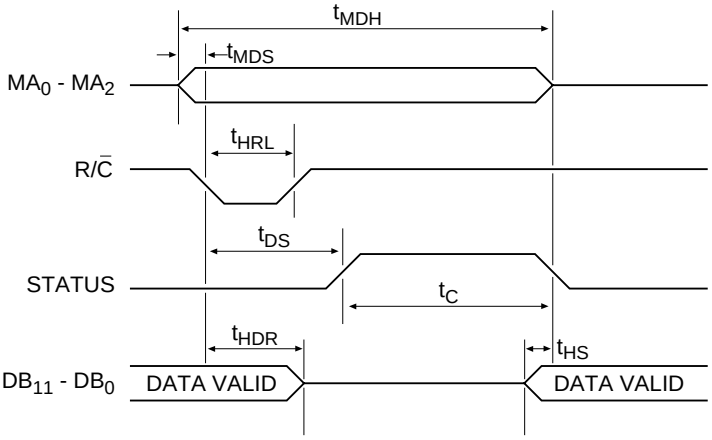
Figure 4. Read Mode Timing



HIGH PULSE FOR R/C̄ DYNAMIC CHARACTERISTICS
V_{CC} = +15V; V_{LOGIC} = +5V; T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{HRH} High R/C̄ Pulse Width	25			ns	
t_{DS} STATUS Delay from R/C̄			200	ns	
t_C Conversion Time	13		25	µs	T_{MIN} to T_{MAX}
t_{DDR} Data Access Time			150	ns	
t_{HDR} Data Valid after R/C̄ Low	25			ns	

Figure 5. High Pulse for R/C̄ — Outputs Enabled While R/C̄ is High, Otherwise High Impedance



LOW PULSE FOR R/C DYNAMIC CHARACTERISTICS
V_{CC} = +15V; V_{LOGIC} = +5V; T_A = 25°C

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{HRL} Low R/C Pulse Width	50			ns	
t_{DS} Status Delay from R/C̄			200	ns	
t_{HDR} Data Valid after R/C̄	25			ns	
t_{HS} Status Delay after Data Valid	500			ns	
t_{MDS} MUX Data Setup	50			ns	
t_{MDH} MUX Data Valid	3		10	µs	

Figure 6. Low Pulse for R/C̄

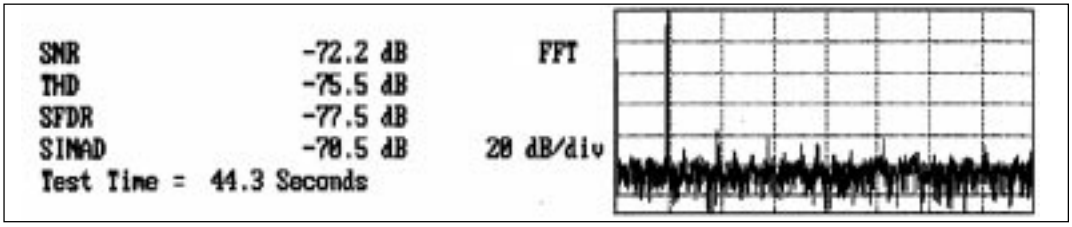


Figure 7. FFT; 6kHz, 5V (0dB) Full Scale Input; F_S = 100kHz

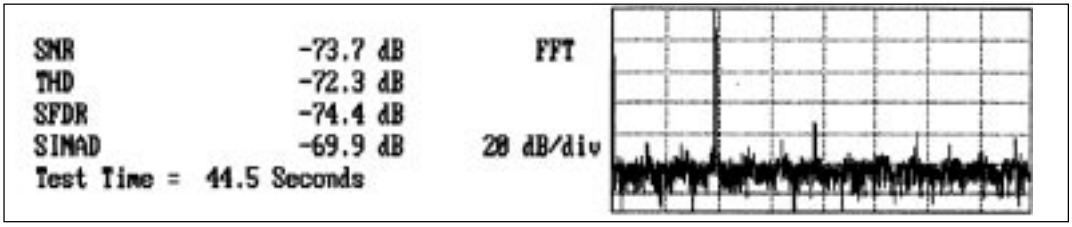


Figure 8. FFT; 12kHz, 5V (0dB) Full Scale Input; F_S = 100kHz

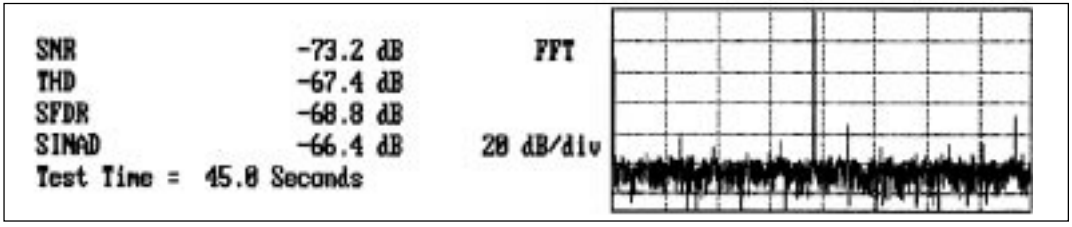


Figure 9. FFT; 24kHz, 5V (0dB) Full Scale Input; F_S = 100kHz

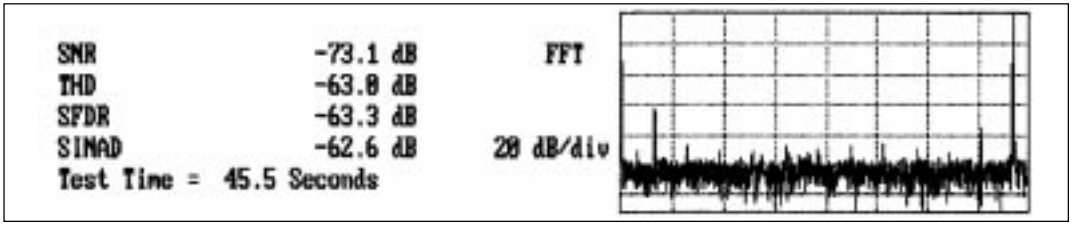


Figure 10. FFT; 48kHz, 5V (0dB) Full Scale Input; F_S = 100kHz

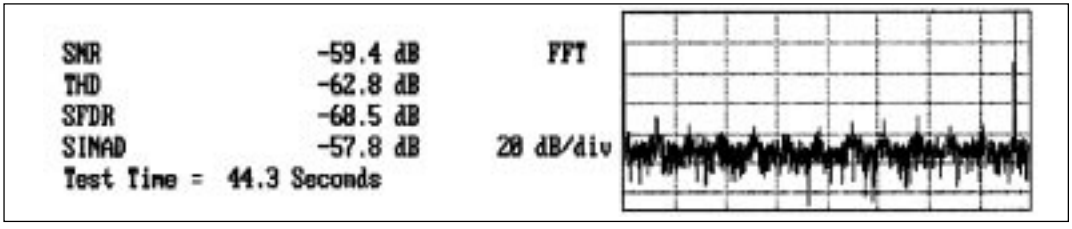
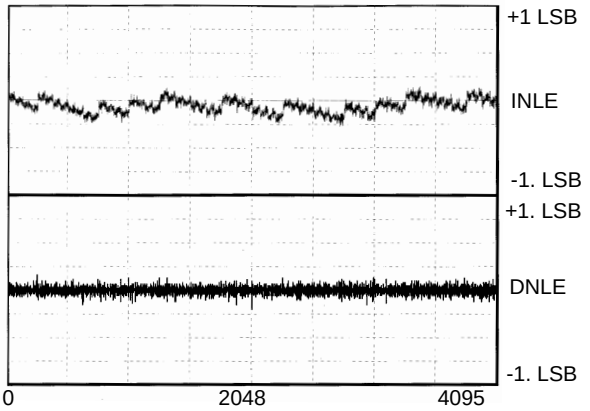


Figure 11. FFT; 48kHz, 1V (–14dB) Input; F_S = 100kHz




```
Icc :                1.964 (mA)
Power :              9.821 (mW)

LSB size :           1.221     (mV)
Conv. rate :         9.92 (us)
Avrg. histo. :       61.666

Offset :   -1.       (LSB)
Gain :      0.247    (%fsr)
INLE max : 0.151     (LSB)
INLE min : -0.277    (LSB)
INLE BSL : 0.214     (LSB)
DNLE max : 0.168     (LSB)
DNLE min : -0.205    (LSB)
DNLE RMS : 0.041     (LSB)
bit DNLEs (at the bit)       (4 codes away)
 DNLE5 : 0.070 (LSB)         0.020 (LSB)
 DNLE6 : 0.037 (LSB)         -0.037 (LSB)
 DNLE7 : -0.075 (LSB)        -0.037 (LSB)
 DNLE8 : 0.168 (LSB)         0.091 (LSB)
 DNLE9 : 0.037 (LSB)         -0.057 (LSB)
 DNLE10 : 0.135 (LSB)        0.072 (LSB)
 DNLE11 : -0.205 (LSB)       -0.079 (LSB)
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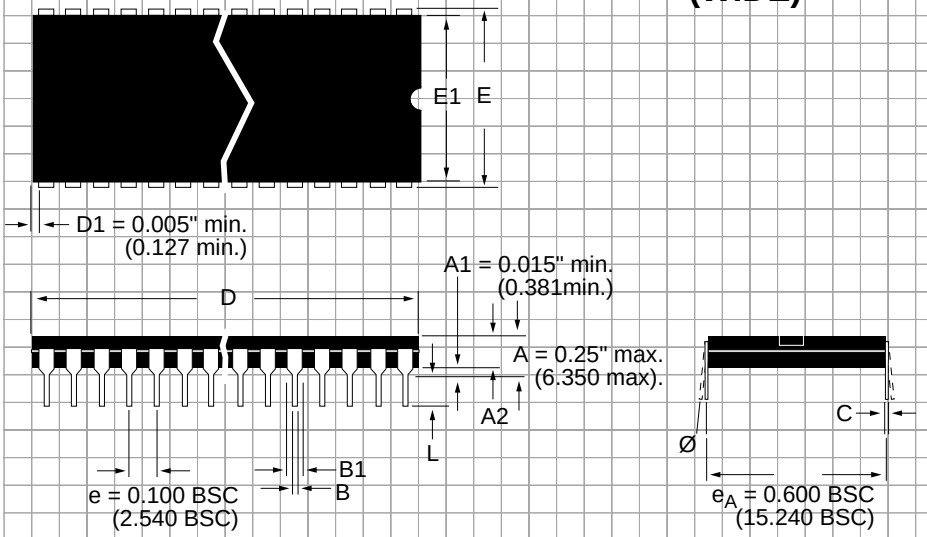
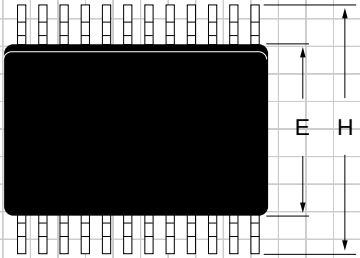
Figure 12. Non-Linearity

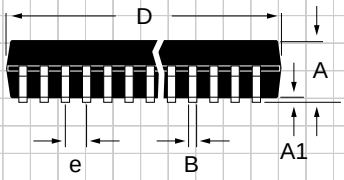
PACKAGE: PLASTIC DUAL–IN–LINE (WIDE)

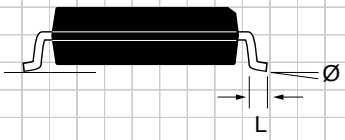


DIMENSIONS (Inches) Minimum/Maximum (mm)	32–PIN
A2	0.125/0.195 (3.175/4.953)
B	0.014/0.022 (0.366/0.559
B1	0.030/0.070 (0.762/1.778)
C	0.008/0.015 (0.203/0.381)
D	1.645/1.655 (41.78/42.04)
E	0.600/0.625 (15.24/15.87)
E1	0.485/0.580 (12.31/14.73)
L	0.115/0.200 (2.921/5.080)
Ø	0°/ 15° (0°/15°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)







DIMENSIONS (Inches) Minimum/Maximum (mm)	32–PIN
A	0.090/0.104 (2.29/2.649)
A1	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)
D	0.810/0.822 (20.57/20.88)
E	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)

ORDERING INFORMATION

12-Bit Data Acquisition System with 12-Bit Parallel Data Output and latched MUX Address Inputs:

Commercial Temperature Range (0°C to +70°C)	Linearity	Package
SP8121JP	±1.0LSB INL	32–pin, 0.6" Plastic DIP
SP8121KP	±0.5LSB INL	32–pin, 0.6" Plastic DIP
SP8121JS	±1.0LSB INL	32–pin, 0.3" SOIC
SP8121KS	±0.5LSB INL	32–pin, 0.3" SOIC

Please consult the factory for pricing and availability on a Tape-On-Reel option.

Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Sipex Corporation

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