

# DATA SHEET



## **PCA9552**

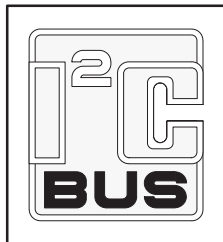
16-bit I<sup>2</sup>C LED driver with programmable  
blink rates

Product data sheet  
Supersedes data of 2003 May 02

2004 Oct 01

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

## PCA9552



### FEATURES

- 16 LED drivers (on, off, flashing at a programmable rate)
- 2 selectable, fully programmable blink rates (frequency and duty cycle) between 0.172 Hz and 44 Hz (5.82 and 0.023 seconds)
- Input/outputs not used as LED drivers can be used as regular GPIOs
- Internal oscillator requires no external components
- I<sup>2</sup>C-bus interface logic compatible with SMBus
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Active-LOW reset input
- 16 open drain outputs directly drive LEDs to 25 mA
- Edge rate control on outputs
- No glitch on power-up
- Supports hot insertion
- Low stand-by current
- Operating power supply voltage range of 2.3 V to 5.5 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO24, TSSOP24, HVQFN24

### ORDERING INFORMATION

| PACKAGES             | TEMPERATURE RANGE | ORDER CODE | TOPSIDE MARK | DRAWING NUMBER |
|----------------------|-------------------|------------|--------------|----------------|
| 24-pin plastic SO    | -40 °C to +85 °C  | PCA9552D   | PCA9552D     | SOT137-1       |
| 24-pin plastic TSSOP | -40 °C to +85 °C  | PCA9552PW  | PCA9552PW    | SOT355-1       |
| 24-pin plastic HVQFN | -40 °C to +85 °C  | PCA9552BS  | 9552         | SOT616-1       |

Standard packing quantities and other packaging data are available at [www.standardproducts.philips.com/packaging](http://www.standardproducts.philips.com/packaging).  
I<sup>2</sup>C is a trademark of Philips Semiconductors Corporation.

### DESCRIPTION

The PCA9552 LED Blinker blinks LEDs in I<sup>2</sup>C-bus and SMBus applications where it is necessary to limit bus traffic or free up the I<sup>2</sup>C Master's (MCU, MPU, DSP, chipset, etc.) timer. The uniqueness of this device is the internal oscillator with two programmable blink rates. To blink LEDs using normal I/O Expanders like the PCF8574 or PCA9554, the bus master must send repeated commands to turn the LED on and off. This greatly increases the amount of traffic on the I<sup>2</sup>C-bus and uses up one of the master's timers. The PCA9552 LED Blinker instead requires only the initial set up command to program BLINK RATE 1 and BLINK RATE 2 (i.e., the frequency and duty cycle) for each individual output. From then on, only one command from the bus master is required to turn each individual open drain output ON, OFF, or to cycle at BLINK RATE 1 or BLINK RATE 2. Maximum output sink current is 25 mA per bit and 200 mA per package.

Any bits not used for controlling the LEDs can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The active-LOW hardware reset pin ( $\overline{\text{RESET}}$ ) and Power-On Reset (POR) initializes the registers to their default state, all zeroes, causing the bits to be set HIGH (LED off).

Three hardware address pins on the PCA9552 allow eight devices to operate on the same bus.

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

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## PIN CONFIGURATION — SO, TSSOP

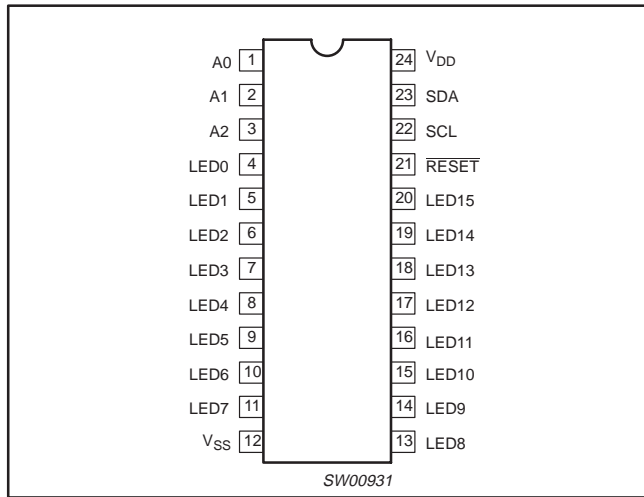


Figure 1. Pin configuration — SO, TSSOP

## PIN CONFIGURATION — HVQFN

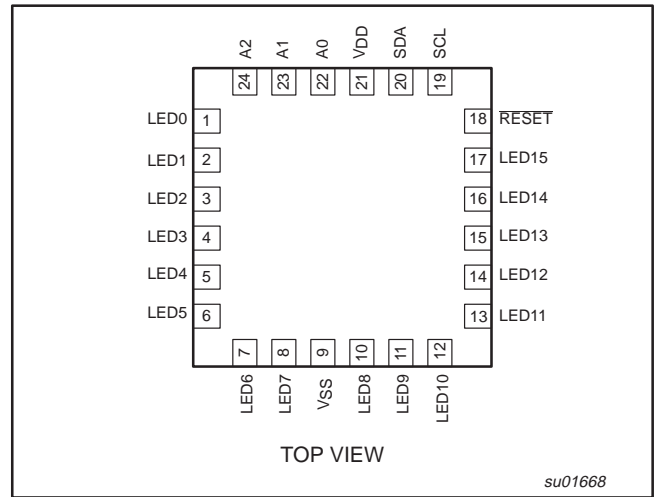


Figure 2. Pin configuration — HVQFN

## PIN DESCRIPTION

| SO, TSSOP<br>PIN<br>NUMBER        | HVQFN<br>PIN<br>NUMBER            | SYMBOL          | FUNCTION               |
|-----------------------------------|-----------------------------------|-----------------|------------------------|
| 1                                 | 22                                | A0              | Address input 0        |
| 2                                 | 23                                | A1              | Address input 1        |
| 3                                 | 24                                | A2              | Address input 2        |
| 4, 5, 6, 7, 8, 9,<br>10, 11       | 1, 2, 3, 4, 5, 6,<br>7, 8         | LED0–7          | LED driver 0–7         |
| 12                                | 9                                 | V <sub>SS</sub> | Supply ground          |
| 13, 14, 15, 16,<br>17, 18, 19, 20 | 10, 11, 12, 13,<br>14, 15, 16, 17 | LED8–15         | LED driver 8–15        |
| 21                                | 18                                | RESET           | Active-LOW reset input |
| 22                                | 19                                | SCL             | Serial clock line      |
| 23                                | 20                                | SDA             | Serial data line       |
| 24                                | 21                                | V <sub>DD</sub> | Supply voltage         |

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## BLOCK DIAGRAM

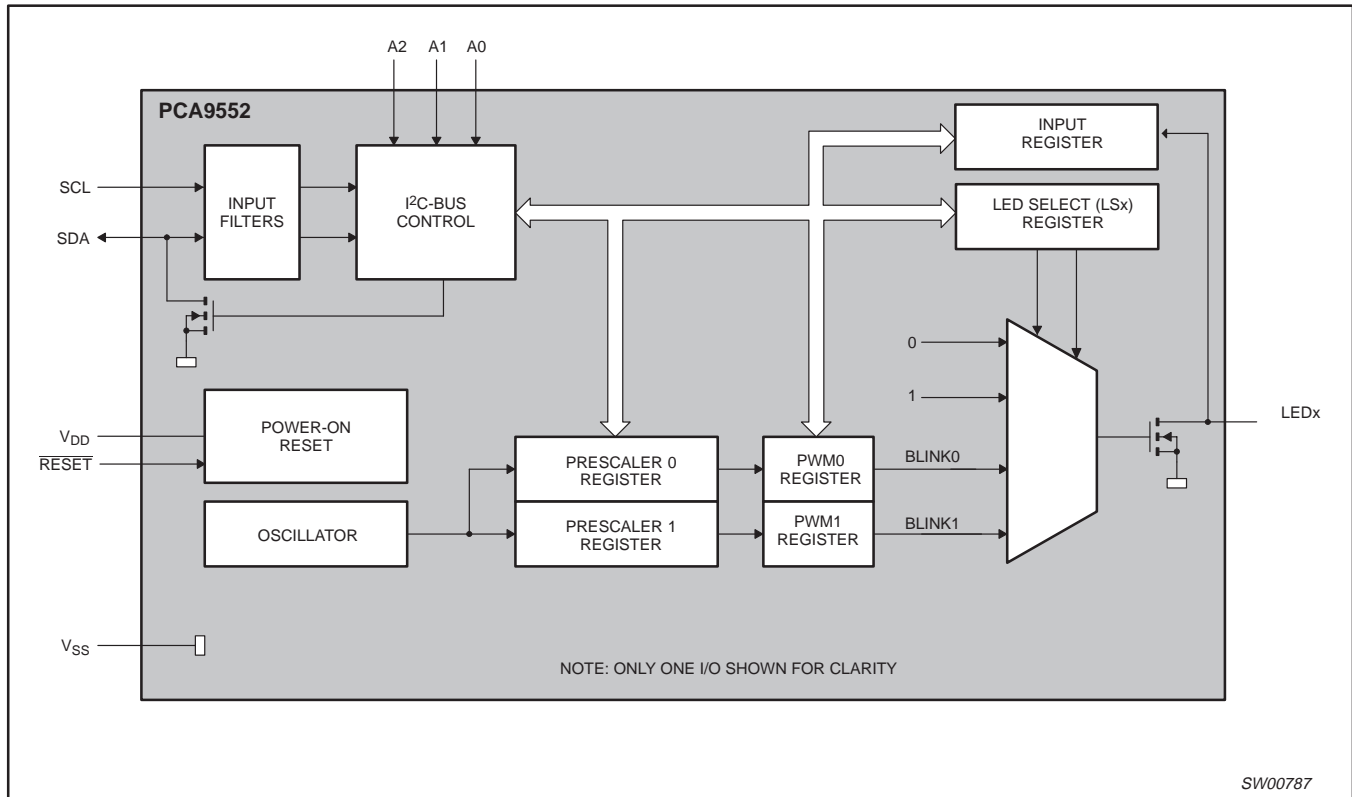


Figure 3. Block diagram

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## DEVICE ADDRESSING

Following a START condition the bus master must output the address of the slave it is accessing. The address of the PCA9552 is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

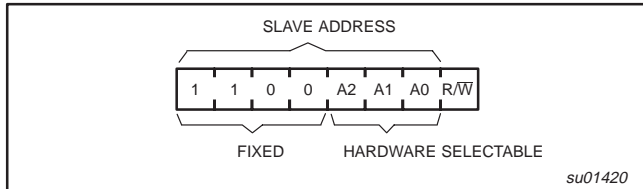


Figure 4. Slave address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

## CONTROL REGISTER

Following the successful acknowledgement of the slave address, the bus master will send a byte to the PCA9552 which will be stored in the Control Register. This register can be read and written via the I<sup>2</sup>C-bus.

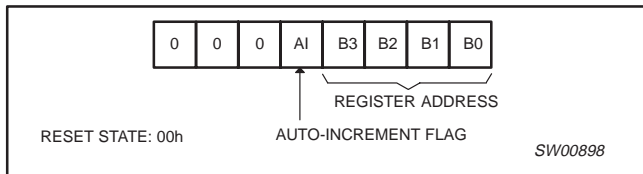


Figure 5. Control register

The lowest 3 bits are used as a pointer to determine which register will be accessed.

If the auto-increment flag (AI) is set, the four low order bits of the Control Register are automatically incremented after a read or write. This allows the user to program the registers sequentially. The contents of these bits will rollover to '0000' after the last register is accessed.

When auto-increment flag is set (AI = 1) and a read sequence is initiated, the sequence must start by reading a register different from '0' (B3 B2 B1 B0 ≠ 0 0 0 0).

Only the 4 least significant bits are affected by the AI flag.

Unused bits must be programmed with zeroes.

## Control Register definition

| B3 | B2 | B1 | B0 | REGISTER NAME | TYPE        | REGISTER FUNCTION     |
|----|----|----|----|---------------|-------------|-----------------------|
| 0  | 0  | 0  | 0  | INPUT0        | READ        | INPUT REGISTER 0      |
| 0  | 0  | 0  | 1  | INPUT1        | READ        | INPUT REGISTER 1      |
| 0  | 0  | 1  | 0  | PSC0          | READ/ WRITE | FREQUENCY PRESCALER 0 |
| 0  | 0  | 1  | 1  | PWM0          | READ/ WRITE | PWM REGISTER 0        |
| 0  | 1  | 0  | 0  | PSC1          | READ/ WRITE | FREQUENCY PRESCALER 1 |
| 0  | 1  | 0  | 1  | PWM1          | READ/ WRITE | PWM REGISTER 1        |
| 0  | 1  | 1  | 0  | LS0           | READ/ WRITE | LED 0–3 SELECTOR      |
| 0  | 1  | 1  | 1  | LS1           | READ/ WRITE | LED 4–7 SELECTOR      |
| 1  | 0  | 0  | 0  | LS2           | READ/ WRITE | LED 8–11 SELECTOR     |
| 1  | 0  | 0  | 1  | LS3           | READ/ WRITE | LED 12–15 SELECTOR    |

## REGISTER DESCRIPTION

### INPUT0 — INPUT REGISTER 0

|         | LED 7 | LED 6 | LED 5 | LED 4 | LED 3 | LED 2 | LED 1 | LED 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| bit     | 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| default | X     | X     | X     | X     | X     | X     | X     | X     |

The INPUT register 0 reflects the state of the device pins (inputs 0 to 7). Writes to this register will be acknowledged but will have no effect.

**NOTE:** The default value "X" is determined by the externally applied logic level, normally '1' when used for directly driving LED with pull-up to V<sub>DD</sub>.

### INPUT1 — INPUT REGISTER 1

|         | LED 15 | LED 14 | LED 13 | LED 12 | LED 11 | LED 10 | LED 9 | LED 8 |
|---------|--------|--------|--------|--------|--------|--------|-------|-------|
| bit     | 7      | 6      | 5      | 4      | 3      | 2      | 1     | 0     |
| default | X      | X      | X      | X      | X      | X      | X     | X     |

The INPUT register 1 reflects the state of the device pins (inputs 8 to 15). Writes to this register will be acknowledged but will have no effect.

**NOTE:** The default value "X" is determined by the externally applied logic level, normally '1' when used for directly driving LED with pull-up to V<sub>DD</sub>.

### PSC0 — FREQUENCY PRESCALER 0

| bit     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

PSC0 is used to program the period of the PWM output.

$$\text{The period of BLINK0} = \frac{(\text{PSC0} + 1)}{44}$$

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### PWM0 — PWM REGISTER 0

| bit     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PWM0 register determines the duty cycle of BLINK0. The outputs are LOW (LED off) when the count is less than the value in PWM0 and HIGH when it is greater. If PWM0 is programmed with 00h, then the PWM0 output is always LOW.

The duty cycle of BLINK0 is:  $\frac{256 - PWM0}{256}$

### PSC1 — FREQUENCY PRESCALER 1

| bit     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

PSC1 is used to program the period of PWM output.

The period of BLINK1 =  $\frac{(PSC1 + 1)}{44}$

### PWM1 — PWM REGISTER 1

| bit     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|---|---|---|---|---|---|---|
| default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The PWM1 register determines the duty cycle of BLINK1. The outputs are LOW (LED off) when the count is less than the value in PWM1 and HIGH when it is greater. If PWM1 is programmed with 00h, then the PWM1 output is always LOW.

The duty cycle of BLINK1 is:  $\frac{256 - PWM1}{256}$

### LS0 — LED 0-3 SELECTOR

|         | LED 3 |   | LED 2 |   | LED 1 |   | LED 0 |   |
|---------|-------|---|-------|---|-------|---|-------|---|
| bit     | 7     | 6 | 5     | 4 | 3     | 2 | 1     | 0 |
| default | 0     | 1 | 0     | 1 | 0     | 1 | 0     | 1 |

### LS1 — LED 4-7 SELECTOR

|         | LED 7 |   | LED 6 |   | LED 5 |   | LED 4 |   |
|---------|-------|---|-------|---|-------|---|-------|---|
| bit     | 7     | 6 | 5     | 4 | 3     | 2 | 1     | 0 |
| default | 0     | 1 | 0     | 1 | 0     | 1 | 0     | 1 |

### LS2 — LED 8-11 SELECTOR

|         | LED 11 |   | LED 10 |   | LED 9 |   | LED 8 |   |
|---------|--------|---|--------|---|-------|---|-------|---|
| bit     | 7      | 6 | 5      | 4 | 3     | 2 | 1     | 0 |
| default | 0      | 1 | 0      | 1 | 0     | 1 | 0     | 1 |

### LS3 — LED 12-15 SELECTOR

|         | LED 15 |   | LED 14 |   | LED 13 |   | LED 12 |   |
|---------|--------|---|--------|---|--------|---|--------|---|
| bit     | 7      | 6 | 5      | 4 | 3      | 2 | 1      | 0 |
| default | 0      | 1 | 0      | 1 | 0      | 1 | 0      | 1 |

The LSx LED select registers determine the source of the LED data.

- 00 = Output is set LOW (LED on)
- 01 = Output is set Hi-Z (LED off – default)
- 10 = Output blinks at PWM0 rate
- 11 = Output blinks at PWM1 rate

### PINS USED AS GENERAL PURPOSE I/Os

LED pins not used to control LEDs can be used as general purpose I/Os.

For use as input: Set LEDx to high-impedance (01) and then read the pin state via the input register.

For use as output: Connect external pull-up resistor to the pin and size it according to the DC recommended operating characteristics. LED output pin is HIGH when the output is programmed as high-impedance, and LOW when the output is programmed LOW through the “LED selector” register. The output can be pulse-width controlled when PWM0 or PWM1 are used.

### POWER-ON RESET

When power is applied to V<sub>DD</sub>, an internal Power-On Reset holds the PCA9552 in a reset condition until V<sub>DD</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the PCA9552 registers are initialized to their default states, all the outputs in the off state. Thereafter, V<sub>DD</sub> must be lowered below 0.2 V to reset the device.

### EXTERNAL RESET

A reset can be accomplished by holding the RESET pin LOW for a minimum of t<sub>W</sub>. The PCA9552 registers and I<sup>2</sup>C state machine will be held in their default state until the RESET input is once again HIGH.

This input requires a pull-up resistor to V<sub>DD</sub> if no active connection is used.

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## CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 6).

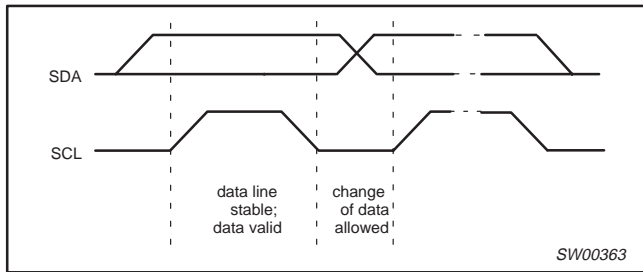


Figure 6. Bit transfer

### Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Figure 7).

### System configuration

A device generating a message is a transmitter: a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 8).

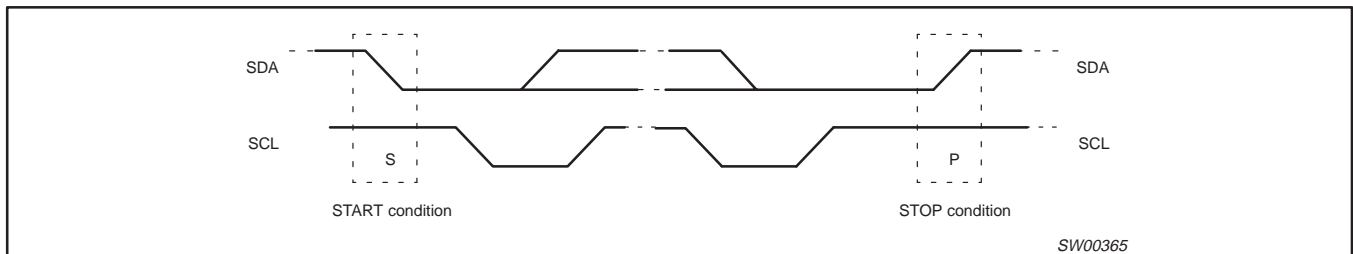


Figure 7. Definition of start and stop conditions

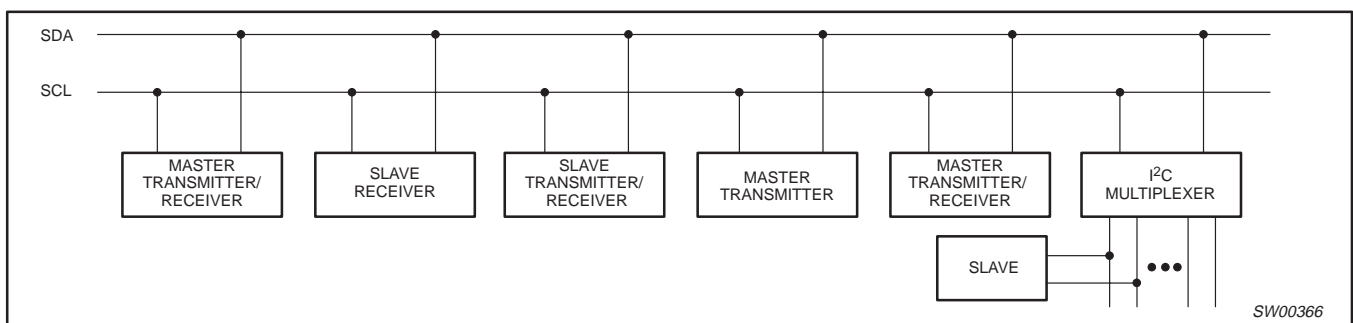


Figure 8. System configuration

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## Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

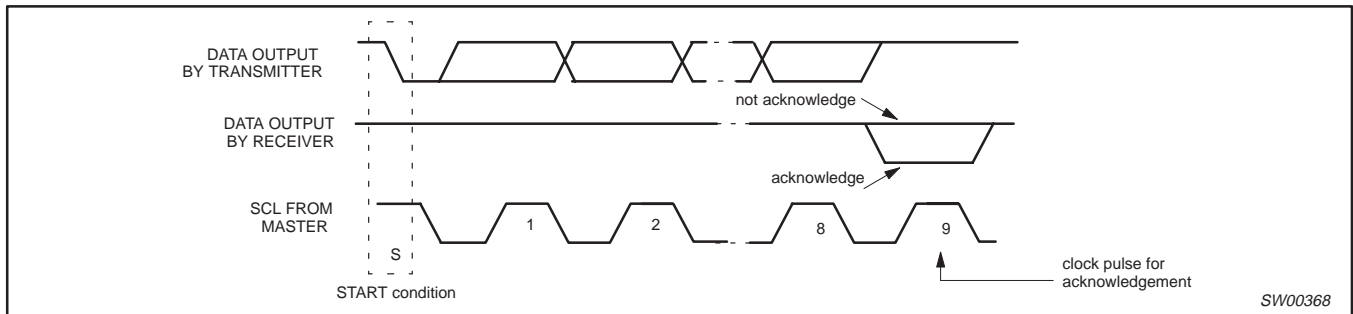


Figure 9. Acknowledgement on the I<sup>2</sup>C-bus



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## Bus transactions

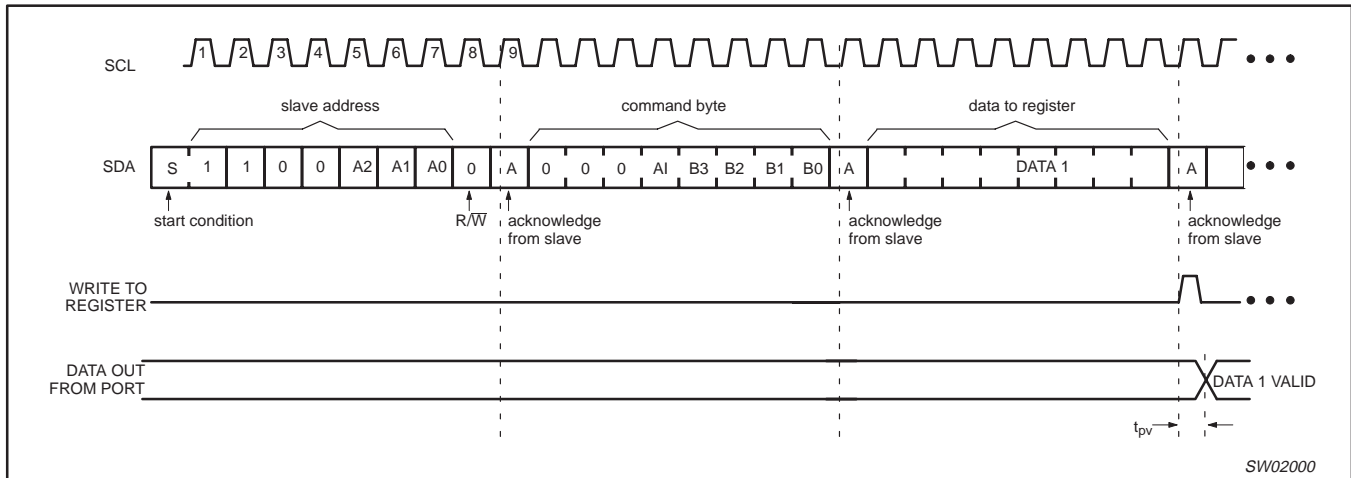


Figure 10. WRITE to register

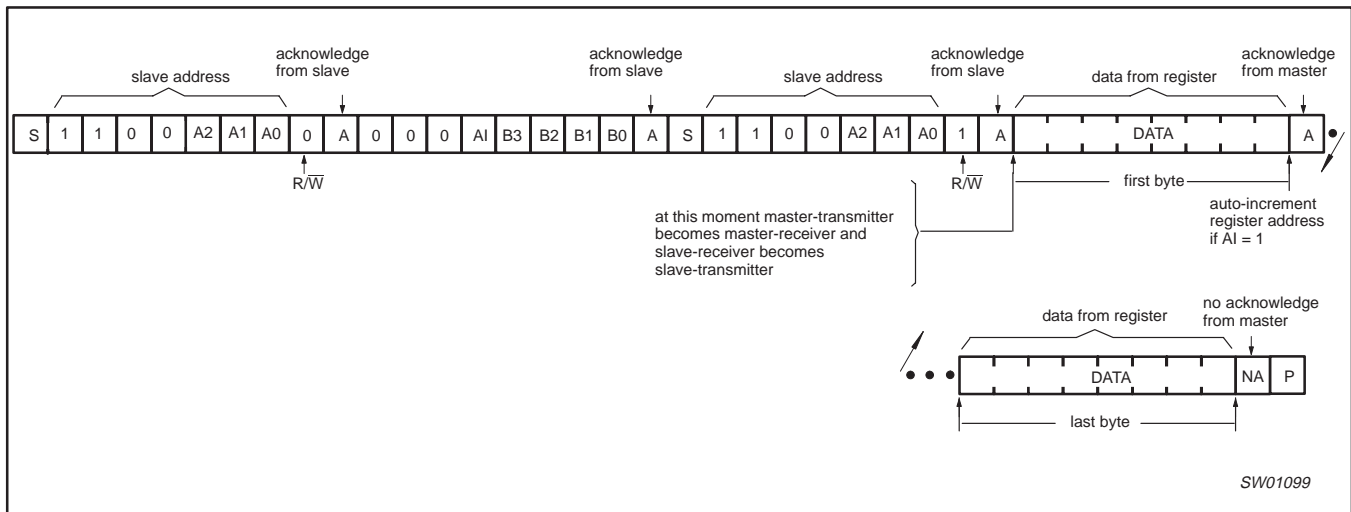
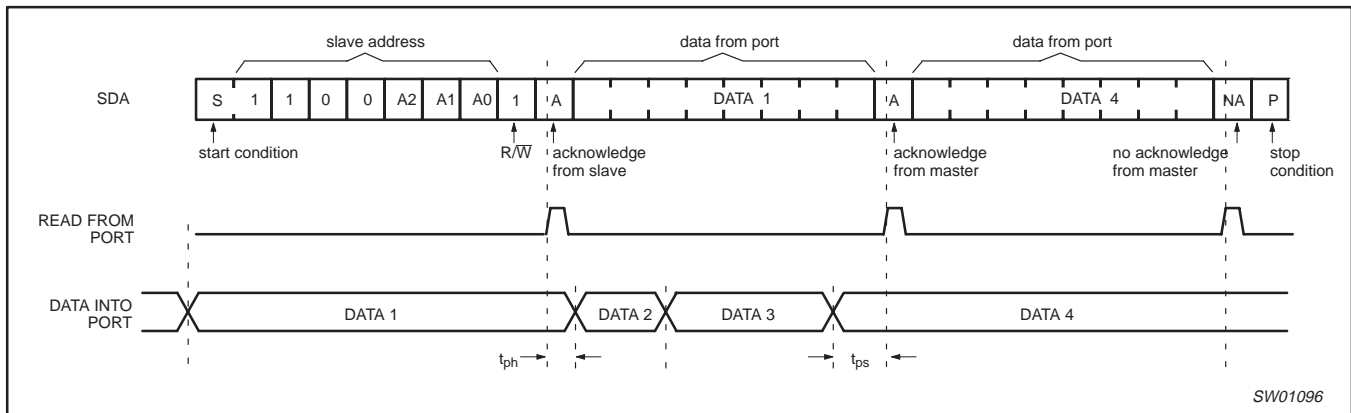


Figure 11. READ from register



**NOTE:**

- This figure assumes the command byte has previously been programmed with 00h.

Figure 12. READ input port register

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## APPLICATION DATA

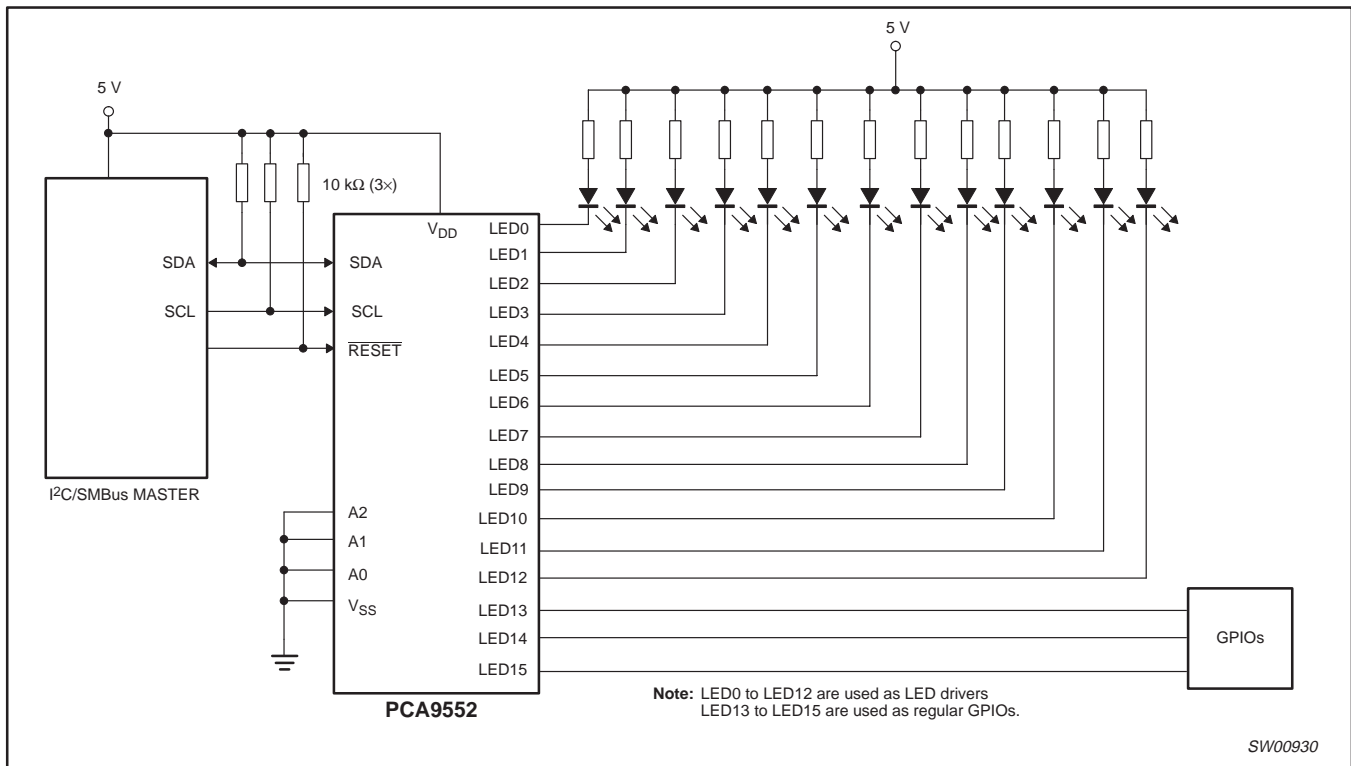


Figure 13. Typical application

### Minimizing I<sub>DD</sub> when the I/O is used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 13. Since the LED acts as a diode, when the LED is off the I/O V<sub>IN</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>IN</sub> becomes lower than V<sub>DD</sub> and is specified as ΔI<sub>DD</sub> in the DC characteristics table.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 14 shows a high value resistor in parallel with the LED. Figure 15 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>IN</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.

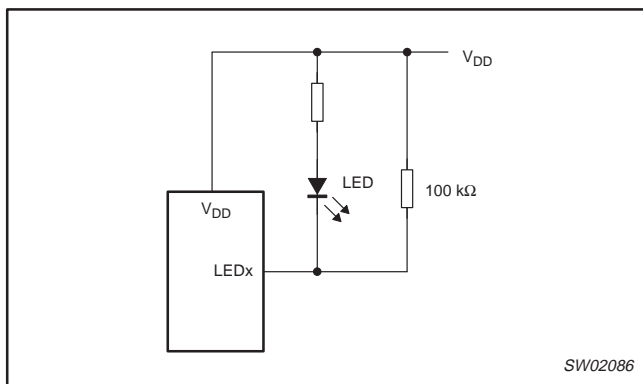


Figure 14. High value resistor in parallel with the LED

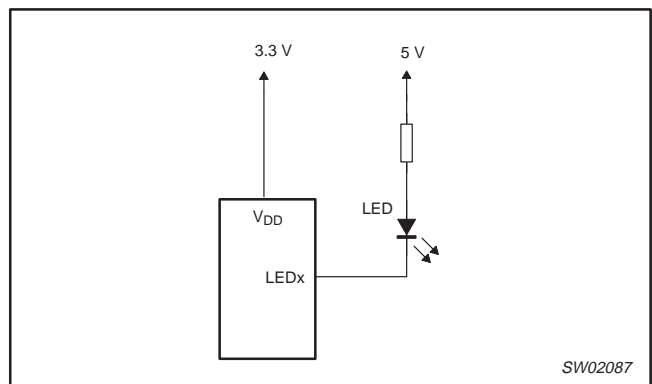


Figure 15. Device supplied by a lower voltage

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**Programming example**

The following example will show how to set LED0 to LED3 on. It will then set LED4 and LED5 to blink at 1 Hz at a 50% duty cycle. LED6 and LED7 will be set to blink at 4 Hz and at a 25% duty cycle. LED8 to LED15 will be set to off.

**Table 1.**

|  | I <sup>2</sup> C-bus |
|--|----------------------|
| Start  | S                    |
| PCA9552 address with A0–A2 = low   | C0h                  |
| PSC0 subaddress + auto-increment   | 12h                  |
| Set prescaler PSC0 to achieve a period of 1 second:<br>$\text{Blink period} = 1 = \frac{\text{PSC0} + 1}{44}$ PSC0 = 43        | 2Bh                  |
| Set PWM0 duty cycle to 50%:<br>$\frac{256 - \text{PWM0}}{256} = 0.5$ PWM0 = 128  | 80h                  |
| Set prescaler PCS1 to achieve a period of 0.25 seconds:<br>$\text{Blink period} = 0.25 = \frac{\text{PSC1} + 1}{44}$ PSC1 = 10 | 0Ah                  |
| Set PWM1 output duty cycle to 25%:<br>$\frac{256 - \text{PWM1}}{256} = 0.25$ PWM1 = 192  | C0h                  |
| Set LED0 to LED3 on  | 00h                  |
| Set LED4 and 5 to PWM0, and LED6 or 7 to PWM1  | FAh                  |
| Set LED8 to LED11 off  | 55h                  |
| Set LED12 to LED15 off   | 55h                  |
| Stop   | P                    |

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**ABSOLUTE MAXIMUM RATINGS**

In accordance with the Absolute Maximum Rating System (IEC 134)

| SYMBOL           | PARAMETER                     | CONDITIONS | MIN                   | MAX  | UNIT |
|------------------|-------------------------------|------------|-----------------------|------|------|
| V <sub>DD</sub>  | Supply voltage                |            | -0.5                  | 6.0  | V    |
| V <sub>I/O</sub> | DC voltage on an I/O          |            | V <sub>SS</sub> - 0.5 | 5.5  | V    |
| I <sub>I/O</sub> | DC output current on an I/O   |            | —                     | ±25  | mA   |
| I <sub>SS</sub>  | Supply current                |            | —                     | 200  | mA   |
| P <sub>tot</sub> | Total power dissipation       |            | —                     | 400  | mW   |
| T <sub>stg</sub> | Storage temperature range     |            | -65                   | +150 | °C   |
| T <sub>amb</sub> | Operating ambient temperature |            | -40                   | +85  | °C   |

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC24 under "Handling MOS devices".

**DC CHARACTERISTICS**V<sub>DD</sub> = 2.3 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; unless otherwise specified. TYP at 3.3 V and 25 °C.

| SYMBOL                                  | PARAMETER                       | CONDITIONS   | MIN                 | TYP | MAX                 | UNIT |
|---|---------------------------------|--|---------------------|-----|---------------------|------|
| <b>Supplies</b>                         |                                 |  |                     |     |                     |      |
| V <sub>DD</sub>                         | Supply voltage                  |  | 2.3                 | —   | 5.5                 | V    |
| I <sub>DD</sub>                         | Supply current                  | Operating mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz | —                   | 350 | 550                 | μA   |
| I <sub>stb</sub>                        | Standby current                 | Standby mode; V <sub>DD</sub> = 5.5 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 0 kHz     | —                   | 2.1 | 5.0                 | μA   |
| ΔI <sub>DD</sub>                        | Additional standby current      | Standby mode; V <sub>DD</sub> = 5.5 V; Every LED I/O at V <sub>IN</sub> = 4.3 V; f <sub>SCL</sub> = 0 kHz                          | —                   | —   | 2                   | mA   |
| V <sub>POR</sub>                        | Power-on reset voltage (Note 1) | V <sub>DD</sub> = 3.3 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>  | —                   | 1.7 | 2.2                 | V    |
| <b>Input SCL; input/output SDA</b>      |                                 |  |                     |     |                     |      |
| V <sub>IL</sub>                         | LOW-level input voltage         |  | -0.5                | —   | 0.3 V <sub>DD</sub> | V    |
| V <sub>IH</sub>                         | HIGH-level input voltage        |  | 0.7 V <sub>DD</sub> | —   | 5.5                 | V    |
| I <sub>OL</sub>                         | LOW-level output current        | V <sub>OL</sub> = 0.4 V  | 3                   | 6.5 | —                   | mA   |
| I <sub>L</sub>                          | Leakage current                 | V <sub>I</sub> = V <sub>DD</sub> = V <sub>SS</sub>   | -1                  | —   | +1                  | μA   |
| C <sub>I</sub>                          | Input capacitance               | V <sub>I</sub> = V <sub>SS</sub>   | —                   | 4.4 | 5                   | pF   |
| <b>I/Os</b>                             |                                 |  |                     |     |                     |      |
| V <sub>IL</sub>                         | LOW-level input voltage         |  | -0.5                | —   | 0.8                 | V    |
| V <sub>IH</sub>                         | HIGH-level input voltage        |  | 2.0                 | —   | 5.5                 | V    |
| I <sub>OL</sub>                         | LOW-level output current        | V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 2.3 V; Note 2   | 9                   | —   | —                   | mA   |
|   |                                 | V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 3.0 V; Note 2   | 12                  | —   | —                   | mA   |
|   |                                 | V <sub>OL</sub> = 0.4 V; V <sub>DD</sub> = 5.0 V; Note 2   | 15                  | —   | —                   | mA   |
|   |                                 | V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 2.3 V; Note 2   | 15                  | —   | —                   | mA   |
|   |                                 | V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 3.0 V; Note 2   | 20                  | —   | —                   | mA   |
|   |                                 | V <sub>OL</sub> = 0.7 V; V <sub>DD</sub> = 5.0 V; Note 2   | 25                  | —   | —                   | mA   |
| I <sub>L</sub>                          | Input leakage current           | V <sub>DD</sub> = 3.6 V; V <sub>I</sub> = 0 V or V <sub>DD</sub>   | -1                  | —   | 1                   | μA   |
| C <sub>IO</sub>                         | Input/output capacitance        |  | —                   | 2.6 | 5                   | pF   |
| <b>Select Inputs A0, A1, A2 / RESET</b> |                                 |  |                     |     |                     |      |
| V <sub>IL</sub>                         | LOW-level input voltage         |  | -0.5                | —   | 0.8                 | V    |
| V <sub>IH</sub>                         | HIGH-level input voltage        |  | 2.0                 | —   | 5.5                 | V    |
| I <sub>LI</sub>                         | Input leakage current           |  | -1                  | —   | 1                   | μA   |
| C <sub>I</sub>                          | Input capacitance               | V <sub>I</sub> = V <sub>SS</sub>   | —                   | 2.3 | 5                   | pF   |

**NOTES:**

- V<sub>DD</sub> must be lowered to 0.2 V in order to reset part.
- Each I/O must be externally limited to a maximum of 25 mA and each octal (LED0–LED7 and LED8–LED15) must be limited to a maximum current of 100 mA for a device total of 200 mA.

16-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9552

## AC SPECIFICATIONS

| SYMBOL                            | PARAMETER  | STANDARD MODE<br>I <sup>2</sup> C-BUS |      | FAST MODE<br>I <sup>2</sup> C-BUS    |     | UNITS |
|-----------------------------------|--|---------------------------------------|------|--------------------------------------|-----|-------|
|                                   |  | MIN                                   | MAX  | MIN                                  | MAX |       |
| f <sub>SCL</sub>                  | Operating frequency  | 0                                     | 100  | 0                                    | 400 | kHz   |
| t <sub>BUF</sub>                  | Bus free time between STOP and START conditions                    | 4.7                                   | —    | 1.3                                  | —   | μs    |
| t <sub>HD;STA</sub>               | Hold time after (repeated) START condition                         | 4.0                                   | —    | 0.6                                  | —   | μs    |
| t <sub>SU;STA</sub>               | Repeated START condition set-up time                               | 4.7                                   | —    | 0.6                                  | —   | μs    |
| t <sub>SU;STO</sub>               | Set-up time for STOP condition                                     | 4.0                                   | —    | 0.6                                  | —   | μs    |
| t <sub>HD;DAT</sub>               | Data in hold time  | 0                                     | —    | 0                                    | —   | ns    |
| t <sub>VD;ACK</sub>               | Valid time for ACK condition <sup>2</sup>                          | —                                     | 600  | —                                    | 600 | ns    |
| t <sub>VD;DAT (L)</sub>           | Data out valid time <sup>3</sup>                                   | —                                     | 600  | —                                    | 600 | ns    |
| t <sub>VD;DAT (H)</sub>           | Data out valid time <sup>3</sup>                                   | —                                     | 1500 | —                                    | 600 | ns    |
| t <sub>SU;DAT</sub>               | Data set-up time   | 250                                   | —    | 100                                  | —   | ns    |
| t <sub>LOW</sub>                  | Clock LOW period   | 4.7                                   | —    | 1.3                                  | —   | μs    |
| t <sub>HIGH</sub>                 | Clock HIGH period  | 4.0                                   | —    | 0.6                                  | —   | μs    |
| t <sub>F</sub>                    | Clock/Data fall time   | —                                     | 300  | 20 + 0.1 C <sub>b</sub> <sup>1</sup> | 300 | ns    |
| t <sub>R</sub>                    | Clock/Data rise time   | —                                     | 1000 | 20 + 0.1 C <sub>b</sub> <sup>1</sup> | 300 | ns    |
| t <sub>SP</sub>                   | Pulse width of spikes that must be suppressed by the input filters | —                                     | 50   | —                                    | 50  | ns    |
| <b>Port Timing</b>                |  |                                       |      |                                      |     |       |
| t <sub>PV</sub>                   | Output data valid  | —                                     | 200  | —                                    | 200 | ns    |
| t <sub>PS</sub>                   | Input data setup time  | 100                                   | —    | 100                                  | —   | ns    |
| t <sub>PH</sub>                   | Input data hold time   | 1                                     | —    | 1                                    | —   | μs    |
| <b>Reset</b>                      |  |                                       |      |                                      |     |       |
| t <sub>W</sub>                    | Reset pulse width  | 10                                    | —    | 10                                   | —   | ns    |
| t <sub>REC</sub>                  | Reset recovery time  | 0                                     | —    | 0                                    | —   | ns    |
| t <sub>RESET</sub> <sup>4,5</sup> | Time to reset  | 400                                   | —    | 400                                  | —   | ns    |

## NOTES:

1. C<sub>b</sub> = total capacitance of one bus line in pF.
2. t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. t<sub>VD;DAT</sub> = minimum time for SDA data out to be valid following SCL LOW.
4. Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
5. Upon reset, the full delay will be the sum of t<sub>RESET</sub> and the RC time constant of the SDA bus.

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

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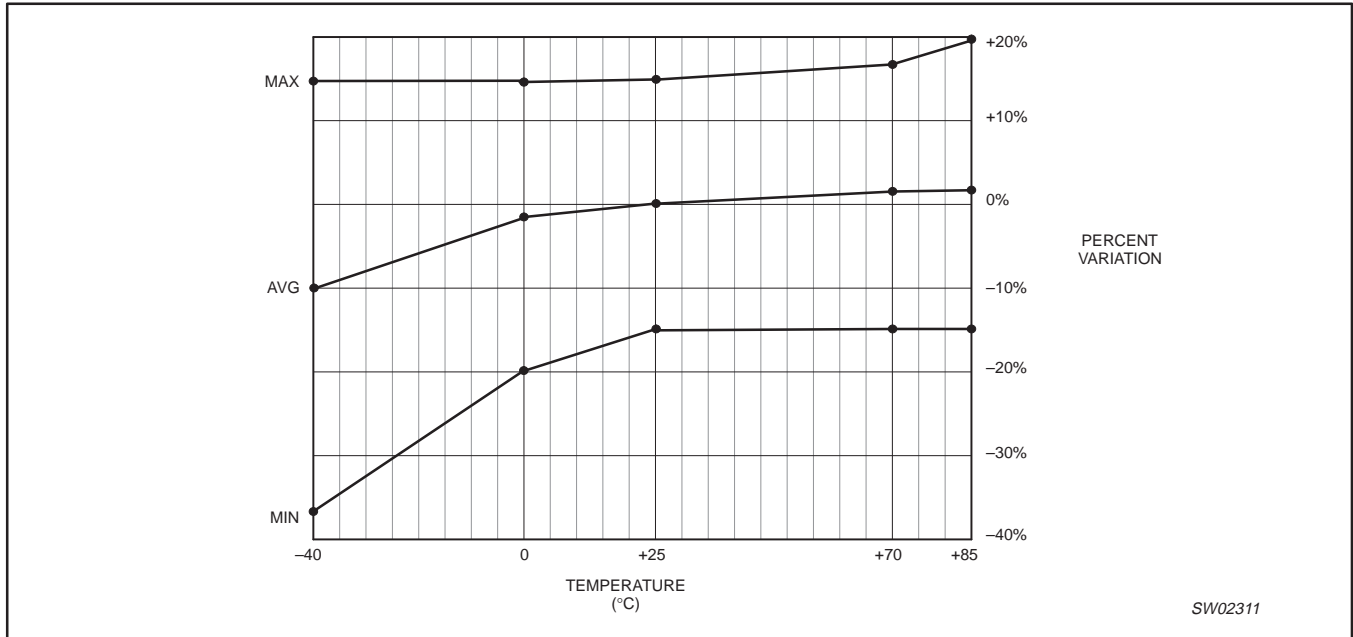


Figure 16. Typical frequency variation over process at V<sub>DD</sub> = 2.3 V to 3.0 V

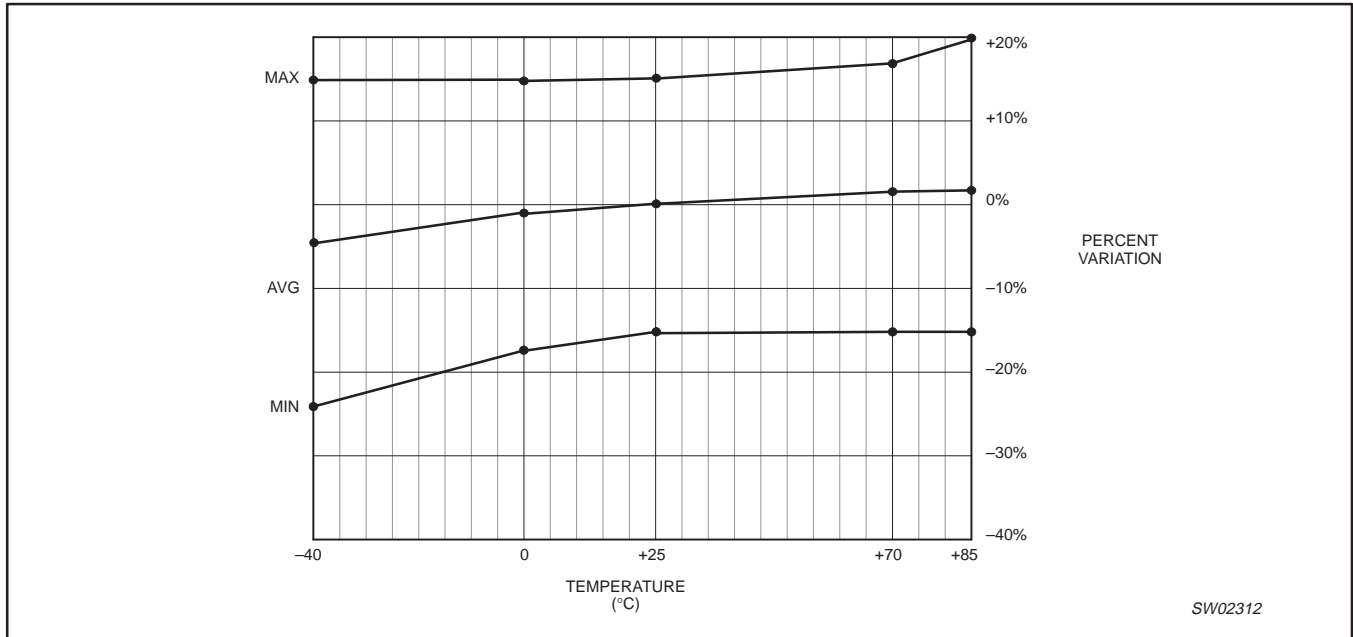


Figure 17. Typical frequency variation over process at V<sub>DD</sub> = 3.0 V to 5.5 V

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

# PCA9552

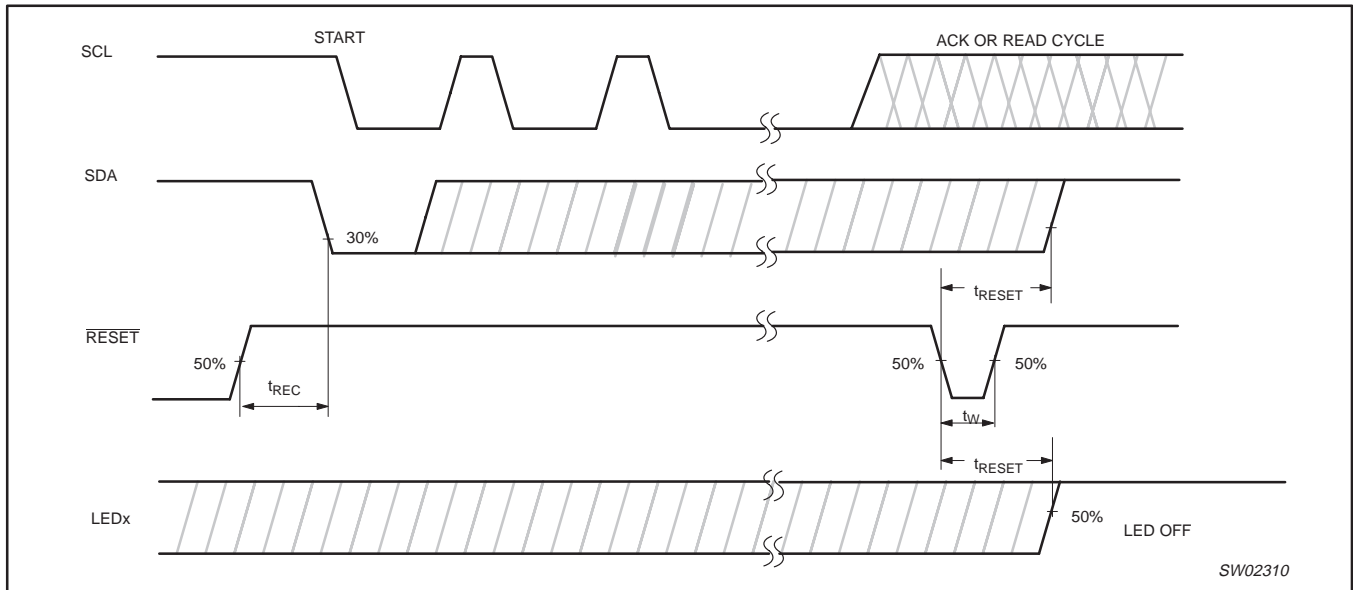


Figure 18. Definition of RESET timing

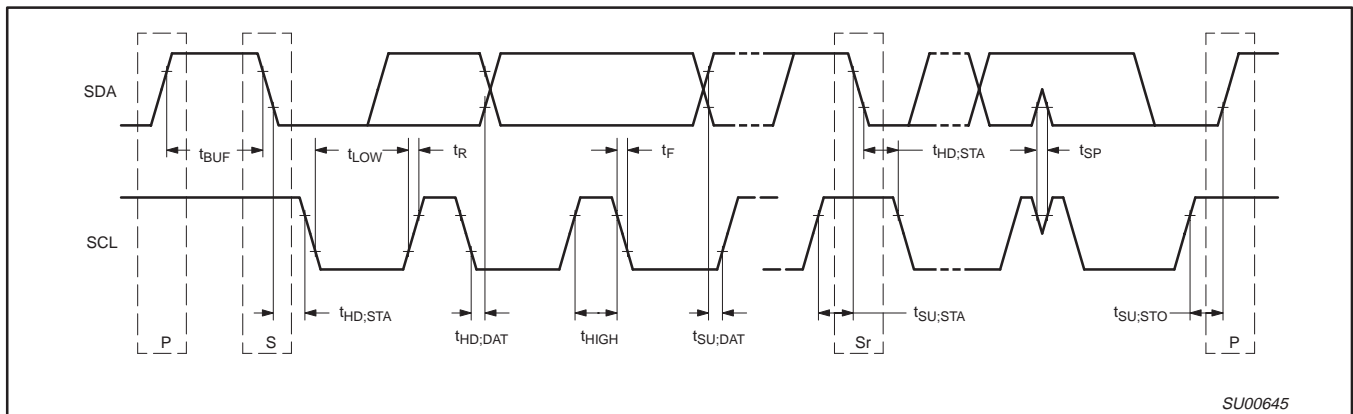


Figure 19. Definition of timing

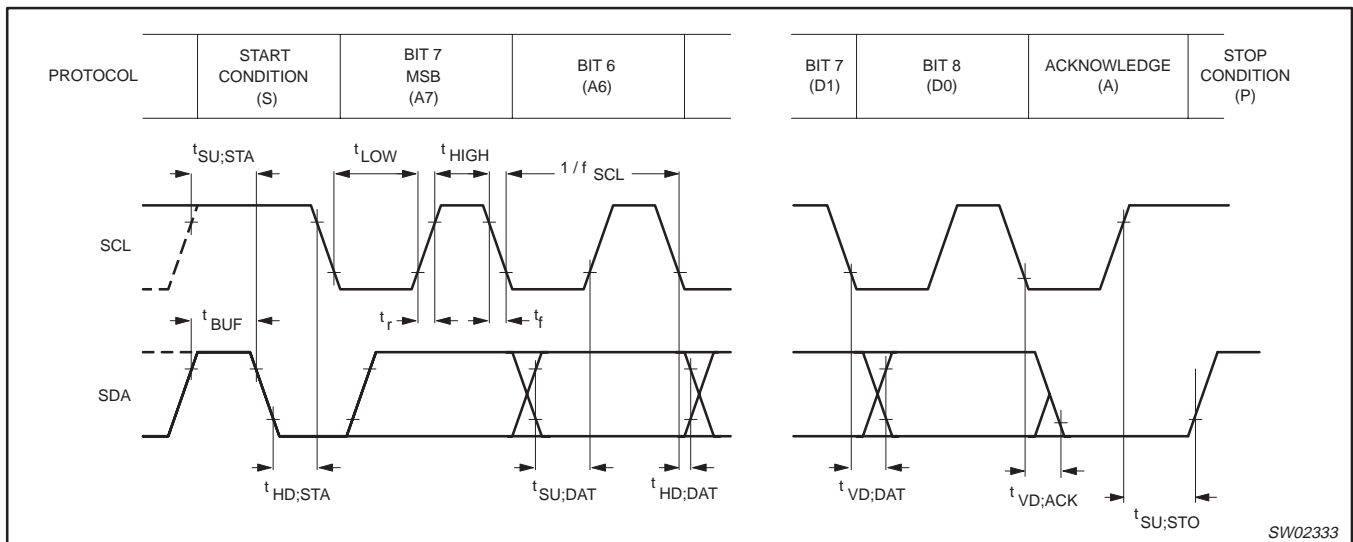


Figure 20. I<sup>2</sup>C-bus timing diagram; rise and fall times refer to V<sub>IL</sub> and V<sub>IH</sub>

16-bit I<sup>2</sup>C LED driver with programmable blink rates

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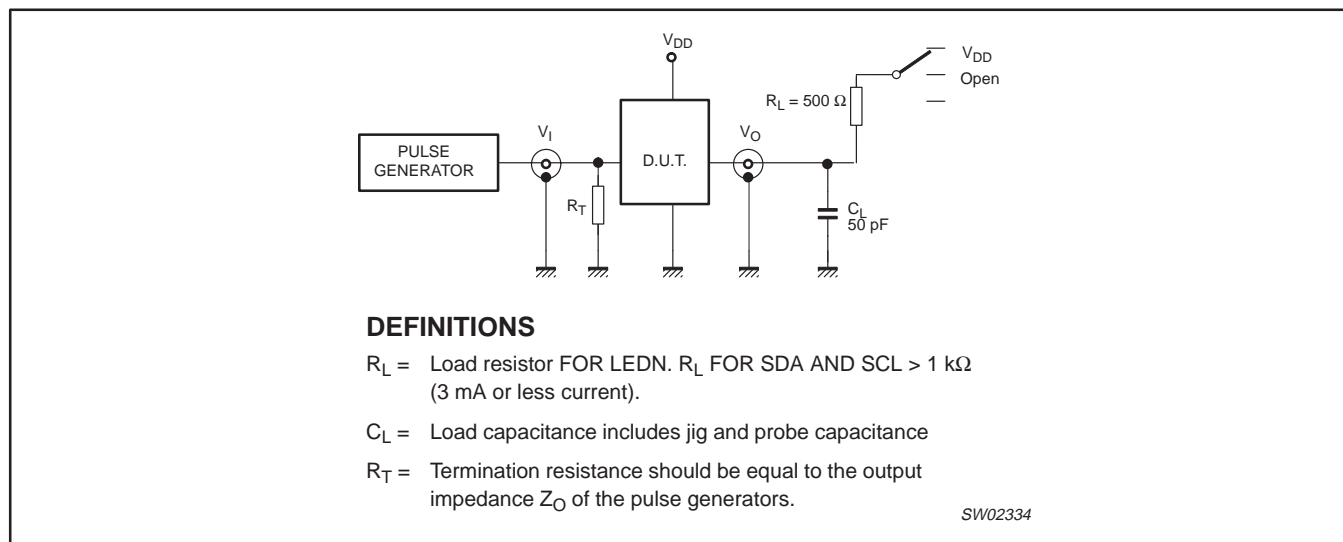


Figure 21. Test circuitry for switching times

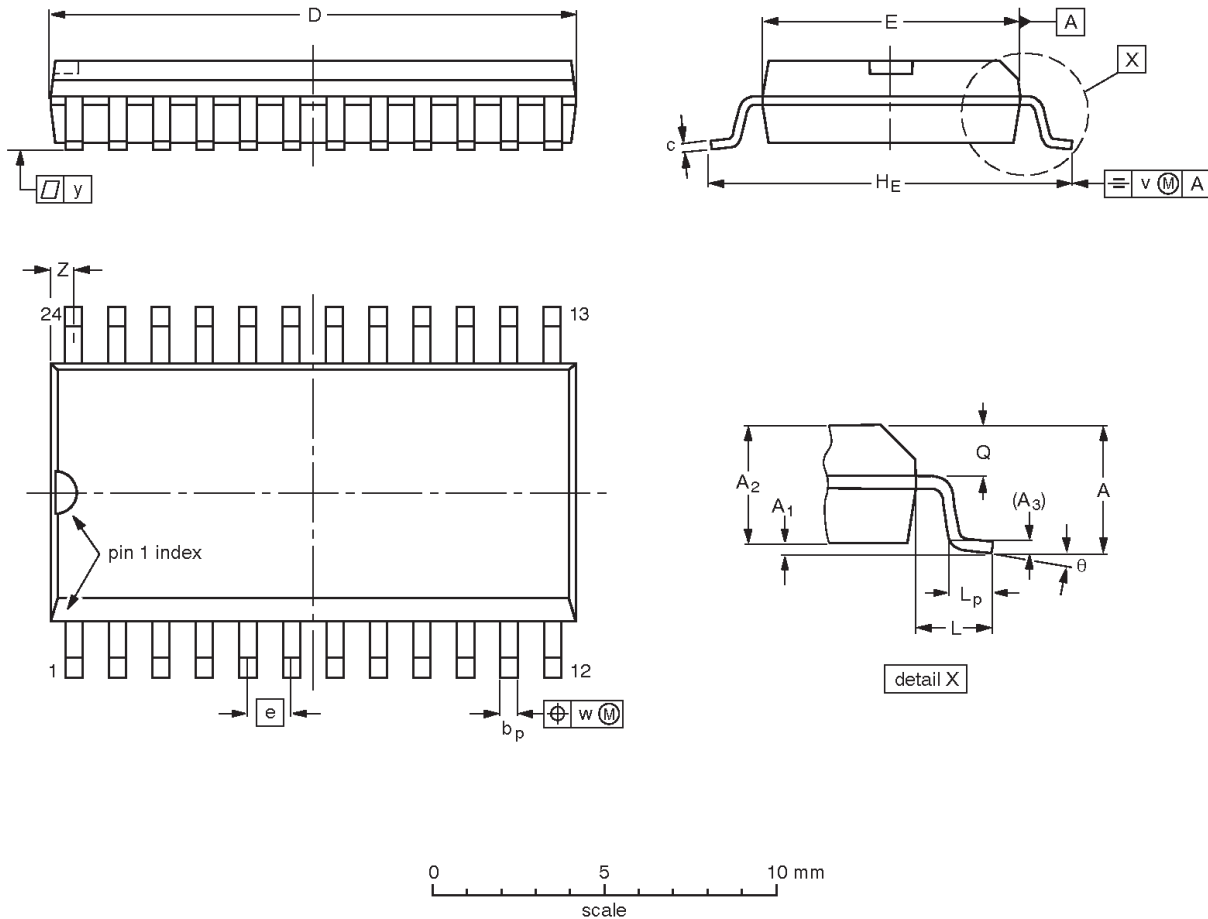


# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9552

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.3<br>0.1     | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 15.6<br>15.2     | 7.6<br>7.4       | 1.27 | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.1    | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60     | 0.30<br>0.29     | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

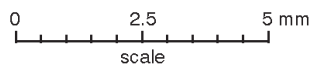
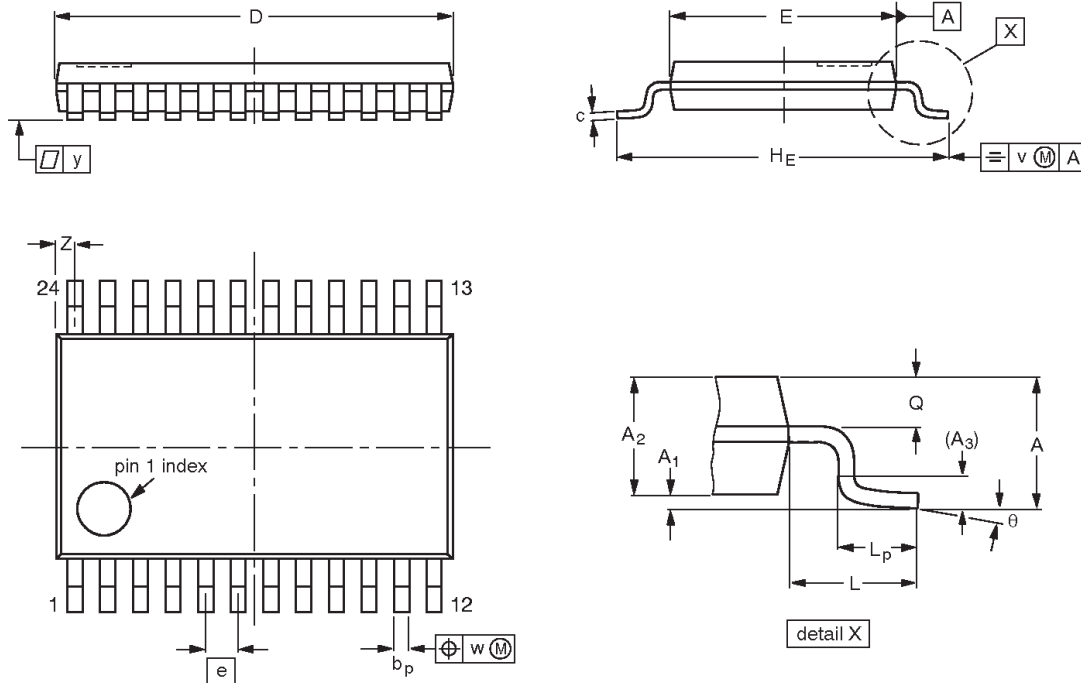
| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|-------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                       |
| SOT137-1        | 075E05     | MS-013 |       |  |                     | -99-12-27<br>03-02-19 |

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9552

**TSSOP24:** plastic thin shrink small outline package; 24 leads; body width 4.4 mm

**SOT355-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.1    | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 7.9<br>7.7       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.5<br>0.2       | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

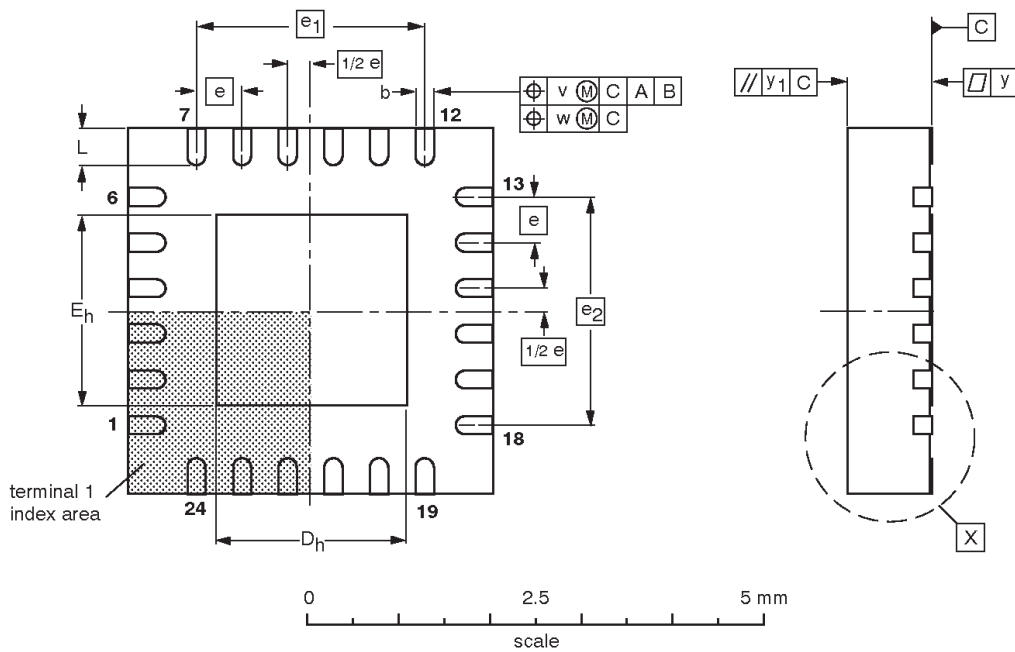
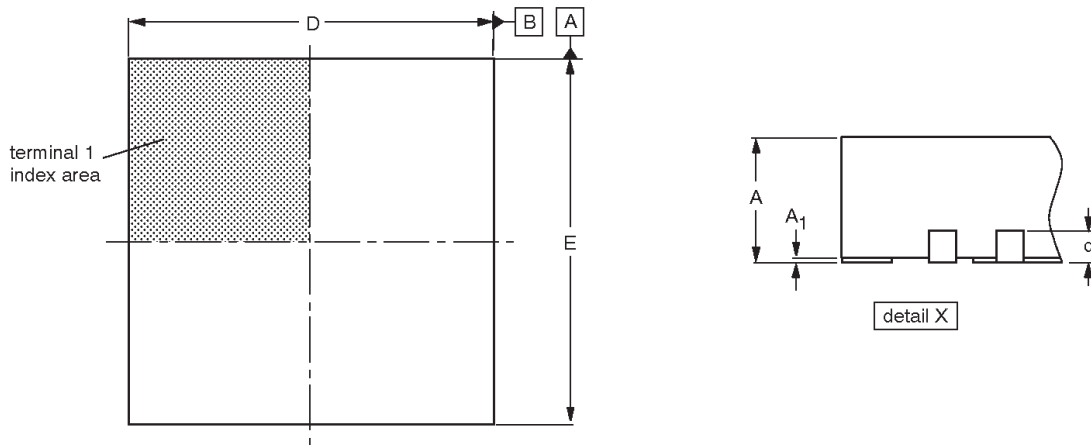
| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|-------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                       |
| SOT355-1        |            | MO-153 |       |  |                     | -99-12-27<br>03-02-19 |

# 16-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9552

**HVQFN24:** plastic thermal enhanced very thin quad flat package; no leads; 24 terminals;  
body 4 x 4 x 0.85 mm

SOT616-1



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A <sup>(1)</sup><br>max. | A <sub>1</sub> | b            | c   | D <sup>(1)</sup> | D <sub>h</sub> | E <sup>(1)</sup> | E <sub>h</sub> | e   | e <sub>1</sub> | e <sub>2</sub> | L          | v   | w    | y    | y <sub>1</sub> |
|------|--------------------------|----------------|--------------|-----|------------------|----------------|------------------|----------------|-----|----------------|----------------|------------|-----|------|------|----------------|
| mm   | 1                        | 0.05<br>0.00   | 0.30<br>0.18 | 0.2 | 4.1<br>3.9       | 2.25<br>1.95   | 4.1<br>3.9       | 2.25<br>1.95   | 0.5 | 2.5            | 2.5            | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1            |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE<br>VERSION | REFERENCES |        |       |  | EUROPEAN<br>PROJECTION | ISSUE DATE           |
|--------------------|------------|--------|-------|--|------------------------|----------------------|
|                    | IEC        | JEDEC  | JEITA |  |                        |                      |
| SOT616-1           | ---        | MO-220 | ---   |  |                        | 01-08-08<br>02-10-22 |

16-bit I<sup>2</sup>C LED driver with programmable blink rates

PCA9552

## REVISION HISTORY

| Rev | Date     | Description   |
|-----|----------|---|
| _4  | 20041001 | <p><b>Product data sheet (9397 750 13727). Supersedes data of 2003 May 02 (9397 750 11463).</b></p> <p>Modifications:</p> <ul style="list-style-type: none"> <li>● “Features” section on page 2: <ul style="list-style-type: none"> <li>– second bullet: change from “... between 0.15625 and 40 Hz (6.4 and 0.025 seconds)” to “... between 0.172 Hz and 44 Hz (5.82 and 0.023 seconds)”</li> </ul> </li> <li>● Section “Register Description” on page 5: <ul style="list-style-type: none"> <li>– “INPUT0 — INPUT REGISTER 1” changed to “INPUT0 — INPUT REGISTER 0”. (Also changed first sentence following table from “The INPUT register 1 reflects ... ” to “The INPUT register 0 reflects ...”.</li> <li>– “INPUT0 — INPUT REGISTER 0” table modified; note added</li> <li>– “INPUT1 — INPUT REGISTER 2” changed to “INPUT1 — INPUT REGISTER 1”.</li> <li>– “INPUT1 — INPUT REGISTER 1” table modified; note added</li> <li>– section “PCS0—Frequency Prescaler 0”: change denominator in equation from 38 to 44.</li> <li>– section “PCS1—Frequency Prescaler 1”: change denominator in equation from 38 to 44.</li> </ul> </li> <li>● Add section “Pins used as General Purpose I/Os” on page 6.</li> <li>● Section “Power-on Reset” on page 6 re-written.</li> <li>● Section “External Reset” on page 6: second paragraph changed from “This input requires a pull-up resistor to V<sub>DD</sub>.” to “This input requires a pull-up resistor to V<sub>DD</sub> if no active connection is used.”.</li> <li>● Figure 13 on page 10: add resistor values</li> <li>● Table 1 on page 11: <ul style="list-style-type: none"> <li>– step “Set prescaler PSC0 ...”: change equation denominator from 38 to 44; change ‘PSC0 = 37’ to ‘PSC0 = 43’; change I<sup>2</sup>C-bus address from ‘25h’ to ‘2Bh’</li> <li>– step “Set prescaler PCS1 ...”: change equation denominator from 38 to 44; change ‘PSC1 = 9’ to ‘PCS1 = 10’; change I<sup>2</sup>C-bus address from ‘09h’ to ‘0Ah’</li> </ul> </li> <li>● DC Characteristics table on page 12: add (new) Note 1 and its reference at V<sub>POR</sub>.</li> <li>● Add Figures 20 and 21.</li> </ul> |
| _3  | 20030502 | <b>Product data (9397 750 11463); ECN 853-2374 29857 of 24 April 2003; supersedes data of 24 February 2003 (9397 750 11156).</b>  |
| _2  | 20030224 | <b>Product data (9397 750 11156); ECN 853-2374 29331 of 20 December 2002; supersedes data of 2002 Sep 09 (9397 750 10329).</b>  |
| _1  | 20020927 | <b>Product data (9397 750 10329); ECN 853-2374 28878 of 09 September 2002.</b>  |

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| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2]</sup> [3] | Definitions  |
|-------|----------------------------------|-----------------------------------|--|
| I     | Objective data sheet             | Development                       | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Document order number: 9397 750 13727

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