GOULD

AMI Semiconductors

32 Bit, High Voltage Driver

S4535

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Features

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

Applications:

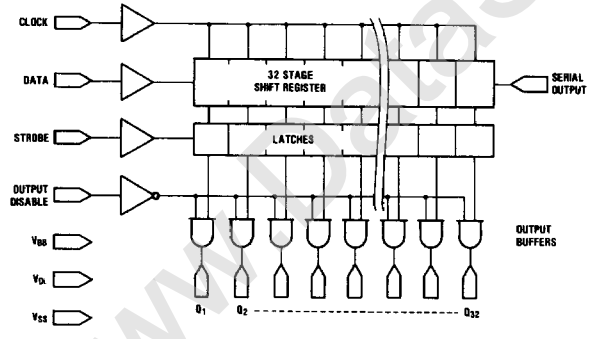
- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

General Description

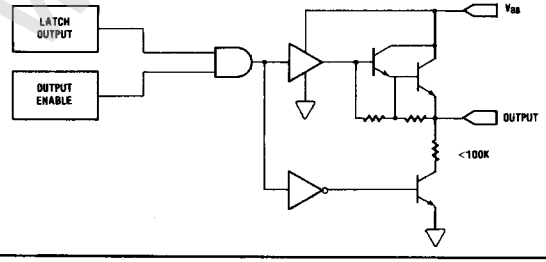
The S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

DISPLAY DRIVERS

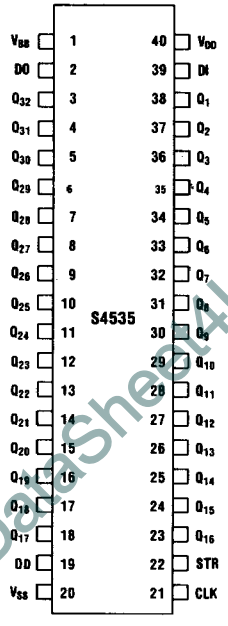
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



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Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	12V
V_{IN}	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Logic)	V_{SS} – .3V to V_{DD} + .3V
V_{OUT} (Display)	V_{SS} – .3V to V_{BB} + .3V
Power Dissipation	1.6W
Operating Temperature	– 40°C to + 85°C*
Storage Temperature	– 65°C to + 125°C

* Extended temperature range available. Please contact AMI for price and delivery information.

Operational Specification: $-40°C \leq T_A \leq +85°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	−0.3	0.8	V	
V_{IH}	Input One Level	3.5	$V_{DD}+0.3$	V	
V_{SL}	Signal Out Zero Level	V_{SS}	0.5	V	$I_{SO} = -20\mu A$
V_{SH}	Signal Out One Level	$V_{DD}-0.5$	V_{DD}	V	$I_{SO} = 20\mu A$
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		35	mA	No Loads, T = 25°C
I_{BB}	Display Supply Current		10	mA	No Loads, T = 25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O = -20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$ $V_{BB}-3.2$	V_{BB} V_{BB}	V V	$I_O = 5mA$ $I_O = 25mA$, One Output
t_{SD}	Serial Out Prop. Delay		500	ns	$C_L = 50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L = 50pF$
t_W	Input Pulse Width	500		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	50		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Pin Description

Pin #	Name	Description
20	V_{SS}	Ground Connection
2	DO	Output of Shift Register—primarily used for cascading
19	OD	Output Disable
1	V_{BB}	Q Output Drive Voltage
21	CLK	System Clock Input
40	V_{DD}	Logic Supply Voltage
22	STR	Strobe to Latch Data from Registers
39	DI	Data Input to Shift Register
3-18 and 23-38	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams